19-1097; Rev 3; 7/04

EVALUATION KIT AVAILABLE

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

General Description

The MAX3761/MAX3762 limiting amplifiers, with 4mV sensitivity and PECL data outputs, are optimized for operation in low-cost, 622Mbps, LAN/ATM LAN fiber optics applications.

An integrated power detector senses the input signal's amplitude. A received-signal-strength indicator (RSSI) gives an analog indication of the power level, while the complementary loss-of-signal (LOS) outputs indicate if the input power level exceeds the programmed threshold level. The LOS threshold can be adjusted to detect signal amplitudes between 3mVp-p and 100mVp-p, providing a 15dB LOS adjustment in fiber optic receivers. The LOS outputs have 3.5dB of hysteresis, which prevents chatter when input signal levels are small. The MAX3761's LOS outputs are compatible with TTL-logic levels. The MAX3762 has PECL LOS outputs.

DISABLE and LOS can be used to implement a squelch function, which turns off the data outputs when the input signal is below the programmed threshold.

Applications

622Mbps LAN/ATM LAN Receivers

155Mbps LAN/ATM LAN Receivers

Features

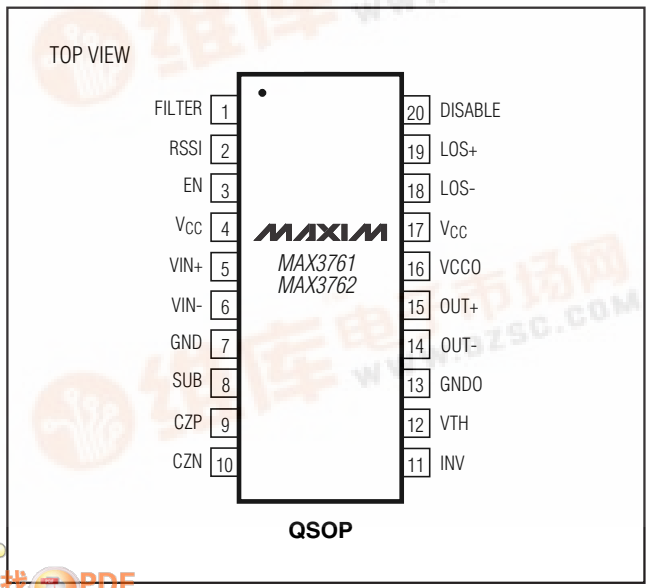
- ♦ **Chatter-Free Power Detector with Programmable Loss-of-Signal Outputs**
- ♦ **4mV Input Sensitivity (PECL Loss-of-Signal Interface Logic—MAX3766**
- ♦ **PECL Data Outputs**
- ♦ **Single 5V Power Supply**
- ♦ **250ps Output Edge Speed**
- ♦ **Low 15ps Pulse-Width Distortion**
- ♦ **TTL Loss-of-Signal Interface Logic—MAX3761**

Ordering Information

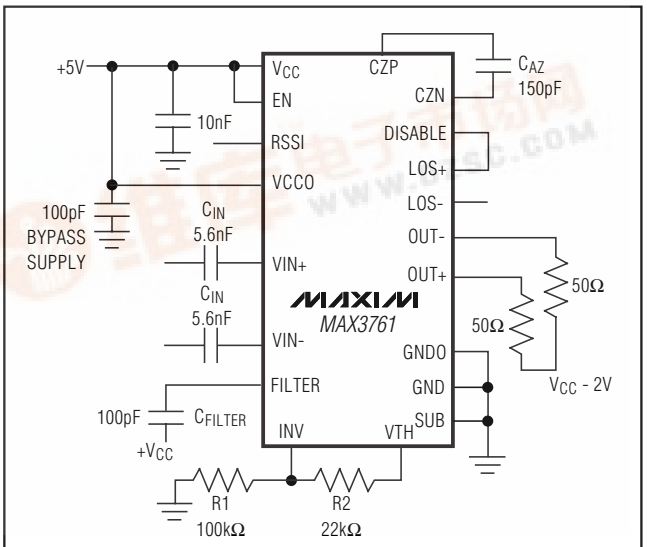
PART	TEMP RANGE	PIN-PACKAGE
MAX3761EEP	-40°C to +85°C	20 QSOP
MAX3761C/D	-40°C to +85°C	Dice*
MAX3762EEP	-40°C to +85°C	20 QSOP
MAX3762EEP+	-40°C to +85°C	20 QSOP
MAX3762C/D	-40°C to +85°C	Dice*

**Dice are designed to operate from -40°C to +85°C, but are tested and guaranteed only at T_A = +25°C.*
+Denotes lead free package.

Pin Configuration



Typical Operating Circuits



MAX3762 at end of data sheet.

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

ABSOLUTE MAXIMUM RATINGS

V_{CC}, VCCO.....-0.5V to +7.0V
FILTER, RSSI, EN, VIN+, VIN-, CZP, CZN,
DISABLE, LOS+, LOS-, INV, VTH.....-0.5V to (V_{CC} + 0.5V)
PECL Output Current (OUT+, OUT-, LOS+, LOS-) 50mA
Continuous Power Dissipation (T_A = +85°C)
QSOP (derate 9.1mW/ºC above +85°C).....591mW
Operating Junction Temperature Range.....-40°C to +150°C
Processing Temperature (die).....+400°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, DISABLE = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Current	MAX3761, I_{VCC}			25	37	mA
	MAX3762, I_{VCC}			30	46	
LOS Output TTL High	MAX3761		2.8			V
LOS Output TTL Low	MAX3761	(T_A = +25°C to +85°C)			0.40	V
		(T_A = -40°C to +25°C)			0.44	
LOS Output PECL High	MAX3762 (Notes 2, 3)		-1150		-880	mV
LOS Output PECL Low	MAX3762 (Notes 2, 3)		-1830		-1555	mV
DISABLE Input Current	Logic high				100	µA
DISABLE Input High	MAX3761		2.65			V
DISABLE Input Low	MAX3761				0.8	V
DISABLE Input PECL High	MAX3762 (Note 3)		-1160			mV
DISABLE Input PECL Low	MAX3762 (Note 3)				-1470	mV
PECL Data Output Voltage High (V_{OH})	(Notes 2, 3)		-1150		-880	mV
PECL Data Output Voltage Low (V_{OL})	(Notes 2, 3)		-1830		-1555	mV
Disabled Differential Output	DISABLE = high		-100		100	mV
Disabled Common-Mode Output	DISABLE = high		V_{CC} - 0.7		V_{CC} -1.2	V

Note 1: Dice are tested at T_A = +25°C.
Note 2: Outputs terminated with 50Ω to V_{CC} - 2V.
Note 3: Voltage measurements are relative to V_{CC}.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input 4mV to 2Vp-p, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V, T_A = +25°C.) (Note 5)

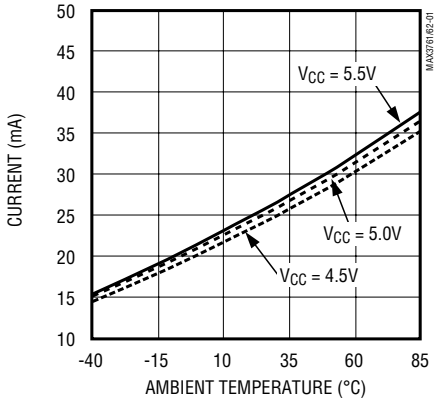
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum LOS Assert Input	T_A = -40°C, 2^{23} - 1 PRBS			3.2	mV
Data-Output Edge Speed	20% to 80%			250	ps
Data-Output Overshoot	(Note 6)			20	%
Pulse-Width Distortion	(Notes 6, 7)		15	80	ps
Input Resistance	Differential		3900		Ω
LOS Hysteresis	2^{23} - 1 PRBS, VTH = 1.8V		3.5		dB

Note 5: AC parameters are guaranteed by design and characterization.
Note 6: Input signal is a 1-0 pattern, 622Mbps.
Note 7: PWD = [(width of wider pulse) - (width of narrower pulse)] / 2.

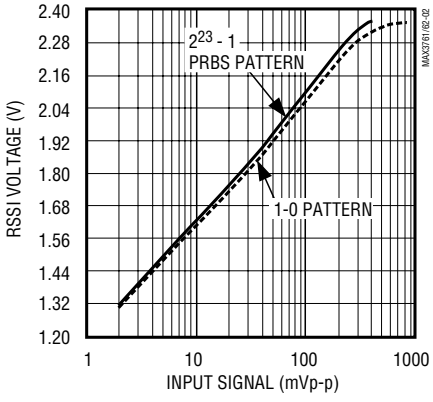
Typical Operating Characteristics

(MAX3761/MAX3762 EV kit, V_{CC} = +5.0V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input is a 1-0 pattern, 622Mbps, T_A = +25°C, unless otherwise noted.)

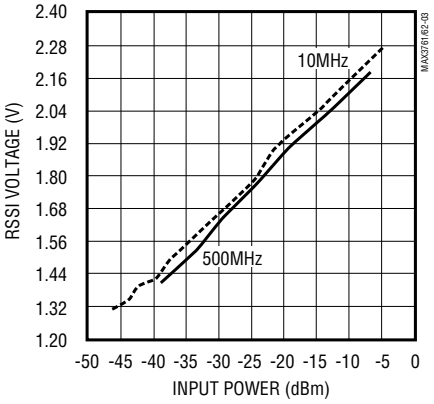
MAX3762
SUPPLY CURRENT vs. TEMPERATURE



RSSI vs. INPUT AMPLITUDE AND DATA PATTERN



RSSI vs. INPUT POWER AND FREQUENCY

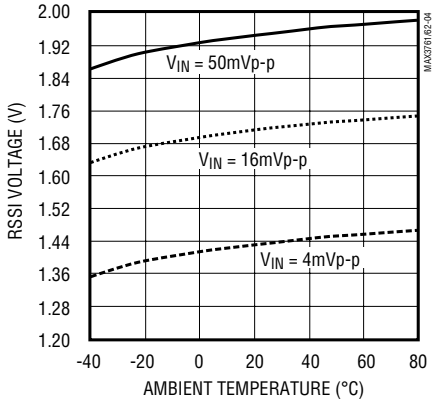


Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

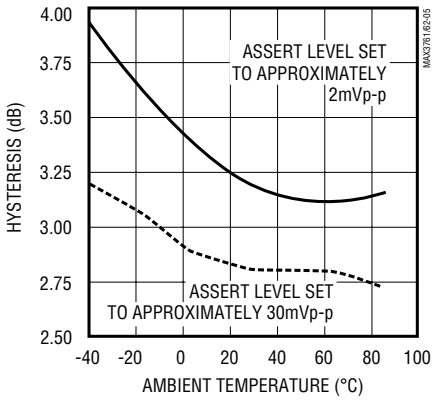
Typical Operating Characteristics (continued)

(MAX3761/MAX3762 EV kit, V_{CC} = +5.0V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input is a 1-0 pattern, 622Mbps, T_A = +25°C, unless otherwise noted.)

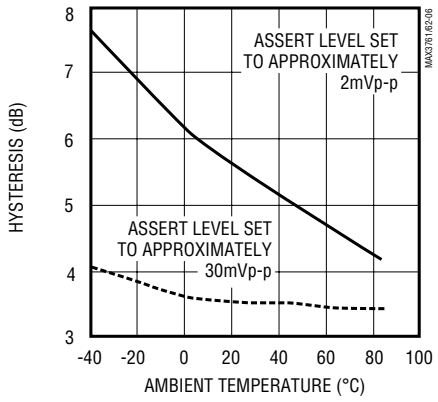
RSSI vs. TEMPERATURE (622Mbps 2^{23} - 1 PRBS)



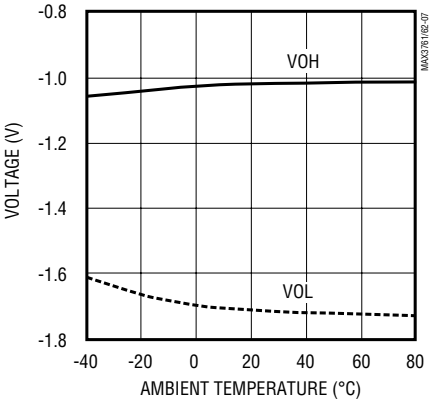
LOS HYSTERESIS vs. TEMPERATURE (622Mbps 2^{23} - 1 PRBS PATTERN)



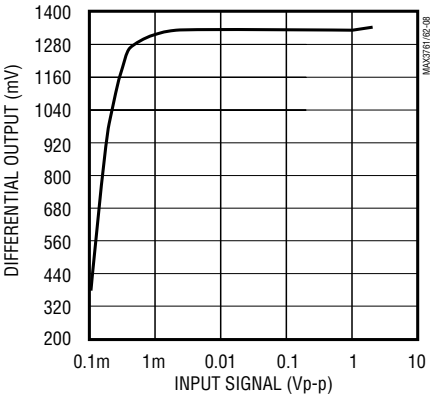
LOS HYSTERESIS vs. TEMPERATURE (622Mbps 1-0 PATTERN)



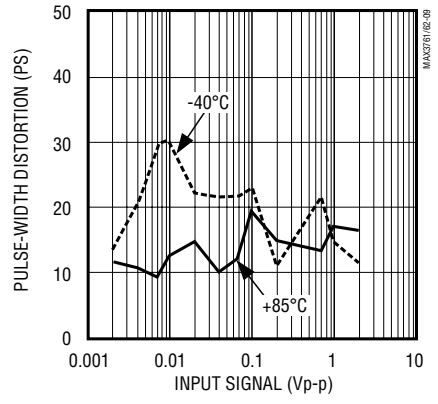
DATA OUTPUT LEVELS (REFERENCE TO V_{CC})



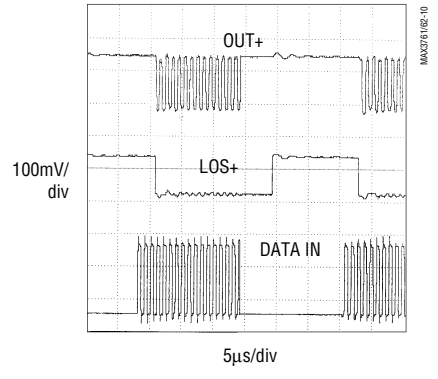
DIFFERENTIAL OUTPUT vs. INPUT AMPLITUDE



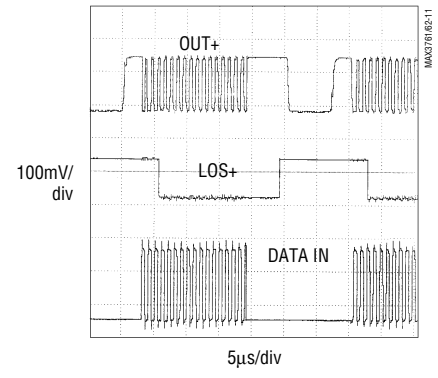
PULSE-WIDTH DISTORTION (622Mbps DATA RATE)



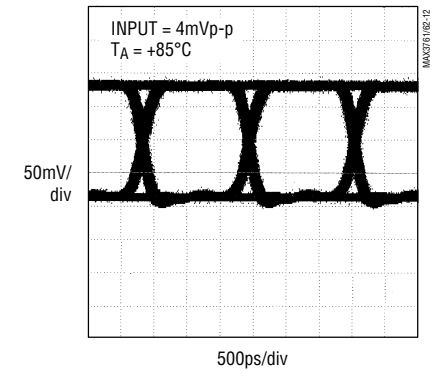
LOS OPERATION WITH SQUELCHING



LOS OPERATION WITHOUT SQUELCHING



DATA OUTPUT SINGLE-ENDED (2^{23} - 1 PRBS PATTERN)

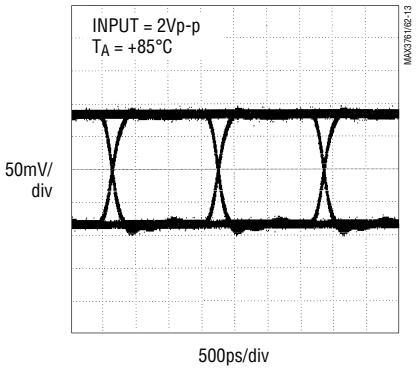


Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

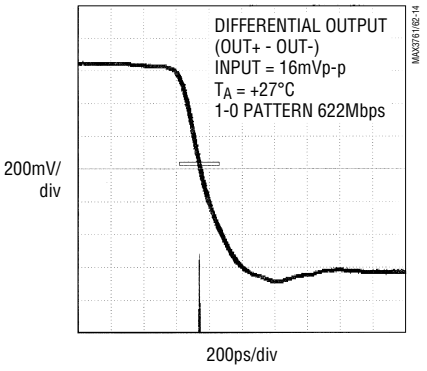
Typical Operating Characteristics (continued)

(MAX3761/MAX3762 EV kit, V_{CC} = +5.0V, PECL outputs terminated with 50Ω to V_{CC} - 2V, input is a 1-0 pattern, 622Mbps, T_A = +25°C, unless otherwise noted.)

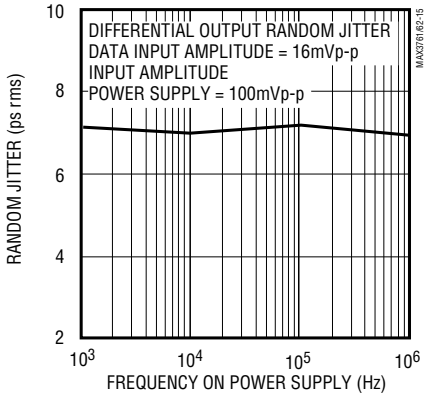
DATA OUTPUT SINGLE-ENDED (2^{23}-1 PRBS PATTERN)



RANDOM JITTER



RANDOM JITTER vs. POWER-SUPPLY NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	FILTER	Sets the integration frequency of the power detector. Impedance at this node is approximately 500Ω.
2	RSSI	Received-Signal-Strength Indicator. An analog DC voltage representing the input power.
3	EN	Connect to V_{CC}.
4, 17	V_{CC}	+5V Power Supply
5	VIN+	Positive Input Data
6	VIN-	Negative Input Data
7	GND	Supply Ground
8	SUB	Substrate. Connect to ground.
9	CZP	Sets input offset correction, low-frequency cutoff.
10	CZN	Sets input offset correction, low-frequency cutoff.
11	INV	Negative Input to Op Amp. Used for programming the loss-of-signal threshold.
12	VTH	Loss-of-Signal Threshold Voltage
13	GNDO	Ground Power Supply for Output Buffers
14	OUT-	Negative PECL Data Output
15	OUT+	Positive PECL Data Output
16	VCCO	+5V Power Supply for Output Buffers
18	LOS-	Negative Loss-of-Power Flag, TTL (MAX3761) or PECL (MAX3762)
19	LOS+	Positive Loss-of-Power Flag, TTL (MAX3761) or PECL (MAX3762)
20	DISABLE	Disables the data outputs when high. TTL (MAX3761) or PECL (MAX3762).

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

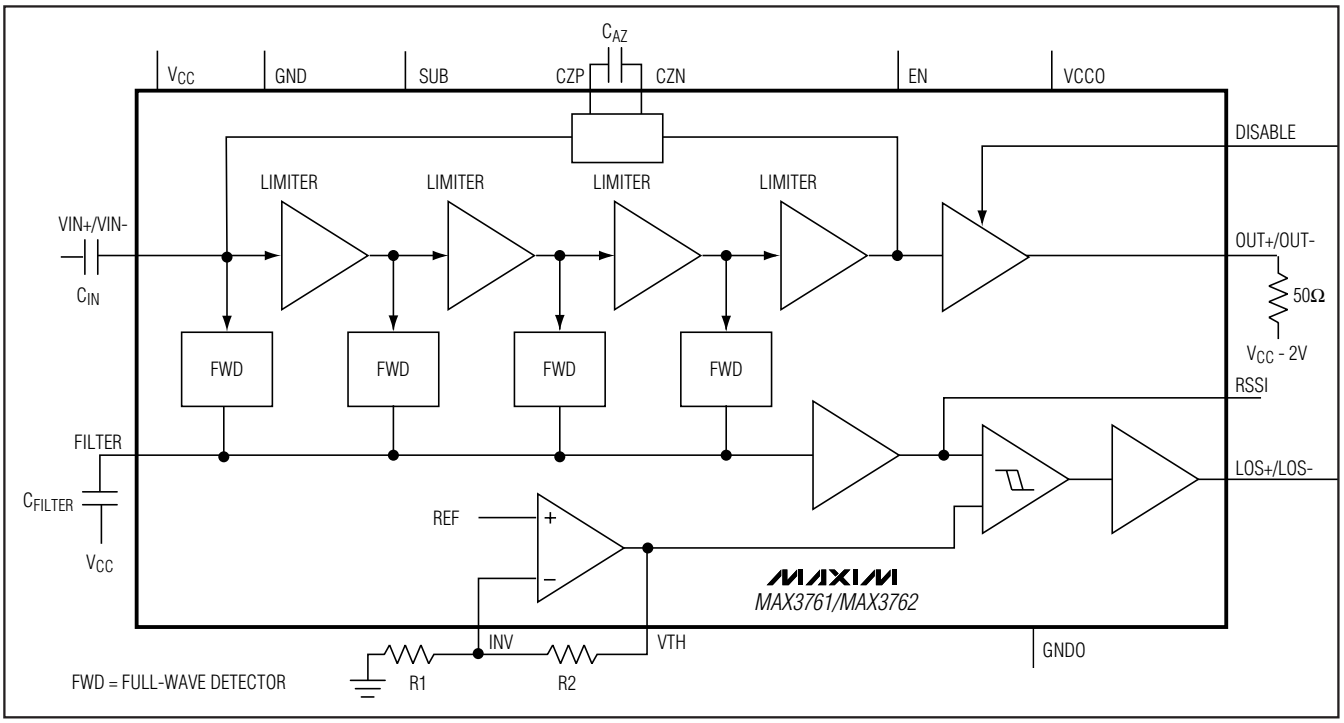


Figure 1. Functional Diagram

Detailed Description

Figure 1 shows the functional diagram for the MAX3761/MAX3762. The input signal is applied to VIN+ and VIN-. A chain of amplifier stages, each contributing approximately 12.5dB of gain, amplifies the input signal to PECL output voltage swings. A 4mVp-p input signal will cause the output to fully limit.

Received-Signal-Strength Indicator (RSSI)

Each amplifier stage contains a full-wave logarithmic detector (FWD). The full-wave detector outputs are summed at the FILTER pin and used to generate the received-signal-strength indication (RSSI). The RSSI output voltage is linearly proportional to the input power (in decibels), and is approximated by:

$$V_{RSSI}(V) = 1.13 + 0.457\log(V_{IN})$$

where V_{IN} is the peak-to-peak input signal in millivolts.

The RSSI output is insensitive to fluctuations in temperature and supply voltage. The power detector functions as a broadband power meter that detects the total power of all signals present in the passband of approximately 750MHz. Refer to the *Typical Operating Characteristics* graphs showing RSSI output versus input power and signal amplitude.

The high-speed RSSI signal is filtered with one external capacitor connected from FILTER to V_{CC}. The impedance at the FILTER pin is approximately 500Ω.

The FILTER capacitor (C_{FILTER}) must be connected to V_{CC} for proper operation.

Input-Offset Correction

The limiting amplifier provides approximately 60dB of gain. An input DC offset of even 1mV reduces the power-detection circuit's accuracy and can cause the output to limit. A low-frequency feedback loop is integrated into the MAX3761/MAX3762 to remove input offset. DC coupling the inputs is not recommended, as this prevents the DC-offset-correction circuitry from functioning properly. Input offset is typically reduced to less than 100µV.

The capacitance between pins CZP and CZN, in parallel with a 10pF integrated capacitance, determines the offset-correction circuit's time constant. The input impedance between CZP and CZN is approximately 800kΩ.

The offset correction circuitry requires an average data-input duty cycle of 50%. If the input data has a different average duty cycle, the output will have increased pulse-width distortion.

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

Loss-of-Signal Indicator

The MAX3761/MAX3762 includes a loss-of-signal monitor with a programmable assert threshold and a hysteresis comparator. Internally, one comparator input is tied to the RSSI output signal and the other is tied to the threshold-voltage (VTH) pin, which provides a threshold for the LOS indication. An op amp referenced to an internal bandgap voltage (1.18V) is supplied for programming a supply-independent threshold voltage. Only two external resistors are needed to program the LOS assert level. VTH is programmable from 1.18V to 2.4V, providing adequate coverage of the RSSI output's useful range. The op amp runs on very low supply current and provides an accurate, temperature-stable threshold, but can source only 20µA of current. For proper operation, resistor R1 (see the *Typical Operating Circuit*) should have a value ≥ 100kΩ. The input bias current at INV is < 50nA.

To ensure chatter-free LOS operation, the internal LOS comparator contains approximately 90mV of hysteresis. The RSSI signal output has a slope of 25mV/dB. Therefore, the overall circuit hysteresis is approximately 3.6dB[90mV / (25mV/dB)]. The LOS assert threshold is 45mV below V_{TH}, while the LOS deassert threshold is 45mV above V_{TH}.

Output Buffers

The DISABLE pin can be used to disable the data-output buffer. When DISABLE is high, the differential output signal at OUT+ and OUT- is approximately zero. In the disabled state, the common-mode voltage of each output is approximately V_{CC} - 0.8V. Connecting DISABLE to LOS+ implements a squelch function. When using the squelch function, the output signal is disabled whenever the input signal is too small to be reliably detected (as determined by the voltage at VTH). Use of the disable function is recommended at all times.

The data outputs (OUT+ and OUT-) are implemented with emitter followers that have output impedance of approximately 2Ω. The MAX3762's PECL LOS outputs also are implemented with emitter followers that have output impedance of approximately 2Ω.

The MAX3761 TTL LOS output buffers are open-collector transistors with 6kΩ internal pull-up resistors.

Design Procedure

Supply Voltage

The MAX3761/MAX3762 can be operated with a single +5V or -5V power supply.

Programming the LOS Assert Level

First determine the receiver system's sensitivity in dBm either by estimating or from prototyping results. Estimate the total gain of the preamplifier and photodiode, then use Figure 3 to select resistor R2, placing the LOS assert 3dB to 4dB below the receiver sensitivity.

Alternatively, use the *Typical Operating Characteristics* to select the V_{TH} value needed for LOS assert, then program V_{TH} with the following relation:

$$V_{TH} = 1.18(1 + R2 / R1)$$

Select R1 ≥ 100kΩ.

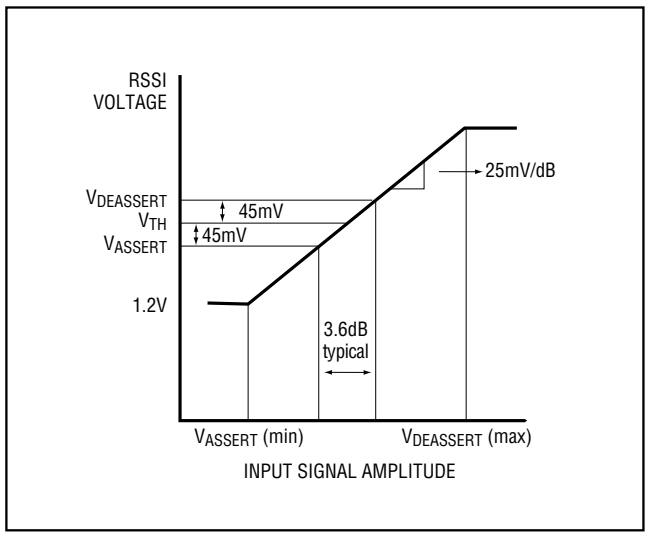


Figure 2. Loss-of-Signal Definitions

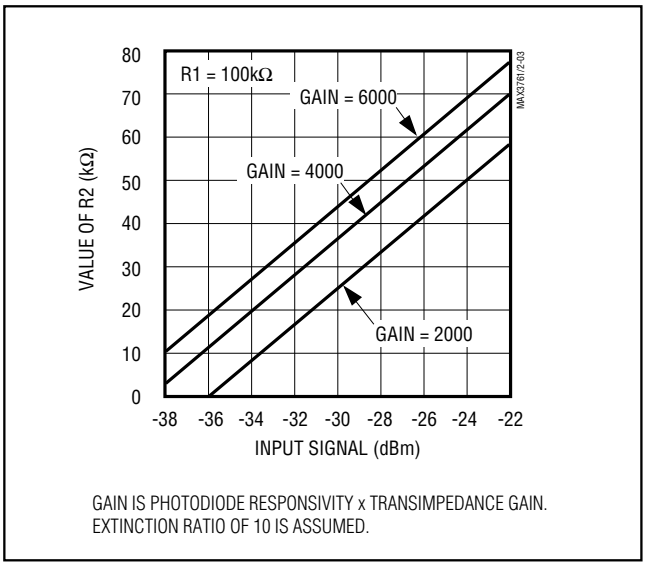


Figure 3. Using TIA Gain and Photodiode Responsivity to Select LOS Programming Resistor

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

Capacitor Selection

A typical MAX3761/MAX3762 implementation requires four external capacitors. To select the capacitors, first determine the following parameters in the receiver system (see the *Applications Information* section for recommendations in 622Mbps ATM and Fibre Channel 1063Mbps systems):

1) The duration of the expected longest run of consecutive bits in the data stream. For example, 72 consecutive zeros in a 622Mbps data stream have a duration of 116ns.
2) The maximum allowable data-dependent jitter.
3) The desired power-detector integration time constant [$1/(2\pi f_{INT})$].
4) The transimpedance amplifier's maximum peak-to-peak output voltage.

Step 1. Select the Input AC-Coupling Capacitors (C_{IN}). When using a limiting preamplifier with a highpass frequency response, select C_{IN} to provide a low-frequency cutoff (f_C) one decade lower than the preamplifier low-frequency cutoff. This causes nearly all data-dependent jitter (DDJ) to be generated in the preamplifer circuit. For example, if the preamplifier's low-frequency cutoff is 150kHz, then select C_{IN} to provide a 15kHz low-frequency cutoff.

Select C_{IN} with the following equation:

$$C_{IN} = \frac{1}{2\pi f_C 1950\Omega}$$

For differential input signals, use a capacitor equal to C_{IN} on both inputs (VIN+ and VIN-). For single-ended input signals, one capacitor should be tied to VIN+ and another should decouple VIN- to ground.

When using a preamplifier without a highpass response, select C_{IN} to ensure that data-dependent jitter is acceptable. The following equation provides an estimate for C_{IN}:

$$C_{IN} \geq \frac{-t_L}{1950 \ln\left[1 - \frac{(DDJ)(BW)}{0.5}\right]}$$

where: t_L = duration of the longest run of consecutive bits with the same value (seconds); DDJ = maximum allowable data-dependent jitter, peak-to-peak (seconds); BW = typical system bandwidth, normally 0.6 to 1.0 times the data rate (hertz).

Regardless of which method is used to select C_{IN}, the maximum LOS assert time can be estimated from the value of C_{IN}. The following equation estimates LOS time delay when the maximum-amplitude signal is instantaneously removed from the input, and when the FILTER time constant is much faster than the input time constant ($C_{FILTER} < 0.4C_{IN}$):

$$t_{LOS\ ASSERT} = 1950 C_{IN} \ln(V_{MAXp\text{-}p} / V_{ASSERTp\text{-}p})$$

where $V_{MAXp\text{-}p}$ is the maximum output of the preamplifier, and $V_{ASSERTp\text{-}p}$ is the input amplitude that causes LOS to assert. The equation describes the input capacitors' discharge time, from maximum input to the LOS threshold into the 1950Ω, single-ended input resistance.

Step 2. Select the Offset-Correction Capacitor (C_{AZ}). To maintain stability, it is important to keep a one-decade separation between f_C and the low-frequency cutoff associated with the DC-offset-correction circuit (f_{OC}).

The input impedance between CZP and CZN is approximately 800kΩ in parallel with 10pF. As a result, the low-frequency cutoff (f_{OC}) associated with the DC-offset-correction loop is computed as follows:

$$f_{OC} = \frac{1}{2\pi 800k\Omega\left(C_{AZ} + 10pF\right)}$$

where C_{AZ} is an optional external capacitor between CZP and CZN.

If C_{IN} is known, then:

$$C_{AZ} \geq \frac{C_{IN}}{41} - 10pF$$

Step 3. Select the Power-Detect Integration Capacitor (C_{FILTER}). For 622Mbps ATM applications, Maxim recommends a filter frequency of 3MHz, which requires C_{FILTER} = 100pF. The integration frequency can be selected lower to remove low-frequency noise, or to prevent unusual data sequences from asserting LOS.

$$C_{FILTER} = 1 / (2\pi 500 f_{INT})$$

where f_{INT} is the integration frequency.

Applications Information

Converting Average Optical Power to Signal Amplitude

Many of the MAX3761/MAX3762's specifications relate to input-signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. The relations given in Table 1 are helpful for converting optical power to input signal when designing with the MAX3761/MAX3762.

Table 1. Optical-Power Relations*

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P0 + P1)/2$
Extinction Ratio	r_e	$r_e = P1 / P0$
Optical Power of a "1"	P1	$P1 = 2P_{AVE}\frac{r_e}{r_e + 1}$
Optical Power of a "0"	P0	$P0 = 2P_{AVE}/(r_e + 1)$
Signal Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVE}\frac{(r_e - 1)}{r_e + 1}$

* Assuming a 50% average input data duty cycle (true for SONET/ATM data).

In an optical receiver, the input voltage to the limiting amplifier can be found by multiplying the relationship in Table 1 with the photodiode responsivity (ρ) and transimpedance amplifier gain (G).

Optical Hysteresis

Power and hysteresis are often expressed in decibels. By definition, decibels are always 10log (power). At the inputs to the MAX3761/MAX3762 limiting amplifier, the power is V_{IN}^2/R. If a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage input to the MAX3761/MAX3762 also increases by a factor of two.

The optical power change is 10log(2x/x) = 10log(2) = +3dB

At the MAX3761/MAX3762, the voltage change is:

$$10\log\frac{(2V_{IN})^2/R}{V_{IN}^2/R} = 10\log(2^2) = 20\log(2) = +6dB$$

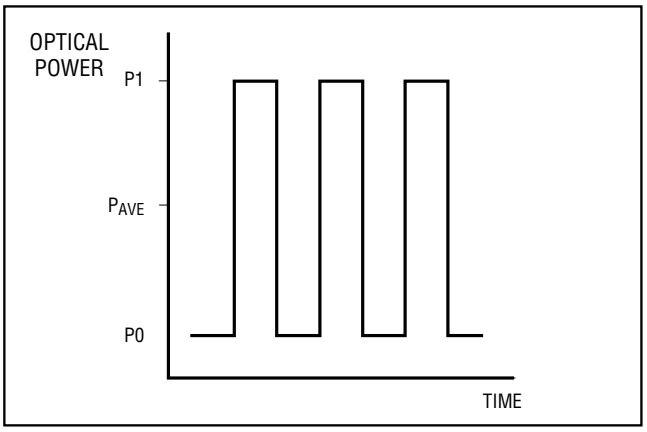


Figure 4. Optical-Power Relations

In an optical receiver the dB change at the MAX3761/MAX3762 will always equal 2x the optical dB change.

The MAX3761/MAX3762's typical voltage hysteresis is 3.6dB. This provides an optical hysteresis of 1.8dB.

Input Sensitivity

The receiver's gain sensitivity defines the smallest signal input that results in fully limited PECL-compatible data outputs. Smaller signals result in nonlimited outputs. The MAX3761/MAX3762's input sensitivity (S_{GAIN}) is 4mVp-p:

$$S_{GAIN} = 4mV$$

Optical gain sensitivity (in dBm) is:

$$10\log\left[\frac{S_{GAIN}}{2G\rho} \times \frac{r_e + 1}{r_e - 1} \times 1000\right]$$

In a receiver with G = 6kΩ, r_e = 10, and ρ = 0.8A/W, gain sensitivity is 510nW, or -32.9dBm.

622Mbps ATM Component Selection

As an example, a preamplifier with a 150kHz low-frequency cutoff and a 950mVp-p maximum output has the best performance with the following selections:

C_{IN} = 5.6nF, so that f_C = 15kHz (one decade below the 150kHz cutoff)

C_{AZ} = 150pF, so that f_{OC} < 1.5kHz (one decade below f_C)

C_{FILTER} = 100pF, so that the integration frequency equals 3MHz.

These selections should provide data-dependent jitter less than 110ps p-p when the input consists of PRBS data with no more than 72 consecutive bits.

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

For LOS assert at -35dBm, select R1 = 100kΩ and R2 = 22kΩ, which programs the LOS assert at input ≅ 3mV. With this selection, LOS assert time will typically be less than 85µs.

Fibre Channel Component Selection

In Fibre Channel applications, the desired LOS assert time is typically 25µs maximum, and data-dependent jitter is reduced by 8B10B coding techniques. The following are recommended in a Fibre Channel system where preamp gain is 2000V/W, LOS assert is set for -24dBm (13mV MAX3761/MAX3762 input), and the maximum input to the MAX3761/MAX3762 is 1Vp-p:

C_{IN} = 3.3nF (to provide LOS assert in 25µs)

C_{AZ} = 82pF (to provide f_{OC} = 1/10 f_C for stability)

C_{FILTER} = 100pF (for a 3MHz integration constant)

R1 = 100kΩ, R2 = 50kΩ (to set LOS assert at -24dBm)

PECL Terminations

The standard PECL termination (50Ω to V_{CC} - 2V) is recommended for best performance and output characteristics. The data outputs operate at high speed, and should always drive transmission lines with 50Ω to 75Ω terminations. Balanced termination is recommended for all outputs.

Figure 5 shows an alternative method for terminating the data outputs. The technique provides approximately 8mA DC bias current, with a 50Ω AC load, for the output termination. This technique is useful for viewing the output on an oscilloscope or changing the PECL reference voltage.

The MAX3762's PECL LOS outputs are relatively slow and do not need 50Ω terminations (although they are capable of driving them). To reduce power, the MAX3762's LOS outputs can be terminated with 500Ω. Figure 6 shows a typical operating circuit for the MAX3762.

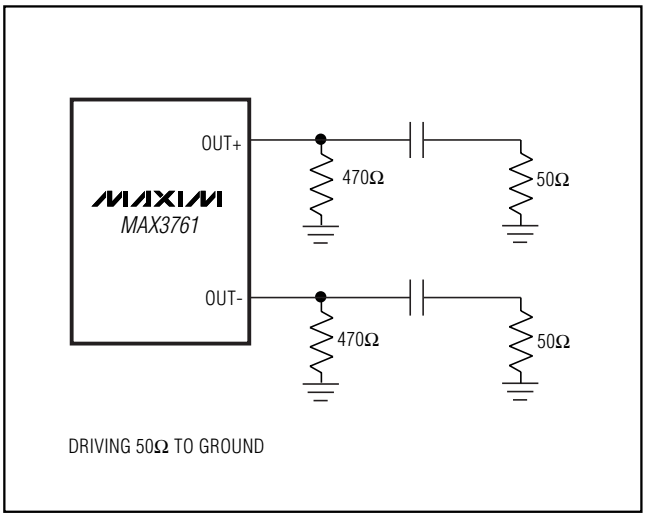


Figure 5. Alternative PECL Termination

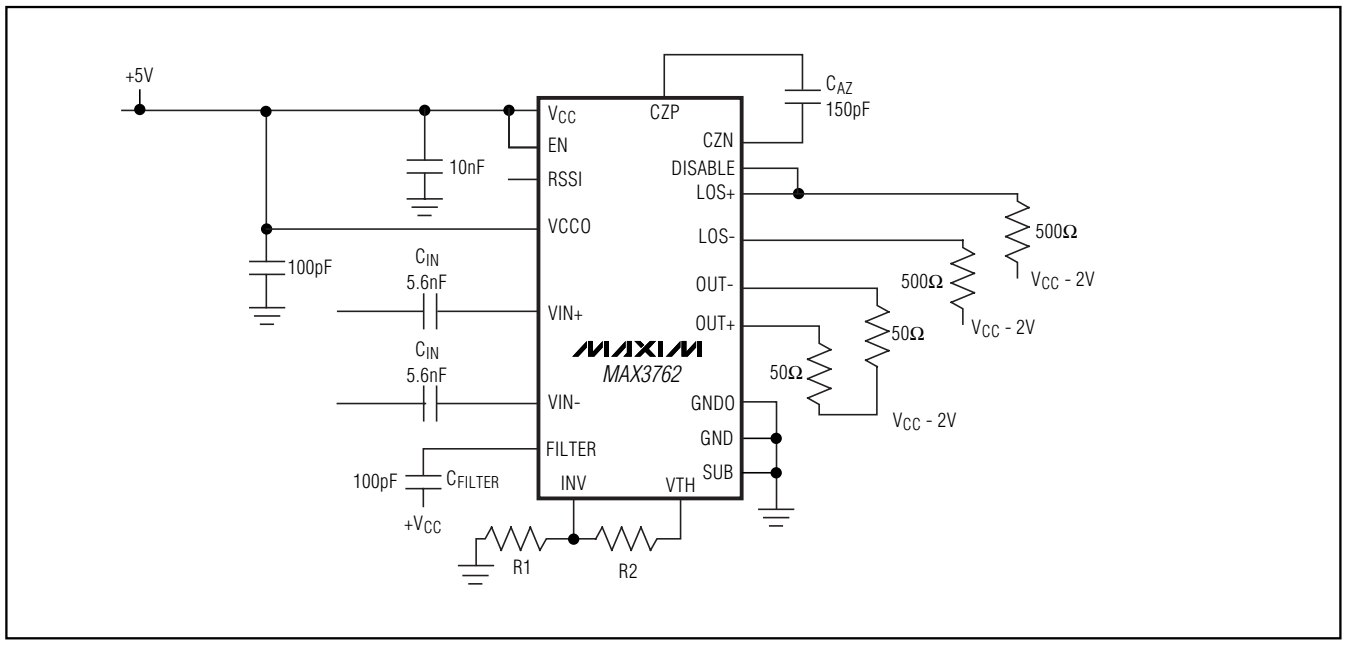
Wire Bonding

For high current density and reliable operation, the MAX3761/MAX3762 use gold metalization. Make connections to the dice with gold wire only, and use ball-bonding techniques (wedge bonding is not recommended). Die-pad size is 4 mils square, with a 6 mil pitch. Die thickness is 12 mils (0.3mm).

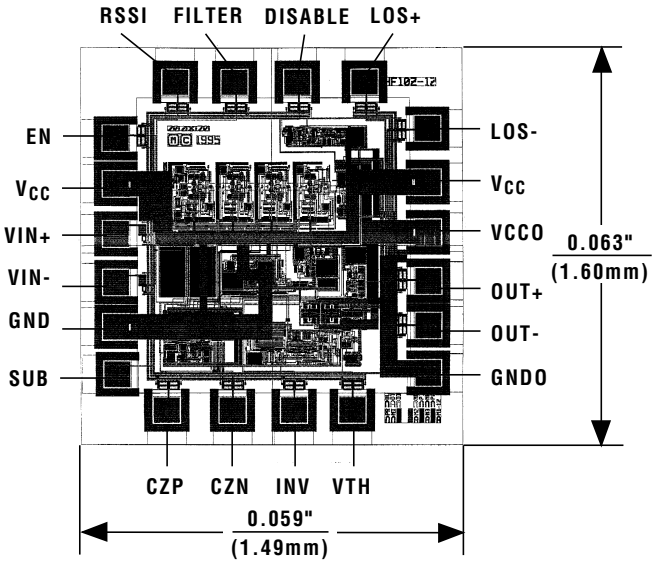
Layout Techniques

The MAX3761/MAX3762 are high-frequency, high-bandwidth circuits. To ensure stability, use good high-frequency layout techniques. Filter voltage supplies, and keep ground connections short. Use multiple vias where possible. Use controlled-impedance transmission lines to connect the MAX3761/MAX3762 data outputs to other circuits.

Typical Operating Circuits (continued)



Chip Topography



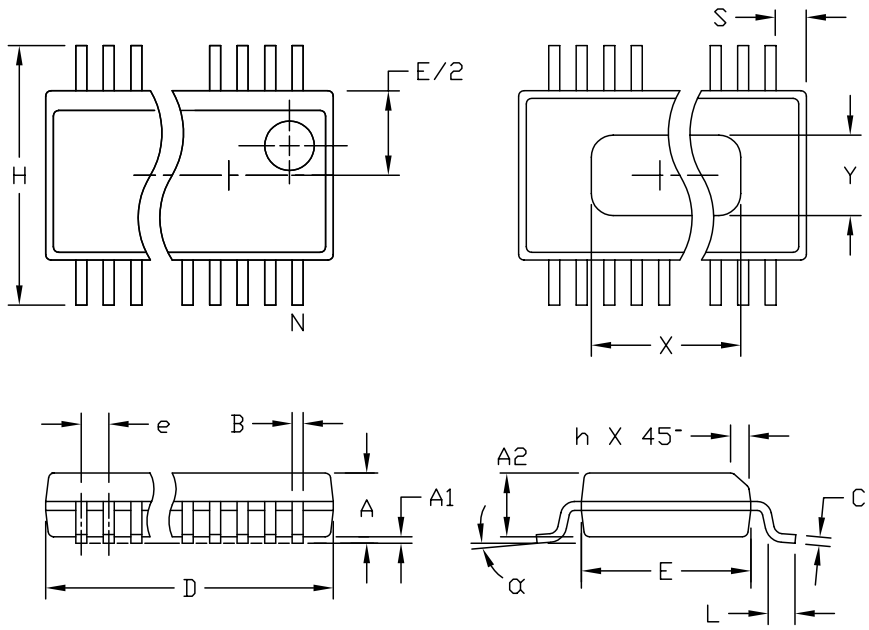
TRANSISTOR COUNT: 961
SUBSTRATE CONNECTED TO SUB

Low-Power, 622Mbps Limiting Amplifiers with Chatter-Free Power Detect for LANs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1