19-2935; Rev 0; 7/03

MAXIM

10Gbps EAM Driver with Integrated Bias Network

General Description

The MAX3941 is designed to drive an electro-absorption modulator (EAM) at data rates up to 10.7Gbps. It incorporates the functions of a biasing circuit and a modulation circuit, with integrated control op amps externally programmed by DC voltages.

The integrated bias circuit provides a programmable biasing current up to 50mA. This bias current reflects a bias voltage of up to 1.25V on an external 50Ω load. The bias and modulation circuits are internally connected on chip, eliminating the need for an external bias inductor.

A high-bandwidth, fully differential signal path is internally implemented to minimize jitter accumulation. When a clock signal is available, the integrated data-retiming function can be selected to reject input-signal jitter.

The MAX3941 receives differential CML signals (ground referenced) with on-chip line terminations of 50Ω. The output has a 50Ω resistor for back termination and is able to deliver a modulation current of 40mA$_{P-P}$ to 120mA$_{P-P}$, with an edge speed of 23ps (20% to 80% typ). This modulation current reflects an EAM modulation voltage of 1.0V$_{P-P}$ to 3.0V$_{P-P}$.

The MAX3941 also includes an adjustable pulse-width control circuit to precompensate for asymmetrical EAM characteristics. It is available in a compact 4mm x 4mm, 24-pin thin QFN package and operates over the -40°C to +85°C temperature range.

Features

- ♦ On-Chip Bias Network
- ♦ 23ps Edge Speed
- ♦ Programmable Modulation Voltage Up to 3V$_{P-P}$
- ♦ Programmable EAM Biasing Voltage Up to 1.25V
- ♦ Selectable Data-Retiming Latch
- ♦ Up to 10.7Gbps Operation
- ♦ Integrated Modulation and Biasing Functions
- ♦ 50Ω On-Chip Input and Output Terminations
- ♦ Pulse-Width Adjustment
- ♦ Enable and Polarity Controls
- ♦ ESD Protection

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3941ETG	-40°C to +85°C	24-Thin QFN (4mm x 4mm)

Applications

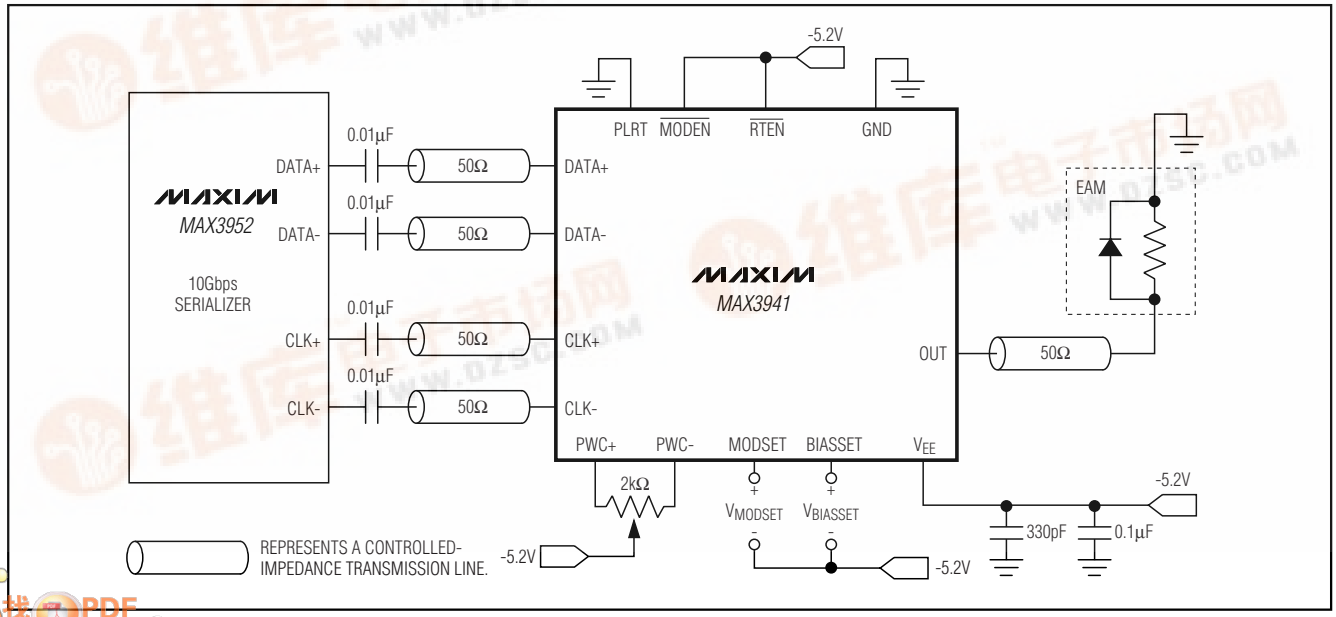
SONET OC-192 and SDH STM-64 Transmission Systems

DWDM Systems

Long/Short-Reach Optical Transmitters

10Gbps Ethernet

Typical Application Circuit



10Gbps EAM Driver with Integrated Bias Network

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{EE} .....-6.0V to +0.5V
Voltage at $\overline{MODEN}$, $\overline{RTEN}$, PLRT, MODSET, BIASSET .....(V_{EE} - 0.5V) to +0.5V
Voltage at DATA+, DATA-, CLK+, and CLK-.....-1.65V to +0.5V
Voltage at OUT .....-4V to +0.5V
Voltage at PWC+, PWC- .....(V_{EE} - 0.5V) to (V_{EE} + 1.7V)
Current Into or Out of OUT.....80mA
Continuous Power Dissipation (T_A = +85°C)
24-Lead Thin QFN
(derate 20.8mW/°C above +85°C).....1354mW
Storage Temperature Range .....-55°C to +150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.5V to -4.9V, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, I_{BIAS} = 30mA, I_{MOD} = 100mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{EE}			-5.5		-4.9	V
Supply Current	I_{EE}	Excluding I_{BIAS} and I_{MOD} (Note 1)	Retime disabled		124	174	mA
			Retime enabled		140	201	
Power-Supply Noise Rejection	PSNR	f ≤ 2MHz (Note 2)			15		dB
SIGNAL INPUT (Note 3)							
Input Data Rates		NRZ			10.7		Gbps
Single-Ended Input Resistance	R_{IN}	Input to GND		42.5	50	58.5	Ω
Single-Ended Input Voltage	V_{IS}	DC-coupled, Figure 1a		-1		0	V
		AC-coupled, Figure 1b		-0.4		+0.4	
Differential Input Voltage	V_{ID}	DC-coupled (Note 4)		0.2		2.0	V_{P-P}
		AC-coupled (Note 4)		0.2		1.6	
Differential Input Return Loss	RL_{IN}	≤15GHz			15		dB
EAM BIAS							
Maximum Bias Current		$V_{BIASSET}$ = V_{EE} + 2V		50	56		mA
Minimum Bias Current		$V_{BIASSET}$ = V_{EE}			0.3	1.2	mA
BIASSET Voltage Range	$V_{BIASSET}$			V_{EE}		V_{EE} + 2	V
Equivalent Bias Resistance	R_{BSEQV}	(Note 5)			36.4		Ω
Bias-Current-Setting Accuracy		T_A = +25°C	$V_{BIASSET}$ = V_{EE} + 0.11V	2.1		4.3	mA
			$V_{BIASSET}$ = V_{EE} + 0.36V	8.8		11.3	
			$V_{BIASSET}$ = V_{EE} + 2.0V	52		58.4	
Bias-Current Temperature Stability		(Note 6)	$V_{BIASSET}$ < V_{EE} + 0.36V	-1100		+1100	ppm/°C
			$V_{BIASSET}$ ≥ V_{EE} + 0.36V	-480		+480	
BIASSET Input Resistance					20		kΩ
BIASSET Bandwidth		50Ω driver load, $V_{BIASSET}$ = V_{EE} + 0.55V, Figure 2			5		MHz
EAM MODULATION							
Maximum Modulation Current				112	120		mA_{P-P}
Minimum Modulation Current		V_{MODSET} = V_{EE}			37	40	mA_{P-P}
MODSET Voltage Range	V_{MODSET}			V_{EE}		V_{EE} + 1	V
Equivalent Modulation Resistance	R_{MODEQV}	(Note 7)			11.1		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.5V to -4.9V, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, I_{BIAS} = 30mA, I_{MOD} = 100mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Modulation Set Bandwidth		Modulation depth 10%, 50Ω driver load, Figure 2		5		MHz
MODSET Input Resistance				20		kΩ
Modulation-Current Temperature Stability		(Note 6)	-957		0	ppm/°C
Modulation-Current-Setting Error		50Ω driver load, T_A = +25°C	-10		+10	%
Output Resistance	R_{OUT}	OUT to GND	42.5	50	58.5	Ω
Total Off Current		BIASSET = V_{EE}, $\overline{MODEN}$ = V_{EE}, MODSET = V_{EE}, DATA+ = high, DATA- = low			1.2	mA
Output Return Loss	RL_{OUT}	I_{BIAS} = 30mA, I_{MOD} = 50mA, ≤15GHz		10		dB
Output Edge Speed		20% to 80% (Notes 6, 8)		23	32	ps
Setup/Hold Time	t_{SU}, t_{HD}	Figure 3 (Note 6)	25			ps
Pulse-Width Adjustment Range		(Notes 6, 8)	±30	±50		ps
Pulse-Width Control Input Range (Single Ended)		For PWC+ and PWC-	V_{EE} + 0.5		V_{EE} + 1.5	V
Pulse-Width Control Input Range (Differential)		(PWC+) - (PWC-)	-0.5		+0.5	V
Output Overshoot	δ	(Notes 6, 8)		10		%
Driver Random Jitter	RJ_{DR}	(Note 6)		0.3	0.7	ps_{RMS}
Driver Deterministic Jitter	DJ_{DR}	PWC- = GND (Notes 6, 9)		6.8	11	ps_{P-P}
CONTROL INPUTS						
Input High Voltage	V_{IH}	(Note 10)	V_{EE} + 2.0			V
Input Low Voltage	V_{IL}	(Note 10)			V_{EE} + 0.8	V
Input Current		(Note 10)	-80		+200	µA

Note 1: Supply current remains elevated once the retiming function is enabled. Power must be cycled to reduce supply current after the retiming function is disabled.

Note 2: Power-supply noise rejection is specified as PSNR = 20log($V_{noise\ (on\ Vcc)}$ / ΔV_{OUT}). V_{OUT} is the voltage across a 50Ω load. $V_{noise\ (on\ Vcc)}$ = $100mV_{P-P}$.

Note 3: For DATA+, DATA-, CLK+, and CLK-.

Note 4: CLK input characterized at 10.7Gbps.

Note 5: R_{BSEQV} = ($V_{BIASSET}$ - V_{EE}) / I_{BIAS} with $\overline{MODEN}$ = V_{EE}, DATA+ = high, and DATA- = low.

Note 6: Guaranteed by design and characterization using the circuit shown in Figure 4.

Note 7: R_{MODEQV} = (V_{MODSET} - V_{EE}) / (I_{MOD} - 37mA) with BIASSET = V_{EE}.

Note 8: 50Ω load, characterized at 10.7Gbps with a 1111 1111 0000 0000 pattern.

Note 9: Deterministic jitter is defined as the arithmetic sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ). Measured with a 10.7Gbps 2^7 - 1 PRBS pattern with eighty 0s and eighty 1s inserted in the data pattern.

Note 10: For $\overline{MODEN}$ and PLRT.

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Test Circuits and Timing Diagrams

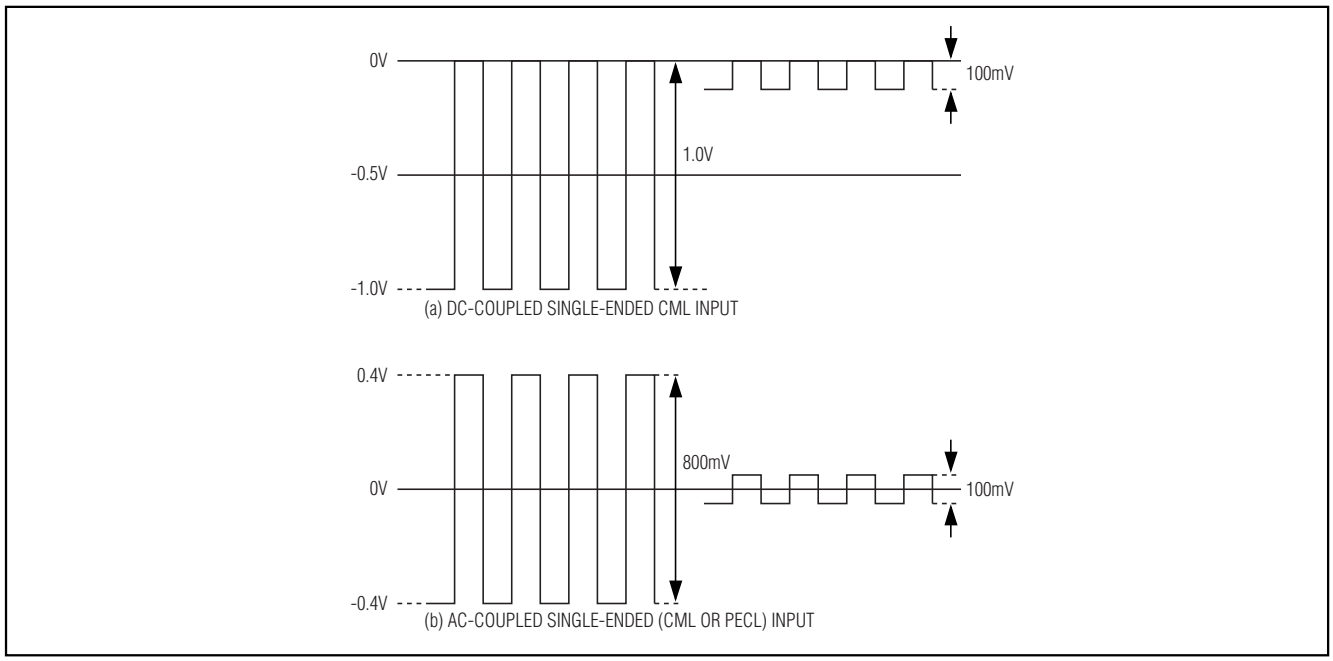

Figure 1. Definition of Single-Ended Input Voltage Range

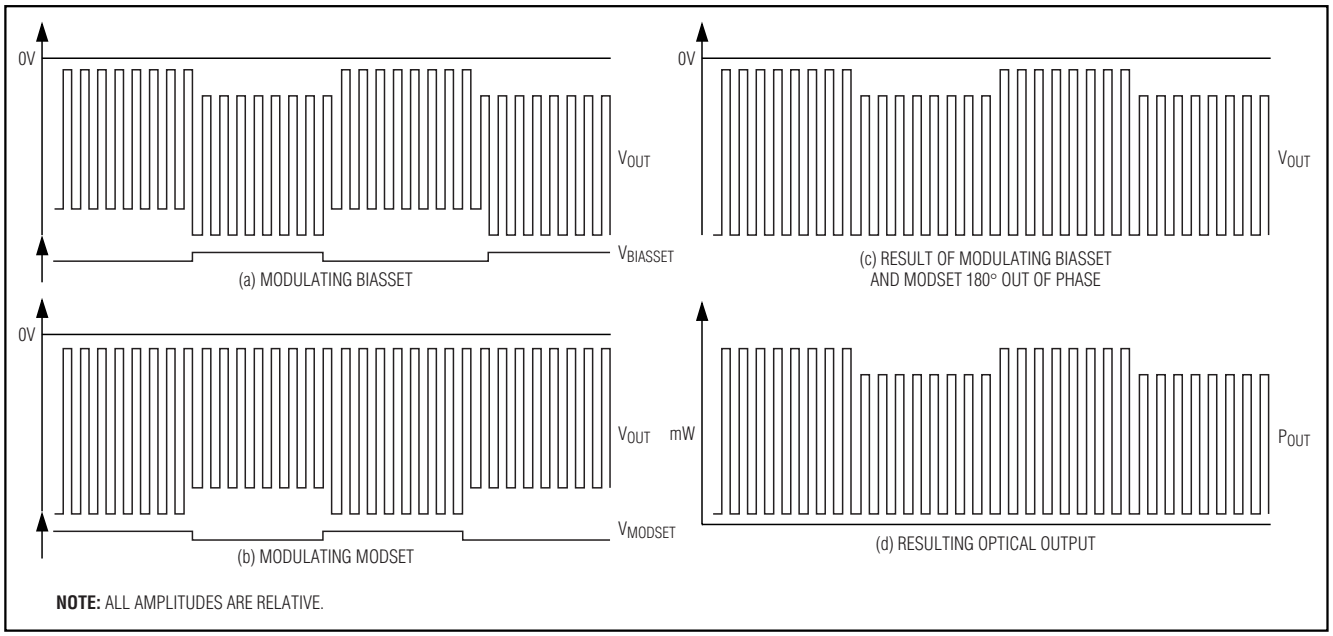

Figure 2. Modulating BIASSET and MODSET Pins

Test Circuits and Timing Diagrams (continued)

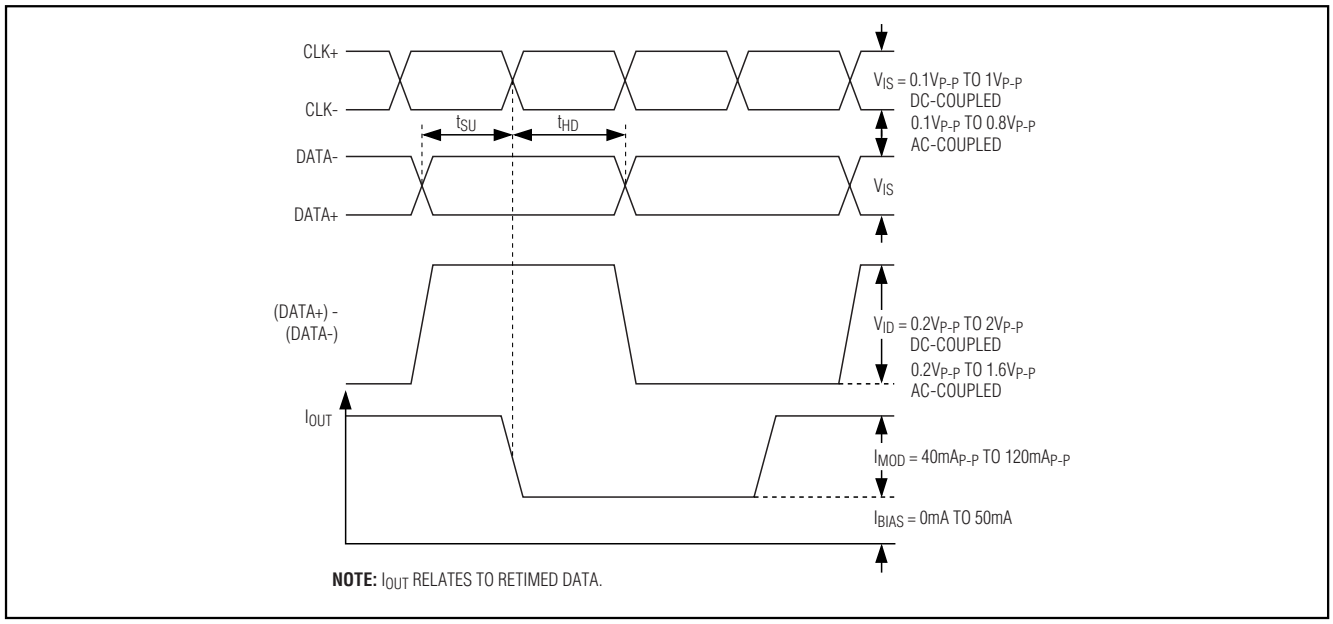

Figure 3. Setup and Hold Timing Definition

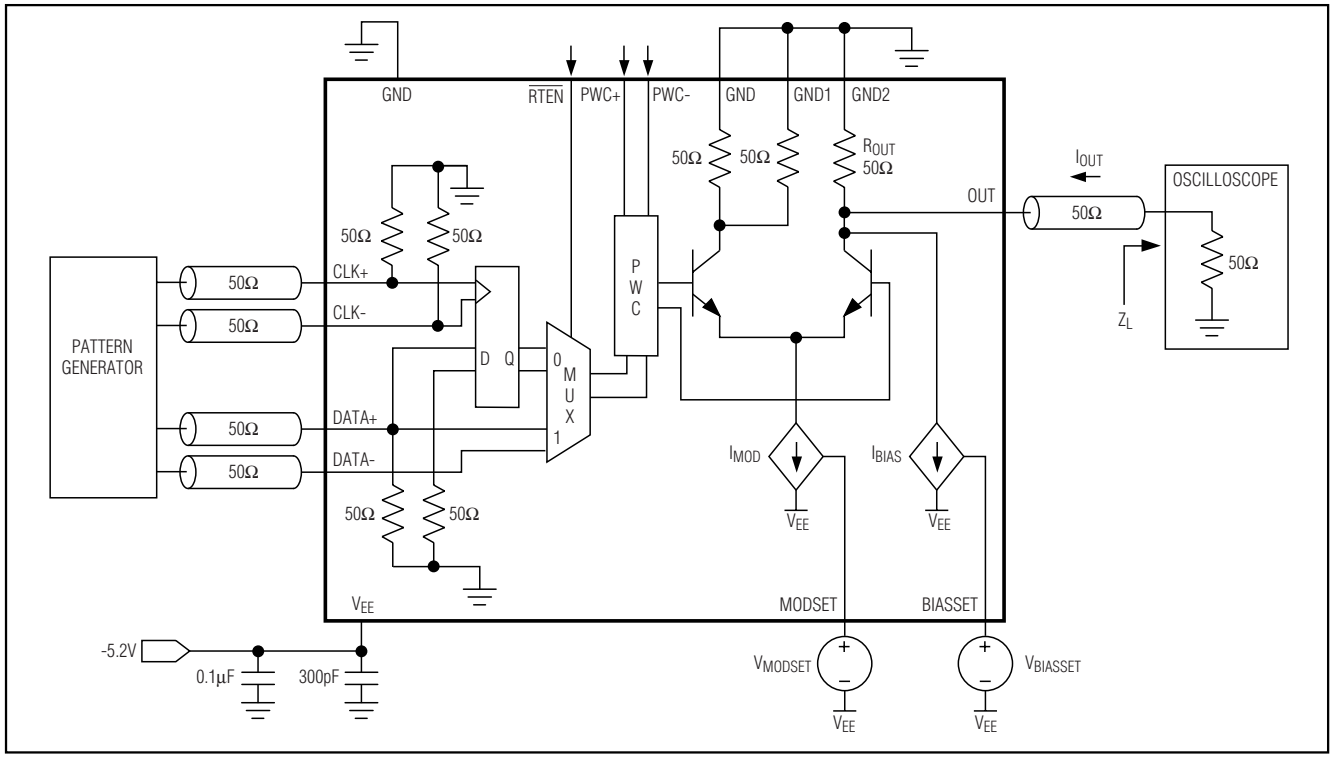

Figure 4. AC-Characterization Circuit

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Test Circuits and Timing Diagrams (continued)

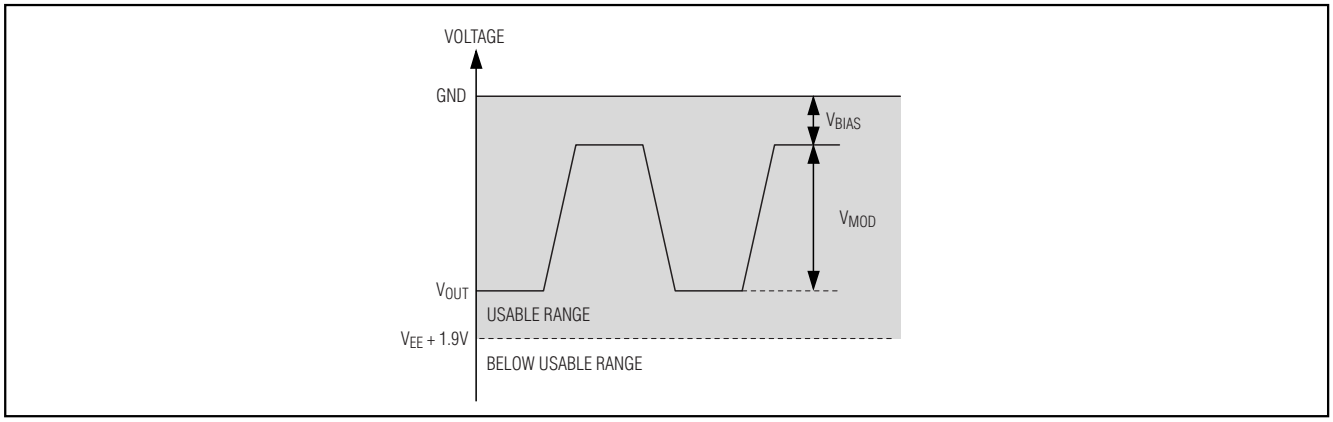
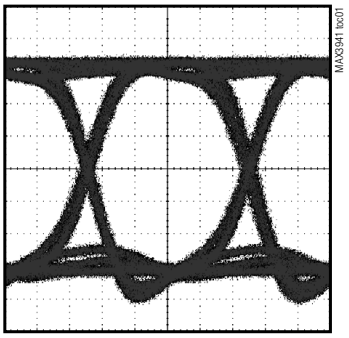


Figure 5. Bias and Modulation Relationship to EAM Voltage

Typical Operating Characteristics

(Typical values are at V_{EE} = -5.2V, I_{BIAS} = 30mA, I_{MOD} = 100mA, T_A = +25°C, unless otherwise noted.)

10Gbps ELECTRICAL EYE DIAGRAM (V_{MOD} = 1V_{P-P}, 2^{31} - 1 PRBS)



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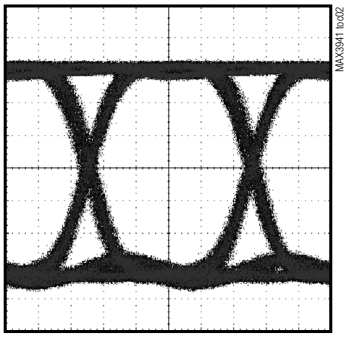
10Gbps ELECTRICAL EYE DIAGRAM (V_{MOD} = 3V_{P-P}, 2^{31} - 1 PRBS)



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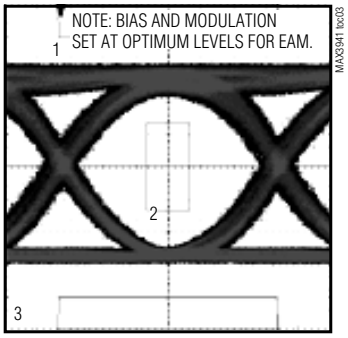
OC-192 OPTICAL EYE DIAGRAM (OC-192 FILTER, 2^{31} - 1 PRBS)



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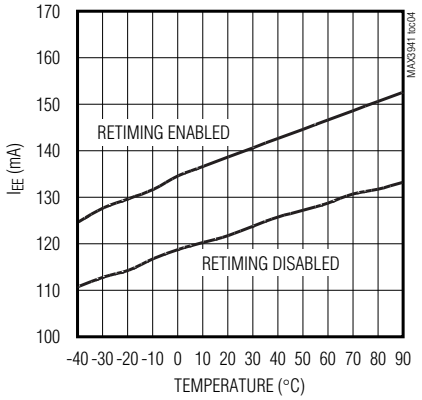
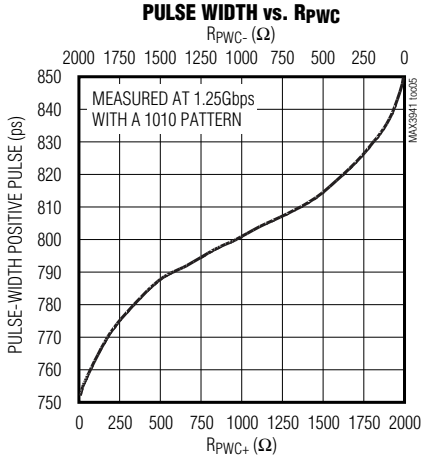
SUPPLY CURRENT vs. TEMPERATURE (50Ω LOAD, EXCLUDES I_{BIAS}, I_{MOD})



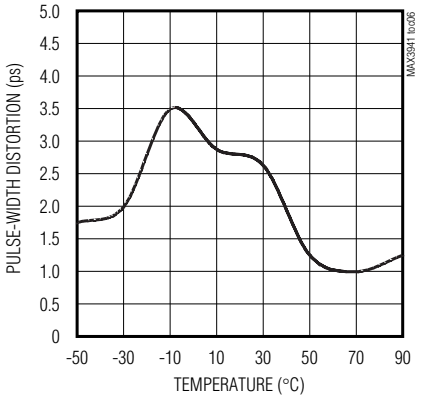
PULSE WIDTH vs. R_{PWC}



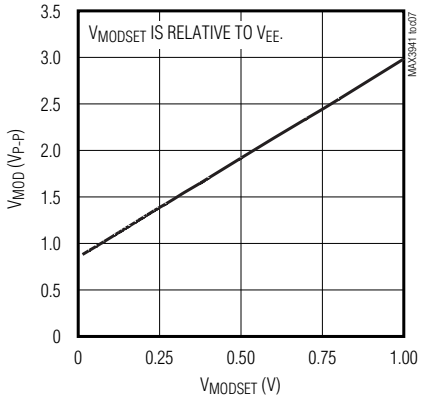
Typical Operating Characteristics (continued)

(Typical values are at V_{EE} = -5.2V, I_{BIAS} = 30mA, I_{MOD} = 100mA, T_A = +25°C, unless otherwise noted.)

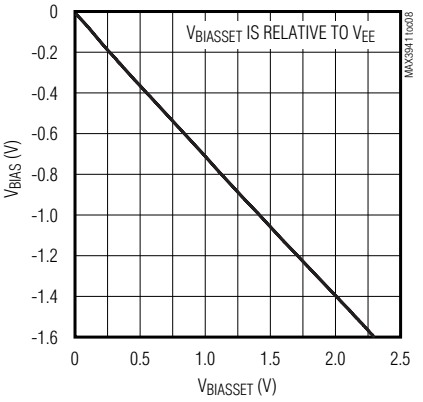
PULSE-WIDTH DISTORTION vs. TEMPERATURE



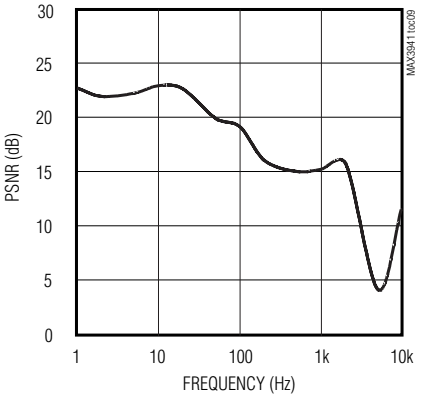
V_{MOD} vs. V_{MODSET} (Z_L = 50Ω)



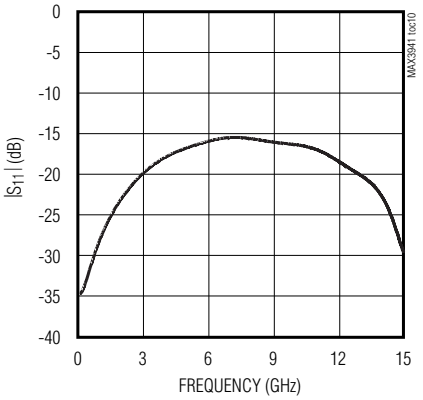
V_{BIAS} vs. $V_{BIASSET}$ (Z_L = 50Ω)



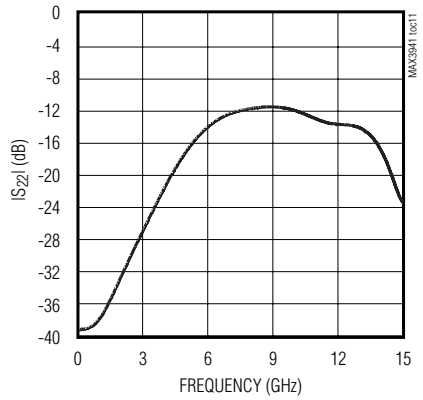
POWER-SUPPLY NOISE REJECTION vs. FREQUENCY



DIFFERENTIAL S_{11} vs. FREQUENCY (DEVICE POWERED)



S_{22} vs. FREQUENCY (DEVICE POWERED)



10Gbps EAM Driver with Integrated Bias Network

Pin Description

PIN	NAME	FUNCTION
1	DATA+	Noninverting Data Input with 50Ω On-Chip Termination
2	DATA-	Inverting Data Input with 50Ω On-Chip Termination
3, 4, 14	GND	Ground. All pins must be connected to board ground.
5	CLK+	Noninverting Clock Input for Data Retiming with 50Ω On-Chip Termination
6	CLK-	Inverting Clock Input for Data Retiming with 50Ω On-Chip Termination
7, 11, 12, 13, 18, 19, 24	V_{EE}	Negative Supply Voltage. All pins must be connected to board V_{EE}.
8	PWC+	Positive Input for Modulation Pulse-Width Adjustment (See the *Design Procedure* Section)
9	PWC-	Negative Input for Modulation Pulse-Width Adjustment. Ground to disable the pulse-width adjustment feature (see the *Design Procedure* section).
10	MODSET	Modulation Current Set. Apply a voltage to set the modulation current of the driver output.
15	GND1	Ground. Ground connection.
16	OUT	Driver Output. Provides both modulation and bias output. DC-couple to EAM.
17	GND2	Ground. Ground connection.
20	PLRT	Differential Data Polarity Swap Input. Set high or float for normal operation. Set low to invert the differential signal polarity. Contains an internal 100kΩ pullup to GND.
21	BIASSET	Bias Current Set. Apply a voltage to set the bias current of the driver output.
22	$\overline{MODEN}$	TTL/CMOS Modulation Enable Input. Set low or float for normal operation. Set high to put the EAM in the absorption (logic 0) state. Contains an internal 100kΩ pulldown to V_{EE}.
23	$\overline{RTEN}$	Data-Retiming Input. Connect to V_{EE} for retimed data. Connect to GND to bypass retiming latch.
EP	Exposed Pad	Ground. Must be soldered to the circuit board ground for proper thermal and electrical performance (see the *Exposed Pad Package* section).

Detailed Description

The MAX3941 EAM driver consists of two main parts: a high-speed modulation driver and an EAM-biasing block. The clock and data inputs to the driver are compatible with PECL and CML logic levels. The modulation and bias currents are output through the OUT pin.

The modulation output stage is composed of a high-speed differential pair and a programmable current source with a maximum modulation current of 120mA. The rise and fall times are typically 23ps. The modulation current is designed to produce an EAM voltage up to $3.0V_{P-P}$ when driving a 50Ω module. The $3.0V_{P-P}$ results from $120mA_{P-P}$ through the parallel combination of the 50Ω EAM load and the internal 50Ω back termination.

Polarity Switch

The MAX3941 includes a polarity switch. When the PLRT pin is high or left floating, the output maintains the polarity of the input data. When the PLRT pin is low, the output is inverted relative to the input data.

Clock/Data Input Logic Levels

The MAX3941 is directly compatible with ground-reference CML. Either DC- or AC-coupling can be used for CML referenced to ground. For all other logic types, AC-coupling should be used.

Optional Data Input Latch

To reject pattern-dependent jitter in the input data, a synchronous differential clock signal should be connected to the CLK+ and CLK- inputs, and the $\overline{RTEN}$ control input should be connected to V_{EE}.

The input data is retimed on the rising edge of CLK+. If $\overline{RTEN}$ is connected to ground, the retiming function is disabled and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

Pulse-Width Control

The pulse-width control circuit can be used to compensate for pulse-width distortion introduced by the EAM. The differential voltage between PWC+ and PWC- adjusts the pulse-width compensation. The adjustment range is typically ±50ps. Optional single-ended operation is possible by forcing a voltage on the PWC+ pin while leaving the PWC- pin unconnected. When PWC- is connected to ground, the pulse-width control circuit is automatically disabled.

Modulation Output Enable

The MAX3941 incorporates a modulation current-enable input. When $\overline{MODEN}$ is low or floating, the modulation/bias output (OUT) is enabled. When $\overline{MODEN}$ is high, the output is switched to the logic 0 state. The typical enable time is 2ns and the typical disable time is 2ns.

Design Procedure

Programming the Modulation Voltage

The EAM modulation voltage results from I_{MOD} passing through the EAM impedance (Z_L) in parallel with the internal 50Ω termination resistor (R_{OUT}):

$$V_{MOD} \approx I_{MOD} \times \frac{Z_L \times R_{OUT}}{Z_L + R_{OUT}}$$

To program the desired modulation current, force a voltage at the MODSET pin (see the *Typical Application Circuit*). The resulting I_{MOD} current can be calculated by the following equation:

$$I_{MOD} \approx \frac{V_{MODSET}}{11.1\Omega} + 37mA$$

An internal, independent current source drives a constant 37mA to the modulation circuitry, and any voltage above V_{EE} on the MODSET pin adds to this. The input impedance of the MODSET pin is typically 20kΩ. Note that the minimum output voltage is V_{EE} + 1.9V (Figure 5).

Programming the Bias Voltage

As in the case of modulation, the EAM bias voltage results from I_{BIAS} passing through the EAM impedance (Z_L) in parallel with the internal 50Ω termination resistor (R_{OUT}):

$$V_{BIAS} \approx I_{BIAS} \times \frac{Z_L \times R_{OUT}}{Z_L + R_{OUT}}$$

To program the desired bias current, force a voltage at the BIASSET pin (see the *Typical Application Circuit*). The resulting I_{BIAS} current can be calculated by the following equation:

$$I_{BIAS} \approx \frac{V_{BIASSET}}{36.4\Omega}$$

The input impedance of the BIASSET pin is typically 20kΩ. Note that the minimum output voltage is V_{EE} + 1.9V (Figure 5).

Programming the Pulse-Width Control

Three methods of control are possible when pulse predistortion is desired to minimize distortion at the receiver. The pulse width can be set with a 2kΩ potentiometer with the center tapped to V_{EE} (or equivalent fixed resistors), by applying a voltage to the PWC+ pin, or by applying a differential voltage across the PWC+ and PWC- pins. See Table 1 for the desired effect of the pulse-width setting. Pulse width is defined as (positive pulse width)/((positive pulse width + negative pulse width)/2).

Input Termination Requirement

The MAX3941 data and clock inputs are CML compatible. However, it is not necessary to drive the IC with a standard CML signal. As long as the specified input voltage swings are met, the MAX3941 operates properly.

Applications Information

Layout Considerations

To minimize loss and crosstalk, keep the connections between the MAX3941 output and the EAM module as short as possible. Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Circuit boards should be made using low-loss dielectrics. Use controlled-impedance lines for the clock and data inputs as well as for the data output. Be sure to filter the power supply with capacitors placed close to the IC.

Table 1. Pulse-Width Control

PULSE-WIDTH (%)	R_{PWC+}, R_{PWC-} FOR $R_{PWC+} + R_{PWC-} = 2k\Omega$	V_{PWC+} (PWC- OPEN) (V)	$V_{PWC+} - V_{PWC-}$ (V)
100	$R_{PWC+} = R_{PWC-}$	V_{EE} + 1	0
>100	$R_{PWC+} > R_{PWC-}$	> V_{EE} + 1	>0
<100	$R_{PWC+} < R_{PWC-}$	< V_{EE} + 1	<0

10Gbps EAM Driver with Integrated Bias Network

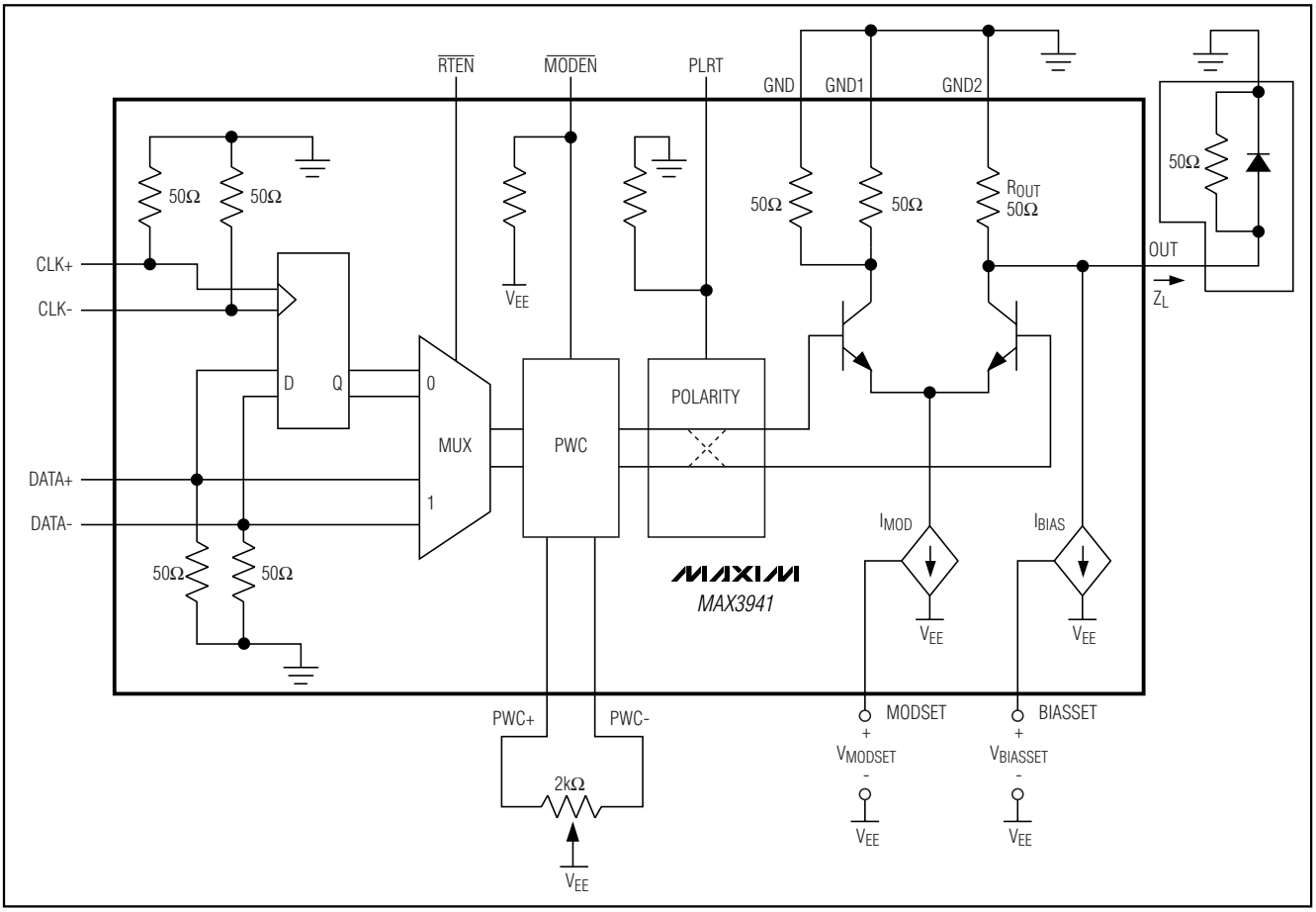


Figure 6. Functional Diagram

Interface Schematics

Figures 7 and 8 show simplified input and output circuits of the MAX3941 EAM driver.

Exposed-Pad Package

The exposed pad on the 24-pin QFN provides a very low thermal-resistance path for heat removal from the IC. The pad is also electrically ground on the MAX3941 and must be soldered to the circuit board for proper thermal and electrical performance. Refer to Maxim Application Note HFAN-08.1: *Thermal Considerations for QFN and Other Exposed-Pad Packages* for additional Information.

Laser Safety and IEC 825

Using the MAX3941 EAM driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each customer must determine the level of fault tolerance required by their application, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

10Gbps EAM Driver with Integrated Bias Network

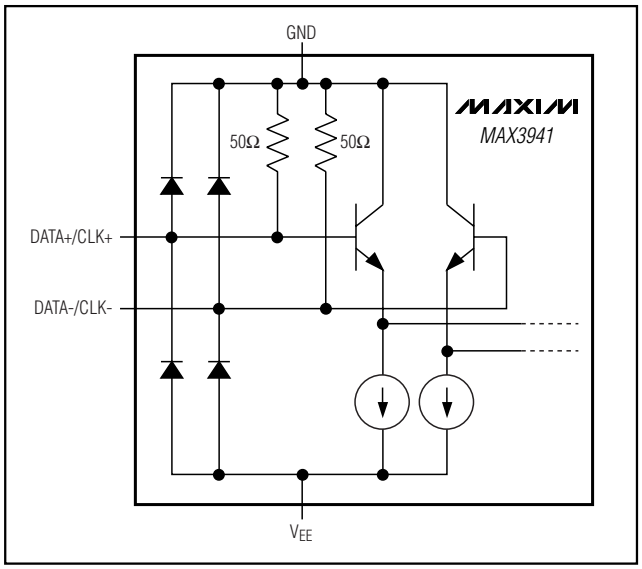


Figure 7. Simplified Input Circuit

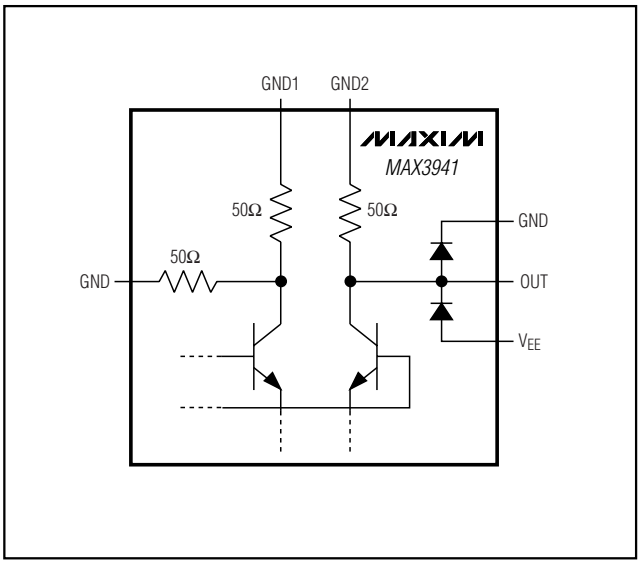
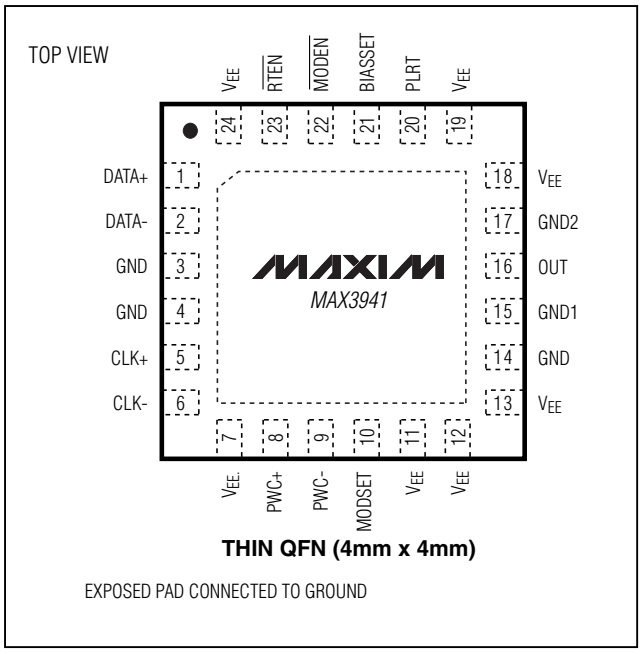


Figure 8. Simplified Output Circuit

Pin Configuration



THIN QFN (4mm x 4mm)

EXPOSED PAD CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PART	PACKAGE TYPE	PACKAGE CODE
MAX3941ETG	24-Thin QFN 4mm x 4mm x 0.8mm	T2444-1

Chip Information

TRANSISTOR COUNT: 1918

PROCESS: SiGe Bipolar