



# High-Precision, Low-Voltage, Micropower Op Amp

MAX480

## General Description

The MAX480 is a precision micropower operational amplifier with flexible power-supply capability. Its guaranteed 140 $\mu$ V maximum offset voltage (25 $\mu$ V typ) is the lowest of any micropower op amp. Similarly, input bias current, input offset current, and drift specifications are within tight limits.

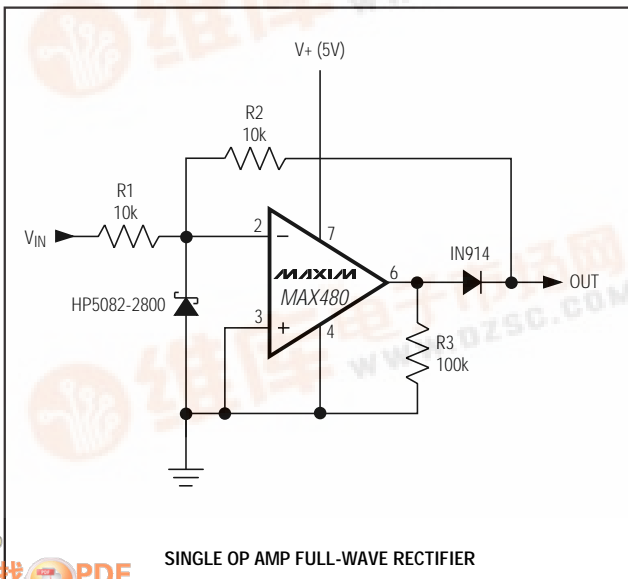
Both the input and output voltage ranges include the negative supply rail, allowing maximum signal range capability in single-supply applications. The MAX480 operates with either a single supply ranging from +1.6V to +36V or dual supplies from  $\pm 0.8$ V to  $\pm 18$ V. The MAX480 consumes less than 20 $\mu$ A, allowing operation in excess of 10,000 hours from a 250mA-hr lithium coin cell. Even with a minimal quiescent current, the amplifier sinks or sources 5mA from its output.

The MAX480 is available in 8-pin DIP and SO packages in commercial, extended, and military temperature ranges.

## Applications

- Precision Micropower Amplifiers
- Micropower Signal Processing
- Battery-Powered Analog Circuits

## Typical Operating Circuit



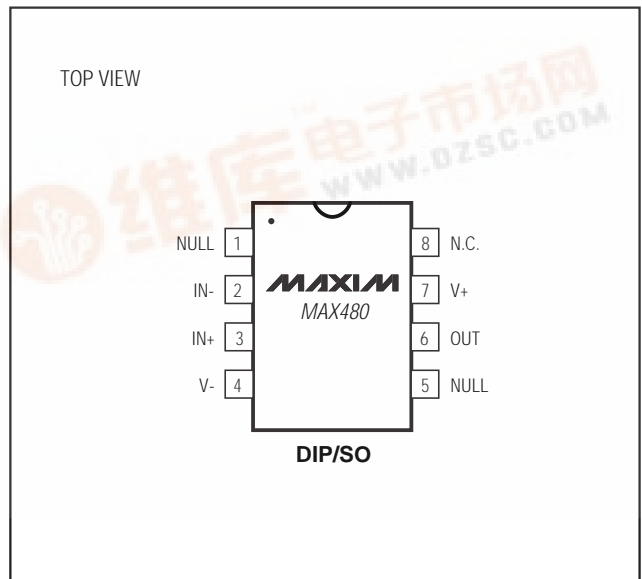
## Features

- ◆ Single- or Dual-Supply Operation: +1.6V to +36V,  $\pm 0.8$ V to  $\pm 18$ V
- ◆ True Single-Supply Operation: Input and Output Voltage Ranges Include Ground
- ◆ 2.0 $\mu$ V/ $^{\circ}$ C Max Offset Voltage Drift
- ◆ 20 $\mu$ A Max Supply Current
- ◆ 5mA Min Output Drive
- ◆ 140 $\mu$ V Max Input Offset Voltage
- ◆ 3nA Max Input Bias Current
- ◆ 500V/mV Min Open-Loop Gain
- ◆ Standard 741 Pinout with Nulling to V-

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX480CPA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 Plastic DIP
MAX480CSA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 SO
MAX480EPA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 Plastic DIP
MAX480ESA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 SO
MAX480MJA	-55 $^{\circ}$ C to +125 $^{\circ}$ C	8 CERDIP

## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-)	±18V
Differential Input Voltage	(V- - 20V) to (V+ + 20V)
Common-Mode Input Voltage	(V- - 20V) to (V+ + 20V)
Output Short-Circuit Duration	Indefinite
Continuous Power Dissipation	
Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
SO (derate 5.88mW/°C above +70°C)	471mW
CERDIP (derate 8.0mW/°C above +70°C)	640mW

## Operating Temperature Ranges

MAX480C_A	0°C to +70°C
MAX480E_A	-40°C to +85°C
MAX480MJA	-55°C to +125°C
Junction Temperature (T <sub>J</sub> )	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>S</sub> = ±1.5V to ±15V, T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V <sub>OS</sub>				25	140	μV
Input Offset Current	I <sub>OS</sub>	V <sub>CM</sub> = 0			0.2	1	nA
Input Bias Current	I <sub>B</sub>	V <sub>CM</sub> = 0			1	3	nA
Large-Signal Voltage Gain	A <sub>VO</sub>	V <sub>S</sub> = ±15V, V <sub>O</sub> = ±10V	R <sub>L</sub> = 100kΩ	500	1200	V/mV	
			R <sub>L</sub> = 10kΩ	200	600		
			R <sub>L</sub> = 2kΩ	75	250		
		V <sub>+</sub> = 5V, V <sub>-</sub> = 0, 1V < V <sub>O</sub> < 4V	R <sub>L</sub> = 100kΩ	100	400		
			R <sub>L</sub> = 10kΩ	50	180		
Input Voltage	IVR	V <sub>+</sub> = 5V, V <sub>-</sub> = 0		0/4		V	
		V <sub>S</sub> = ±15kV (Note 1)		-15/13.5			
Output Voltage Swing	V <sub>O</sub>	V <sub>S</sub> = ±15V	R <sub>L</sub> = 10kΩ	±14	±14.2	V	
			R <sub>L</sub> = 2kΩ	±11	±12		
	V <sub>OH</sub>	V <sub>+</sub> = 5V, V <sub>-</sub> = 0, R <sub>L</sub> = 2kΩ		4.0	4.2		
	V <sub>OL</sub>	V <sub>+</sub> = 5V, V <sub>-</sub> = 0, R <sub>L</sub> = 10kΩ		100	500	μV	
Common-Mode Rejection Ratio	CMRR	V <sub>+</sub> = 5V, V <sub>-</sub> = 0, 0 < V <sub>CM</sub> < 4V		85	110	dB	
		V <sub>S</sub> = ±15V, -15V < V <sub>CM</sub> < 13.5V		90	130		
Power-Supply Rejection Ratio	PSRR				1.0	12	μV/V
Slew Rate	SR	V <sub>S</sub> = ±15V		5	12	V/ms	
Supply Current	I <sub>SY</sub>	V <sub>S</sub> = ±1.5V			9	15	μA
		V <sub>S</sub> = ±15V			14	20	
Capacitive Load Stability		A <sub>v</sub> = +1V/V, no oscillations (Note 2)		250	650	pF	
Input Noise Voltage	e <sub>np-p</sub>	f <sub>O</sub> = 0.1Hz to 10Hz, V <sub>S</sub> = ±15V			3	μVp-p	
Differential-Mode Input Resistance	R <sub>IN</sub>	V <sub>S</sub> = ±15V			30	MΩ	
Common-Mode Input Resistance	R <sub>INCM</sub>	V <sub>S</sub> = ±15V			20	GΩ	

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## ELECTRICAL CHARACTERISTICS

( $V_S = \pm 1.5V$  to  $\pm 15V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX480C			MAX480E			MAX480M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		40	220		50	250	70	300		$\mu V$	
Input Offset Voltage Drift	$TCV_{OS}$	(Note 2)	0.3	2.0		0.3	2.0	0.3	2.0		$\mu V/^{\circ}C$	
Input Offset Current	$I_{OS}$	$V_{CM} = 0$	0.2	2.0		0.3	2.0	0.5	2.0		nA	
Input Bias Current	$I_B$	$V_{CM} = 0$	1	3		2	5	3	7		nA	
Large-Signal Voltage Gain	$A_{VO}$	$V_S = \pm 15V$ , $V_- = \pm 10V$	$R_L = 100k\Omega$	350	950		350	800	60	400	V/mV	
			$R_L = 10k\Omega$	130	400		130	400	45	240		
			$R_L = 2k\Omega$	55	125		55	150	30	110		
		$V_+ = 5V$ , $V_- = 0$ , $1V < V_O < 4V$	$R_L = 100k\Omega$	50	360		50	280	35	200		
			$R_L = 10k\Omega$	30	150		30	140	22	110		
Input Voltage Range	IVR	$V_+ = 5V$ , $V_- = 0$	0/3.5			0/3.5		0/3.5		V		
		$V_S = \pm 15V$ (Note 1)	-15/13.5			-15/13.5		-15/13.5				
Output Voltage Swing	$V_O$	$V_S = \pm 15V$	$R_L = 10k\Omega$	$\pm 13.5$	$\pm 14$		$\pm 13.5$	$\pm 14$	$\pm 13.5$	$\pm 13.7$	V	
			$R_L = 2k\Omega$	$\pm 10.5$	$\pm 11.8$		$\pm 10.5$	$\pm 11.8$	$\pm 10.5$	$\pm 11.5$		
	$V_{OH}$	$V_+ = 5V$ , $V_- = 0$ $R_L = 2k\Omega$	3.9	4.1		3.9	4.1	3.9	4.1			
	$V_{OL}$	$V_+ = 5V$ , $V_- = 0$ $R_L = 10k\Omega$	100	500		100	500	100	500	$\mu V$		
Common-Mode Rejection Ratio	CMRR	$V_+ = 5V$ , $V_- = 0$ , $0 < V_{CM} < 3.5V$	85	110		85	110	80	105	dB		
		$V_S = \pm 15V$ , $-15V < V_{CM} < 13.5V$	90	120		90	120	85	115			
Power-Supply Rejection Ratio	PSRR		1.0	12		1.0	12	3.2	15	$\mu V/V$		
Supply Current	$I_{SY}$	$V_S = \pm 1.5V$	12	25		13	25	15	25	$\mu A$		
		$V_S = \pm 15V$	16	30		17	30	19	30			

**Note 1:** Guaranteed by CMRR test.

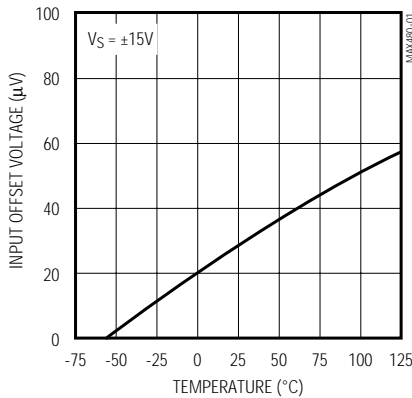
**Note 2:** Guaranteed by design.

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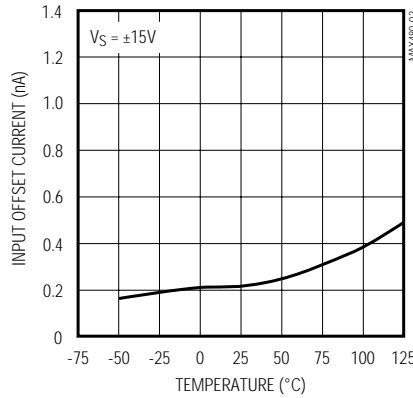
## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

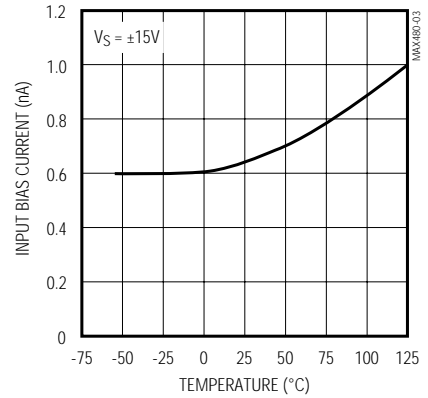
**INPUT OFFSET VOLTAGE vs. TEMPERATURE**



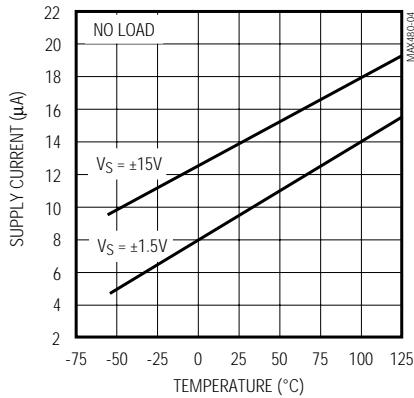
**INPUT OFFSET CURRENT vs. TEMPERATURE**



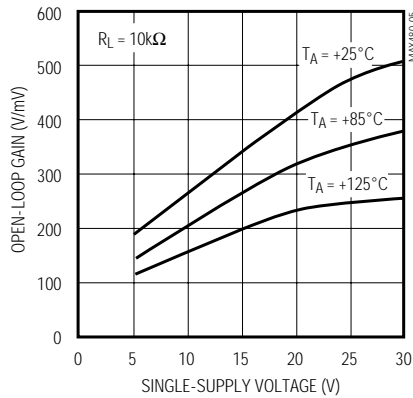
**INPUT BIAS CURRENT vs. TEMPERATURE**



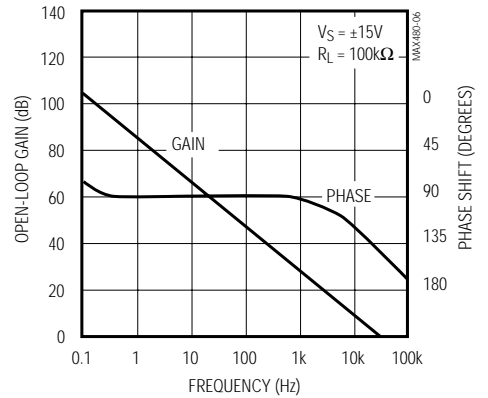
**SUPPLY CURRENT vs. TEMPERATURE**



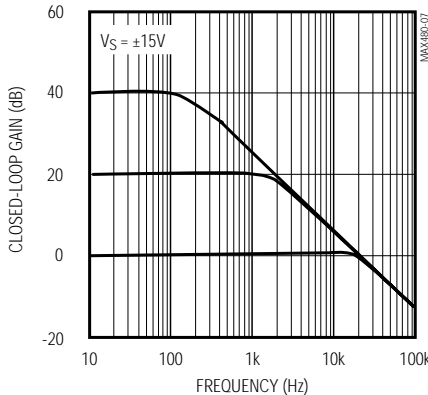
**OPEN-LOOP GAIN vs. SINGLE-SUPPLY VOLTAGE**



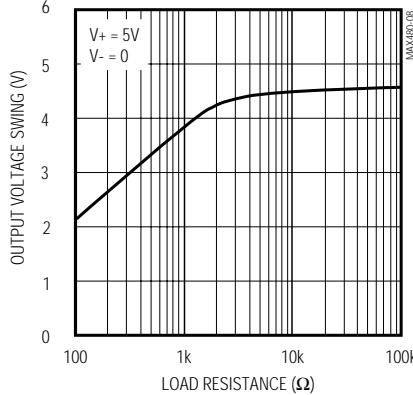
**OPEN-LOOP GAIN AND PHASE SHIFT vs. FREQUENCY**



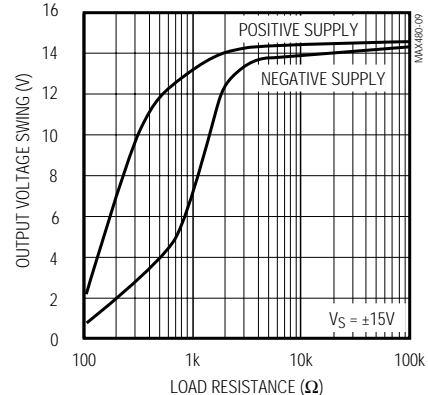
**CLOSED-LOOP GAIN vs. FREQUENCY**



**OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE**



**OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE**

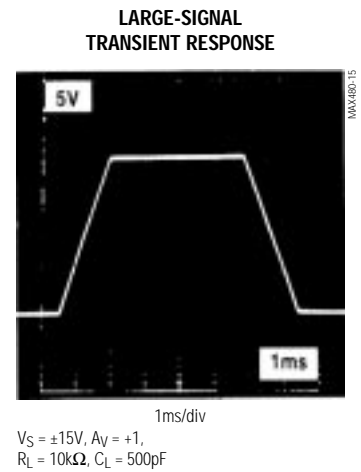
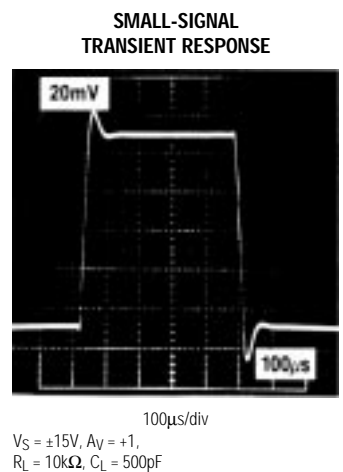
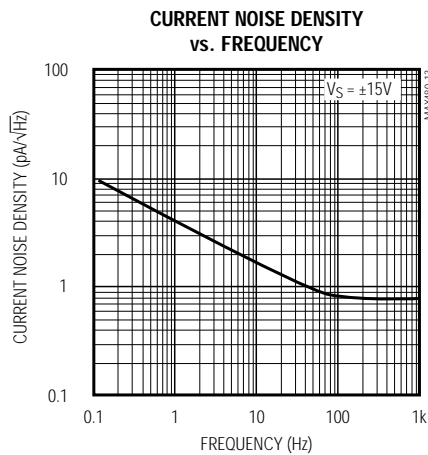
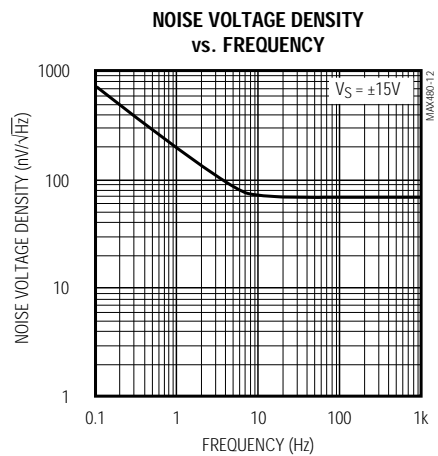
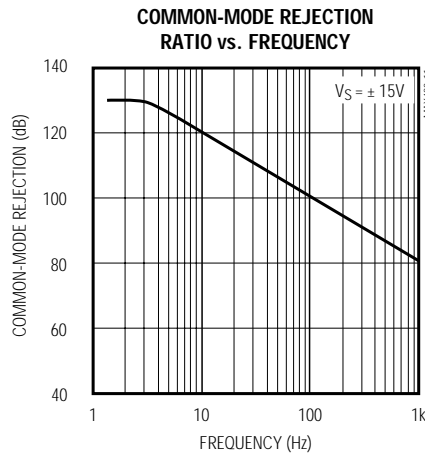
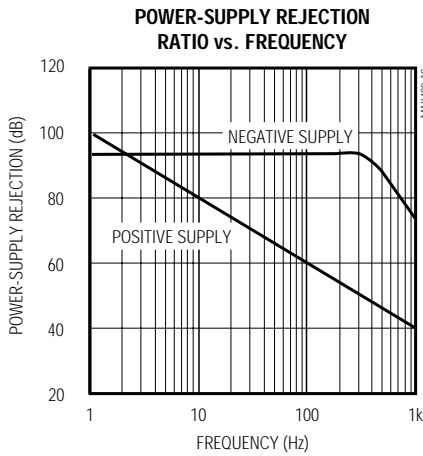


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## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

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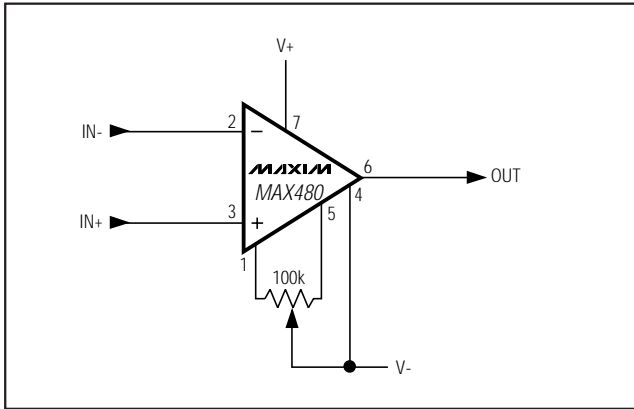


Figure 1. Offset Nulling Circuit

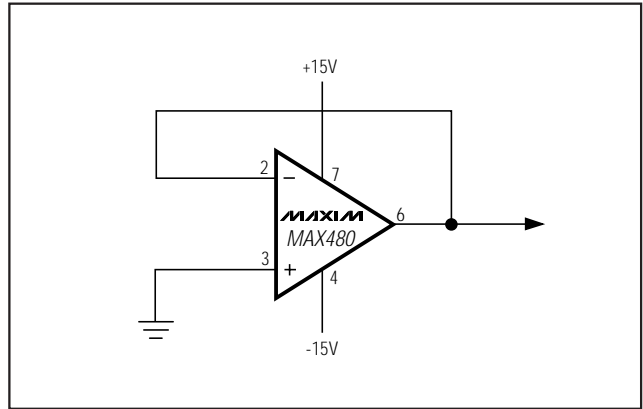


Figure 2. Burn-In Circuit

## Package Information

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:  
 1. D&E DO NOT INCLUDE MOLD FLASH  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")  
 3. LEADS TO BE COPLANAR WITHIN .102mm (.004")  
 4. CONTROLLING DIMENSION: MILLIMETER  
 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE  
 6. N = NUMBER OF PINS

**MAXIM** PACKAGE FAMILY OUTLINE: SOIC .150" 1/1 21-0041 A  
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