



Monolithic CMOS Analog Multiplexers

General Description

Maxim's MX7506 and MX7507 are monolithic CMOS analog multiplexers. The MX7506 is a single 16 channel (1 of 16) multiplexer, and the MX7507 is a differential 8 channel (2 of 16) multiplexer.

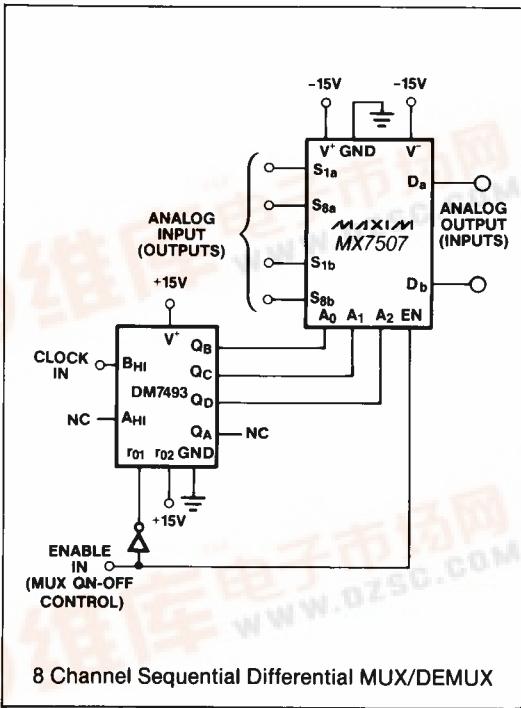
Both devices feature break-before-make switching. Maxim guarantees that these multiplexers will not latch-up if the power supplies are turned off with the input signals still present, as long as absolute maximum ratings are not violated. The multiplexers operate over a wide range of power supplies from $\pm 4.5V$ to $\pm 18V$.

Compared to the original manufacturer's devices, Maxim's MX7506 and MX7507 consume significantly less power, making them ideal for portable equipment.

Applications

- Control Systems
- Data Logging Systems
- Aircraft Heads Up Displays
- Data Acquisition Systems
- Signal Routing

Typical Operating Circuit



Features

- ◆ Improved 2nd Source!
- ◆ Drop in Replacement for Analog Devices
- ◆ Operable with $\pm 4.5V$ to $\pm 18V$ Supplies
- ◆ Symmetrical, Bi-Directional Operation
- ◆ Logic and Enable inputs, TTL and CMOS Compatible
- ◆ Latch-Up Proof Construction
- Monolithic, Low-Power CMOS Design

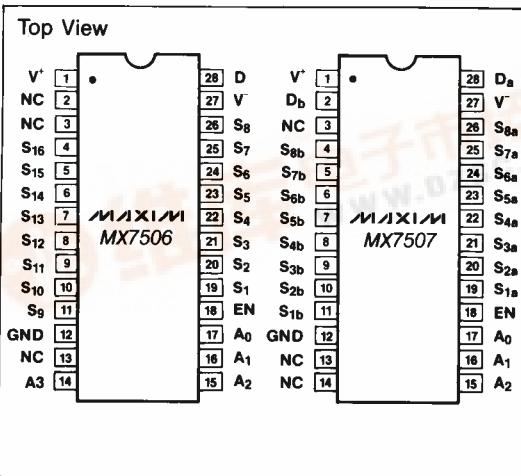
Ordering Information

PART	TEMP. RANGE	PACKAGE*
MX7506JN	0°C to +70°C	28 Lead Plastic DIP
MX7506KN	0°C to +70°C	28 Lead Plastic DIP
MX7506JQ	-25°C to +85°C	28 Lead CERDIP
MX7506KQ	-25°C to +85°C	28 Lead CERDIP
MX7506SQ	-55°C to +125°C	28 Lead CERDIP
MX7506TQ	-55°C to +125°C	28 Lead CERDIP
MX7507JN	0°C to +70°C	28 Lead Plastic DIP
MX7507KN	0°C to +70°C	28 Lead Plastic DIP
MX7507JQ	-25°C to +85°C	28 Lead CERDIP
MX7507KQ	-25°C to +85°C	28 Lead CERDIP
MX7507SQ	-55°C to +125°C	28 Lead CERDIP
MX7507TQ	-55°C to +125°C	28 Lead CERDIP

For Dice, Plastic Chip Carrier, Ceramic Leadless Chip Carrier and Ceramic Sidebrazed DIP contact factory.

*Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages.

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS (TA = 25°C unless otherwise noted.)

V _{DD} -GND	+17V	Power Dissipation (Any Package)
V _{SS} -GND	-17V	Up to +50°C 1000mW
V Between Any Switch Terminals (Note 1)	25V	Derates above +50°C by 10mW/°C
Digital Input Voltage Range	V _{DD} to GND	Operating Temperature
Oversupply at V _{OUT} (Vs)	V _{SS} , V _{DD}	Commercial (JN, KN Versions) 0°C to +70°C
Switch Current (I _S , Continuous One Channel)	20mA	Industrial (JQ, KQ Versions) -25°C to +85°C
Switch Current (I _S , Surge One Channel)		Extended (SQ, TQ Versions) -55°C to +125°C
1ms Duration, 10% Duty Cycle	35mA	Storage Temperature -65°C to +150°C

Note 1: Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.

Note 2: The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V⁺ = 15V, V⁻ = -15V, GND = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	VERSION (Note 3)	SWITCH CONDITION	TEST CONDITIONS	OVER SPECIFIED TEMP. RANGE			UNITS
					+25°C	MIN	TYP	
ANALOG SWITCH								
Drain-Source ON Resistance	r _{DS(ON)}	J, K S, T	ON ON	V _S = -10V to +10V, I _S = 1mA	300	450	550	Ω
	r _{DS(ON)} vs. V _S	All	ON		15			
Tempco of ON Resistance	r _{DS(ON)} vs. Temp.	All	ON	V _S = 0V, I _S = 1mA	0.5			%/°C
Difference in ON Resistance Between Channels	Δr _{DS(ON)} Between Switches	All	ON	V _S = 0V, I _S = 1mA	4			%
	Δr _{DS(ON)} vs. Temp. Between Switches	All	ON		0.05			%/°C
Source OFF Leakage Current	I _{S(OFF)}	J, K S, T	OFF OFF	V _S = -10V, V _D = +10V and V _S = +10V, V _D = -10V "Enable Low"	0.05	5	50	nA
Drain OFF Leakage Current	I _{D(OFF)}	J, K S, T	OFF OFF		0.3	20	500	
		J, K S, T	OFF OFF		0.3	10	500	
	MX7506	J, K S, T	OFF OFF		0.3	10	250	
Channel ON Leakage Current I _{D(ON)} -I _S (Any Switch ON)	MX7506	J, K S, T	ON ON	V _S = 0	0.3	20	500	nA
		J, K S, T	ON ON		0.3	10	500	
	MX7507	J, K S, T	ON ON		0.3	10	250	
		J, K S, T	ON ON		0.3	5	250	

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ELECTRICAL CHARACTERISTICS (Continued)

($V^+ = 15V$, $V^- = -15V$, GND = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	VERSION (Note 3)	SWITCH CONDITION	TEST CONDITIONS	+25°C			OVER SPECIFIED TEMP. RANGE	UNITS	
					MIN	TYP	MAX			
DIGITAL CONTROL										
Address Input Threshold (Low)	V_{INL}							0.8	V	
Address Input Threshold (High)	V_{INH}	J, S K, T		(Note 4)				3.0 2.4	V	
Input Logic Current	I_{INL} or I_{INH}	All				10		30	μ A	
Address Input Capacitance	C_{IN}	All			3				pF	
DYNAMIC CHARACTERISTICS (Note 5)										
Switching Time of Multiplexers	$t_{TRANSITION}$	J, S K, T		V_{IN} : 0 to 3.0V	700 700 1000			ns	μ s	
Break-Before-Make Interval	t_{OPEN}	All			100					
Enable Turn-ON Time	t_{ON} (EN)	J, S K, T		V_{EN} : 0 to 3.0V	0.8 1.5			1		
Enable Turn-OFF Time	t_{OFF} (EN)	J, S K, T			0.8 1					
OFF Isolation	OIRR	All		$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3.0\text{pF}$, $V_S = 3.0V_{RMS}$, $f = 50\text{kHz}$	70			dB		
Source OFF Capacitance	$C_{S(OFF)}$	All	OFF		5					
Drain OFF Capacitance	$C_{D(OFF)}$	All	OFF		40					
Source to Drain Capacitance	C_{S-D}	All	OFF		20					
Capacitance Between Any Two Switches	C_{SS}	All	OFF		0.5					
POWER SUPPLY										
Positive Supply Current	I^+	J, K S, T	OFF OFF	All Digital Inputs Low	0.05 0.05	0.5 0.5		1	mA	
Negative Supply Current	I^-	J, K S, T	OFF OFF		0.05 0.05	0.3 0.3		0.6		
Positive Supply Current	I^+	J, K S, T	ON ON	All Digital Inputs High	0.3 0.3	0.5 0.5		1		
Negative Supply Current	I^-	J, K S, T	ON ON		0.05 0.05	0.3 0.3		0.6		

Note 3: JN and KN versions specified for 0°C to +70°C; JQ and KQ versions for -25°C to +85°C; SQ and TQ versions for -55°C to +125°C.

Note 4: A pullup resistor, typically 1-2k Ω is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.

Note 5: AC parameters are sample tested to ensure conformance to specifications.

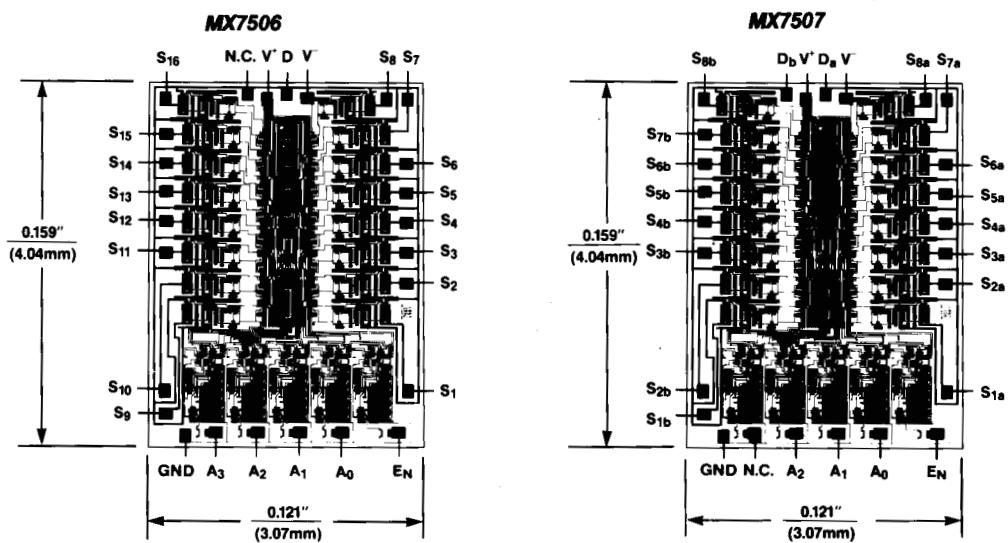
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Truth Tables

MX7506						MX7507					
A ₃	A ₂	A ₁	A ₀	EN	ON SWITCH	A ₂	A ₁	A ₀	EN	ON SWITCH	
X	X	X	X	0	NONE	X	X	X	0	NONE	
0	0	0	0	1	1	0	0	0	1	1	
0	0	0	1	1	2	0	0	1	1	2	
0	0	1	0	1	3	0	1	0	1	3	
0	0	1	1	1	4	0	1	1	1	4	
0	1	0	0	1	5	1	0	0	1	5	
0	1	0	1	1	6	1	0	1	1	6	
0	1	1	0	1	7	1	1	0	1	7	
0	1	1	1	1	8	1	1	1	1	8	
1	0	0	0	1	9						
1	0	0	1	1	10						
1	0	1	0	1	11						
1	0	1	1	1	12						
1	1	0	0	1	13						
1	1	0	1	1	14						
1	1	1	0	1	15						
1	1	1	1	1	16						

Logic "0" = V_{AL} ≤ 0.8V Logic "1" = V_{AH} ≥ 2.4V "0" = DON'T CARE

Chip Topography



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