19-2918; Rev 1; 1/04

MAXIM

PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

General Description

The MAX8506/MAX8507/MAX8508 integrate a PWM step-down DC-DC regulator and a 75mΩ (typ) bypass FET to power the PA in WCDMA and cdmaOne™ cell phones. The supply voltage range is from 2.6V to 5.5V, and the guaranteed output current is 600mA. One megahertz PWM switching allows for small external components.

The MAX8506 and MAX8507 are dynamically controlled to provide varying output voltages from 0.4V to 3.4V. The MAX8508 is externally programmed for fixed 0.75V to 3.4V output. Digital logic enables a high-power (HP) bypass mode that connects the output directly to the battery for all versions. The MAX8506/MAX8507/MAX8508 are designed so the output settles in less than 30µs for a full-scale change in output voltage and load current.

The MAX8506/MAX8507/MAX8508 are offered in 16-pin 4mm x 4mm thin QFN packages (0.8mm max height).

Applications

WCDMA/NCDMA Cell Phones

Wireless PDAs, Palmtops, and Notebook Computers

Wireless Modems

cdmaOne is a trademark of CDMA Development Group.

Features

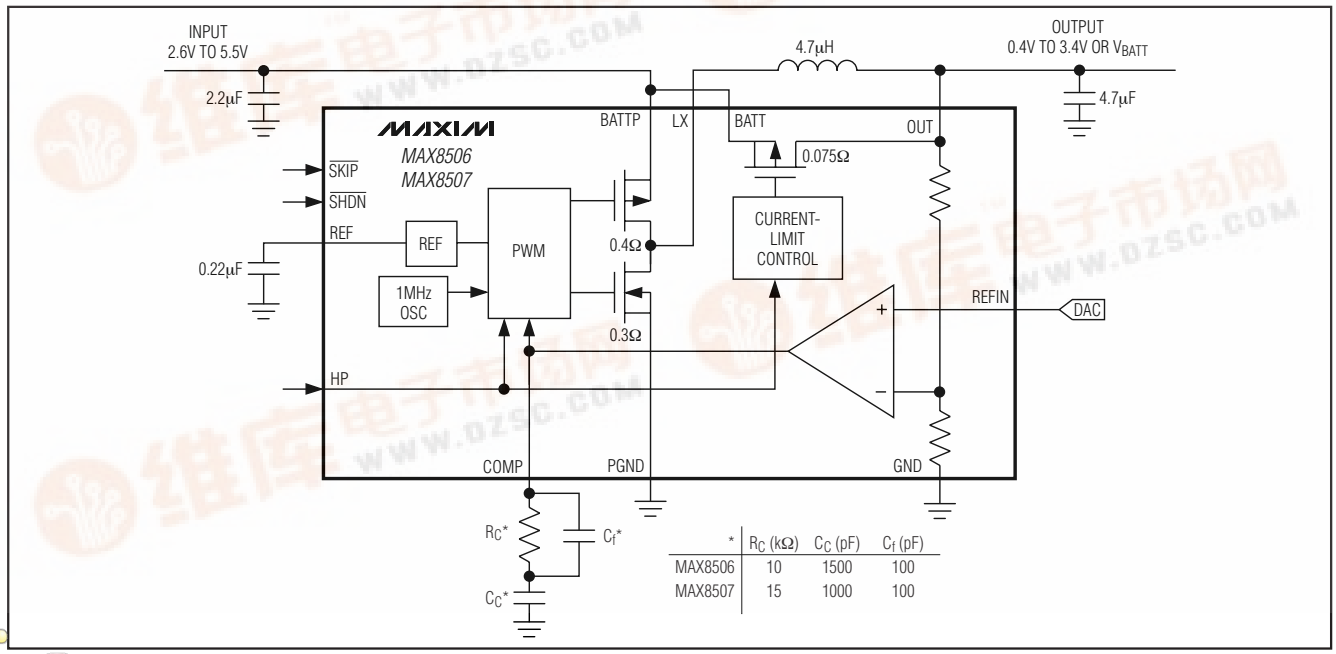
- **Integrated 75mΩ (typ) Bypass FET**
- **38mV Dropout at 600mA Load**
- **Up to 94% Efficiency**
- **Dynamically Adjustable Output from 0.4V to 3.4V (MAX8506, MAX8507)**
- **Externally Fixed Output from 0.75V to 3.4V (MAX8508)**
- **1MHz Fixed-Frequency PWM Switching**
- **600mA Guaranteed Output Current**
- **Shutdown Mode 0.1µA (typ)**
- **16-Pin Thin QFN (4mm x 4mm, 0.8mm max Height)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8506ETE	-40°C to +85°C	16 Thin QFN
MAX8507ETE	-40°C to +85°C	16 Thin QFN
MAX8508ETE	-40°C to +85°C	16 Thin QFN

Pin Configurations appear at end of data sheet.

Typical Application Circuits (MAX8506/MAX8507)



Typical Application Circuits continued at end of data sheet.

PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

ABSOLUTE MAXIMUM RATINGS

BATTP, BATT, OUT, $\overline{SHDN}$, $\overline{SKIP}$, HP, REFIN, FB to GND ..... -0.3V to +6V
PGND to GND ..... -0.3V to +0.3V
BATT to BATTP ..... -0.3V to +0.3V
OUT, COMP, REF to GND ..... -0.3V to (V_{BATT} + 0.3V)
LX Current (Note 1) 1.6A
OUT Current (Note 1) 3.2A
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 16.9mW/°C above +70°C) ... 1.349W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: LX has internal clamp diodes to PGND and BATT. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = V_{BATTP} = 3.6V, $\overline{SHDN}$ = $\overline{SKIP}$ = BATT, HP = GND, V_{REFIN} = 1.932V (MAX8506), V_{REFIN} = 1.70V (MAX8507), C_{REF} = 0.22µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input BATT Voltage			2.6		5.5	V
Undervoltage Lockout Threshold	V_{BATT} rising		2.150	2.35	2.575	V
Undervoltage Lockout Hysteresis				40		mV
Quiescent Current	$\overline{SKIP}$ = GND (normal mode)			180	250	µA
	$\overline{SKIP}$ = BATT, 1MHz switching			1750		
Quiescent Current in Dropout	HP = BATT			775	1000	µA
Shutdown Supply Current	$\overline{SHDN}$ = GND			0.1	5	µA
OUT Voltage Accuracy	V_{REFIN} = 1.932V, I_{OUT} = 0 to 600mA (MAX8506)		3.375	3.40	3.425	V
	V_{REFIN} = 0.426V, I_{OUT} = 0 to 30mA (MAX8506)		0.740	0.75	0.760	
	V_{REFIN} = 1.700V, I_{OUT} = 0 to 600mA (MAX8507)		3.375	3.40	3.425	
	V_{REFIN} = 0.375V, I_{OUT} = 0 to 30mA (MAX8507)		0.740	0.75	0.760	
OUT Input Resistance	MAX8506		250	485		kΩ
	MAX8507		275	535		
REFIN Input Current			-1	0.1	+1	µA
REFIN to OUT Gain	MAX8506			1.76		V/V
	MAX8507			2.00		
Reference Voltage			1.225	1.25	1.275	V
Reference Load Regulation	10µA < I_{REF} < 100µA			2.5	8.5	mV
Reference Bypass Capacitor			0.1	0.22		µF
FB Voltage Accuracy	FB = COMP (MAX8508)		0.7275	0.75	0.7725	V
FB Input Current	V_{FB} = 1V (MAX8508)			0.03	0.175	µA
P-Channel On-Resistance	I_{LX} = 180mA	V_{BATT} = 3.6V		0.4	0.825	Ω
		V_{BATT} = 2.6V		0.5		
N-Channel On-Resistance	I_{LX} = 180mA	V_{BATT} = 3.6V		0.3	0.5	Ω
		V_{BATT} = 2.6V		0.35		
HP/Bypass P-Channel On-Resistance	I_{OUT} = 180mA, V_{BATT} = 3.6V			0.075	0.110	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = V_{BATTP} = 3.6V, $\overline{SHDN}$ = $\overline{SKIP}$ = BATT, HP = GND, V_{REFIN} = 1.932V (MAX8506), V_{REFIN} = 1.70V (MAX8507), C_{REF} = 0.22µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
P-Channel Current-Limit Threshold		1.00	1.25	1.50	A
N-Channel Current-Limit Threshold	$\overline{SKIP}$ = BATT (PWM mode)	-0.6	-0.45	-0.30	A
	$\overline{SKIP}$ = GND (normal mode)	0.03	0.05	0.07	
P-Channel Pulse-Skipping Current Threshold	$\overline{SKIP}$ = GND (normal mode)	0.050	0.125	0.170	A
HP/Bypass P-Channel Current-Limit Threshold	V_{OUT} = 3.1V	0.8	1.5	2.5	A
LX Leakage Current		-2	0.01	+2	µA
OUT Leakage Current		-2	0.01	+2	µA
Maximum Duty Cycle		100			%
Minimum Duty Cycle	$\overline{SKIP}$ = GND (normal mode)			0	%
	$\overline{SKIP}$ = BATT			12	
COMP Clamp Low Voltage			0.8		V
COMP Clamp High Voltage			2.0		V
Transconductance	MAX8506	85	150	215	µS
	MAX8507	75	130	188	
	MAX8508	150	260	376	
Current-Sense Transresistance		0.36	0.48	0.60	V/A
OSCILLATOR					
Internal Oscillator Frequency		0.8	1	1.2	MHz
LOGIC INPUTS ($\overline{SHDN}$, HP, $\overline{SKIP}$)					
Logic-Input High Voltage	V_{BATT} = 2.6V to 5.5V	1.6			V
Logic-Input Low Voltage	V_{BATT} = 2.6V to 5.5V			0.4	V
Logic Input Current			0.1	1	µA
THERMAL SHUTDOWN					
Thermal-Shutdown Temperature			+160		°C
Thermal-Shutdown Hysteresis			15		°C

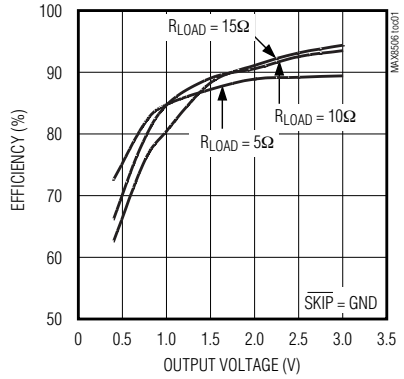
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

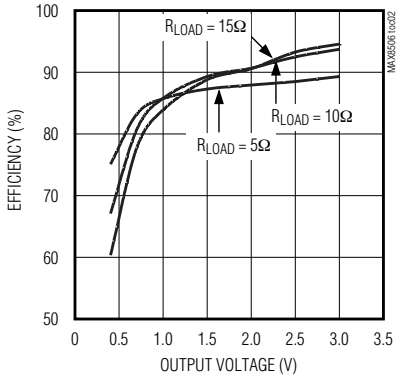
Typical Operating Characteristics

(V_{BATT} = V_{BATTP} = 3.6V, $\overline{SHDN}$ = $\overline{SKIP}$ = BATT, HP = GND, T_A = +25°C, unless otherwise noted.) (See the *Typical Application Circuits*.)

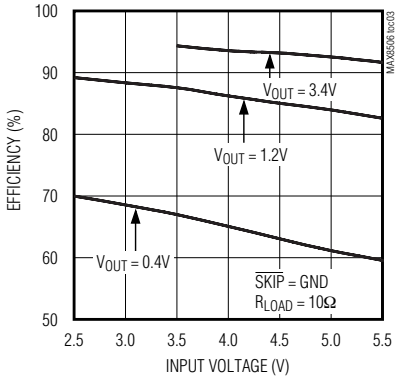
EFFICIENCY vs. OUTPUT VOLTAGE IN NORMAL MODE



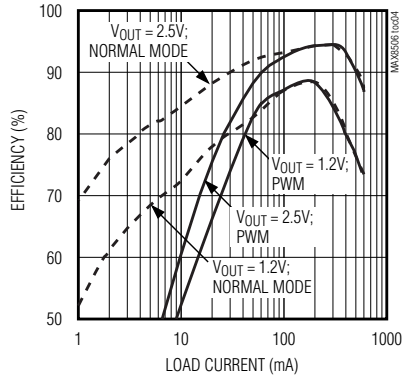
EFFICIENCY vs. OUTPUT VOLTAGE IN PWM MODE



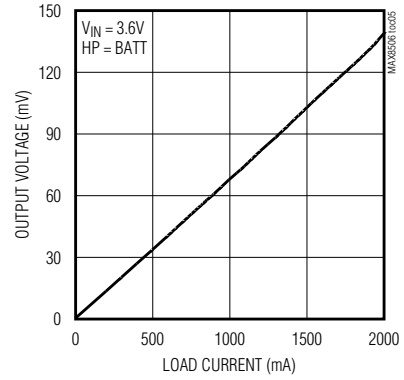
EFFICIENCY vs. INPUT VOLTAGE



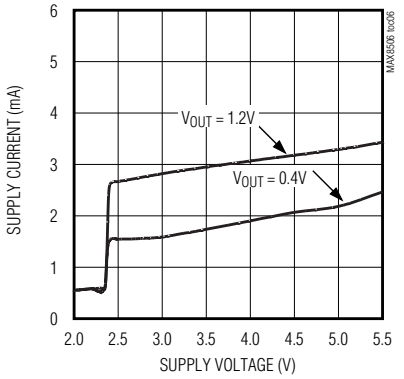
EFFICIENCY vs. LOAD CURRENT



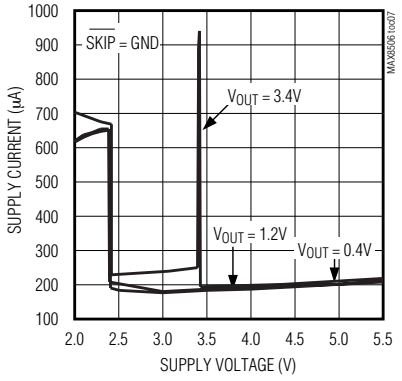
DROPOUT VOLTAGE vs. LOAD CURRENT



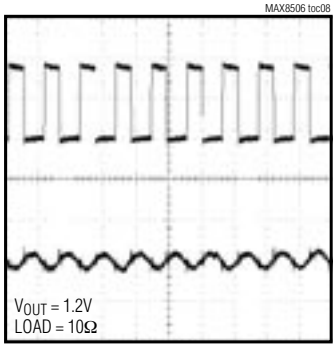
SUPPLY CURRENT vs. SUPPLY VOLTAGE IN PWM MODE



SUPPLY CURRENT vs. SUPPLY VOLTAGE IN NORMAL MODE



HEAVY-LOAD SWITCHING WAVEFORM

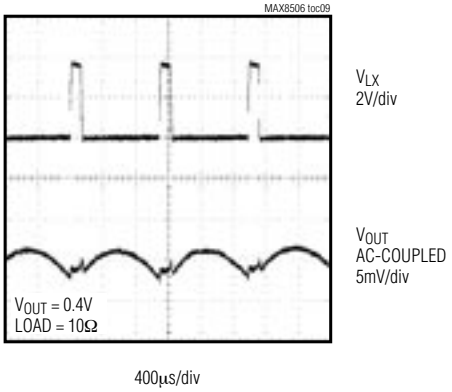


PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

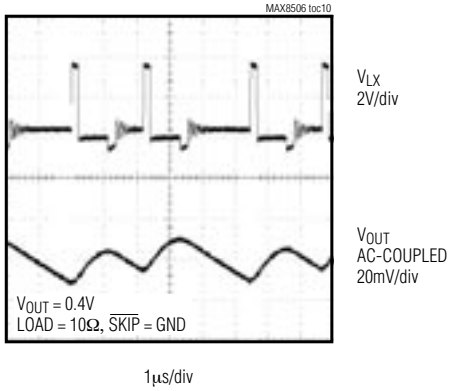
Typical Operating Characteristics (continued)

(V_{BATT} = V_{BATTP} = 3.6V, $\overline{SHDN}$ = $\overline{SKIP}$ = BATT, HP = GND, T_A = +25°C, unless otherwise noted.) (See the *Typical Application Circuits*.)

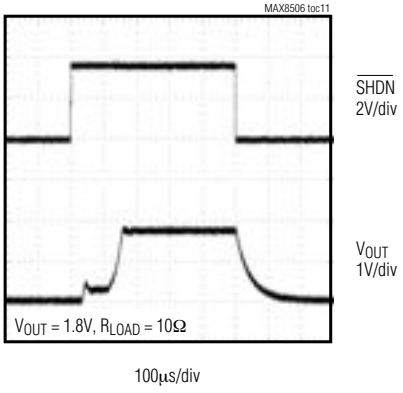
LIGHT-LOAD SWITCHING WAVEFORM IN PWM MODE



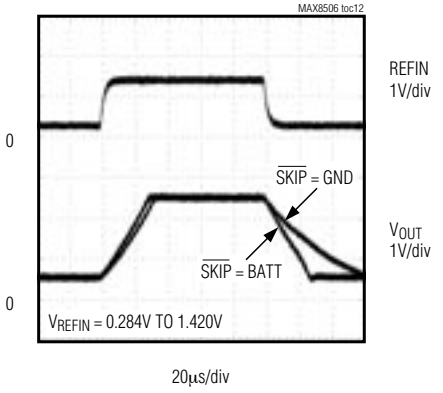
LIGHT-LOAD SWITCHING WAVEFORM IN NORMAL MODE



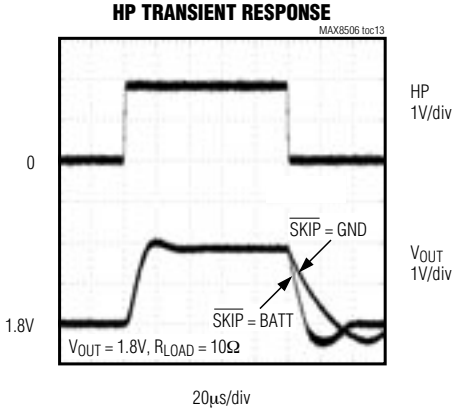
EXITING AND ENTERING SHUTDOWN



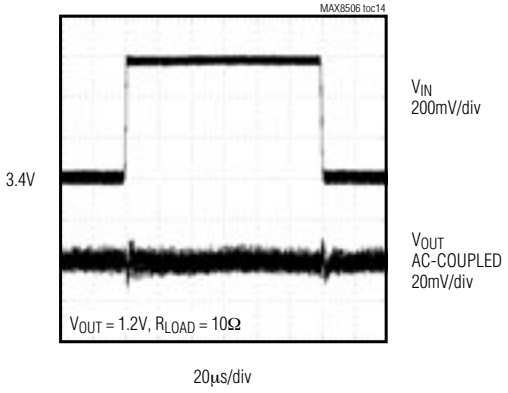
REFIN TRANSIENT RESPONSE



HP TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

Pin Description

PIN		NAME	FUNCTION
MAX8506 MAX8507	MAX8508		
1	1	$\overline{SHDN}$	Shutdown Control Input. Drive low for shutdown mode. Connect to BATT or logic high to enable the IC.
2	2	GND	Ground. Connect to PGND and directly to EP.
3	3	REF	Reference Output. Output of the internal 1.25V reference. Bypass to GND with a 0.22µF capacitor.
4	—	REFIN	External Reference Input. Connect to the output of a digital-to-analog converter for dynamic adjustment of the output voltage.
5	5	COMP	Compensation. Connect a compensation network from COMP to GND to stabilize the regulator. See the *Typical Application Circuits*.
6	6	HP	High-Power Bypass Control Input. Drive low for OUT to regulate to the voltage set by REFIN (MAX8506/MAX8507) or the external resistors on FB (MAX8508). Drive HP high for OUT to be connected to BATT by an internal bypass PFET.
7	7	N.C.	No Connection. Connect to PGND.
8	8	PGND	Power Ground. Connect to GND.
9	9	LX	Inductor Connection to the Drains of the Internal Power MOSFETs. LX is high impedance in shutdown mode.
10	10	BATTP	Supply Voltage Input. Connect to a 2.6V to 5.5V source. Bypass BATTP to PGND with a low-ESR 2.2µF capacitor. Connect BATTP to BATT.
11, 13, 15	11, 13, 15	BATT	Supply Voltage Input. Connect all BATT pins to BATTP.
12, 14	12, 14	OUT	Regulator Output. Connect both OUT pins directly to the output voltage.
16	16	$\overline{SKIP}$	Skip Control Input. Connect to GND or drive low to enable pulse skipping under light loads. Connect $\overline{SKIP}$ to BATT or logic high for forced-PWM mode.
—	4	FB	Output Feedback Sense Input. To set the output voltage, connect FB to the center of an external resistive voltage-divider between OUT and GND. FB voltage regulates to 0.75V when HP is low.
—	—	EP	Exposed Pad. Connect directly to GND underneath the IC.

Detailed Description

The MAX8506/MAX8507/MAX8508 PWM step-down DC-DC converters with integrated bypass PFET are optimized for low-voltage, battery-powered applications where high efficiency and small size are priorities. An analog control signal dynamically adjusts the MAX8506/MAX8507s' output voltage from 0.4V to 3.4V with a settling time of 30µs. The MAX8508 uses external feedback resistors to set the output voltage from 0.75V to 3.4V.

The MAX8506/MAX8507/MAX8508 operate at a high 1MHz switching frequency that reduces external component size. Each device includes an internal synchronous rectifier for high efficiency, which eliminates the need for an external Schottky diode. The normal operating mode uses constant-frequency PWM switching at medium and heavy loads and automatically pulse skips at light loads to reduce supply current and extend battery life. A forced-PWM mode switches at a constant frequency, regardless of load, to provide a well-controlled spectrum in noise-sensitive applications. Battery life is maximized by the low-dropout (75mΩ) high-power mode and a 0.1µA (typ) logic-controlled shutdown mode.

PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

PWM Control

The MAX8506/MAX8507/MAX8508 use a fixed-frequency, current-mode and PWM controller capable of achieving 100% duty cycle. Current-mode feedback provides cycle-by-cycle current limiting and superior load and line response, as well as overcurrent protection for the internal MOSFET and rectifier. A comparator at the P-channel MOSFET switch detects overcurrent at 1.25A.

During PWM operation, the MAX8506/MAX8507/MAX8508 regulate the output voltage by switching at a constant frequency and then modulating the duty cycle with PWM control. The error-amp output, the main switch current-sense signal, and the slope-compensation ramp are all summed using a PWM comparator. The comparator modulates the output power by adjusting the peak inductor current during the first half of each cycle based on the output-error voltage. The MAX8506/MAX8507/MAX8508 have relatively low AC loop gain coupled with a high-gain integrator to enable the use of a small and low-valued output filter capacitor. The resulting load regulation is 0.1% at 0 to 600mA.

Normal-Mode Operation

Connecting $\overline{SKIP}$ to GND enables normal operation. This allows automatic PWM control at medium and heavy loads and skip mode at light loads to improve efficiency and reduce quiescent current to 180µA. Operating in normal mode allows the MAX8506/MAX8507/MAX8508 to pulse skip when the peak inductor current drops below 90mA. During skip operation, the MAX8506/MAX8507/MAX8508 switch only as needed to service the load, reducing the switching frequency and associated losses in the internal switch and synchronous rectifier.

There are three steady-state operating conditions for the MAX8506/MAX8507/MAX8508 in normal mode:

1) The device performs in continuous conduction for heavy loads in a manner identical to forced-PWM mode. 2) The inductor current becomes discontinuous at medium loads, requiring the synchronous rectifier to be turned off before the end of a cycle as the inductor current reaches zero. 3) The device enters into skip mode when the converter output voltage exceeds its regulation limit before the inductor current reaches its skip threshold level.

During skip mode, a switching cycle initiates when the output voltage has dropped out of regulation. The P-channel MOSFET switch turns on and conducts current to the output-filter capacitor and load until the inductor current reaches the pulse-skipping current threshold. Then the main switch turns off and the magnetic field in the inductor collapses while current flows through the synchronous rectifier to the output filter capacitor and the load. The synchronous rectifier is turned off when the inductor current reaches zero. The MAX8506/MAX8507/MAX8508 wait until the skip comparator senses a low output voltage again.

Forced-PWM Operation

Connect $\overline{SKIP}$ to BATT for forced-PWM operation. Forced-PWM operation is desirable in sensitive RF and data-acquisition applications to ensure that switching harmonics do not interfere with sensitive IF and data-sampling frequencies. A minimum load is not required during forced-PWM operation since the synchronous rectifier passes reverse-inductor current as needed to allow constant-frequency operation with no load. Forced-PWM operation uses higher supply current with no load (1.75mA typ) compared to skip mode (180µA typ).

100% Duty-Cycle Operation and Dropout

The maximum on-time can exceed one internal oscillator cycle, which permits operation at 100% duty cycle. Near dropout, cycles can be skipped, reducing switching frequency. However, voltage ripple remains small because the current ripple is still low. As the input voltage drops even further, the duty cycle increases until the internal P-channel MOSFET stays on continuously. Dropout voltage at 100% duty cycle is the output current multiplied by the sum of the internal PMOS on-resistance (400mΩ typ) and the inductor resistance. For lower dropout, use the high-power bypass mode (75mΩ typ).

High-Power Bypass Mode

A high-power bypass mode is available for use when a PA transmits at high power. This mode connects OUT to BATT through the bypass PFET. Additionally, the PWM buck converter is forced into 100% duty cycle to further reduce dropout. The dropout in the bypass PFET equals the load current multiplied by the on-resistance (75Ω typ) in parallel with the buck converter and inductor dropout resistance.

Undervoltage Lockout (UVLO)

The MAX8506/MAX8507/MAX8508 do not operate with battery voltages below the UVLO threshold of 2.35V (typ). The output remains off until the supply voltage exceeds the UVLO threshold. This guarantees the integrity of the output voltage regulation.

PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

Synchronous Rectification

An N-channel synchronous rectifier operates during the second half of each switching cycle (off-time). When the inductor current falls below the N-channel current-comparator threshold or when the PWM reaches the end of the oscillator period, the synchronous rectifier turns off. This prevents reverse current from the output to the input in pulse-skipping mode. During PWM operation, the NEGLIM threshold adjusts to permit reverse current during light loads. This allows regulation with a constant switching frequency and eliminates minimum load requirements for fixed-frequency operation.

Shutdown Mode

Drive $\overline{SHDN}$ to GND to place the MAX8506/MAX8507/MAX8508 in shutdown mode. In shutdown, the reference, control circuitry, internal switching MOSFET, and synchronous rectifier turn off and the output becomes high impedance. Input current falls to 0.1µA (typ) during shutdown mode. Drive $\overline{SHDN}$ high to enable the IC.

Current-Sense Comparators

The MAX8506/MAX8507/MAX8508 use several internal current-sense comparators. In PWM operation, the PWM comparator terminates the cycle-by-cycle on-time and provides improved load and line response. A second current-sense comparator used across the P-channel switch controls entry into skip mode. A third current-sense comparator monitors current through the internal N-channel MOSFET to prevent excessive reverse currents and determine when to turn off the synchronous rectifier. A fourth comparator used at the P-channel MOSFET detects overcurrent. A fifth comparator used at the bypass P-channel MOSFET detects overcurrent in the HP mode or at dropout. This protects the system, external components, and internal MOSFETs under overload conditions.

Applications Information

Setting the Output Voltage

Using a DAC (MAX8506/MAX8507)

The MAX8506/MAX8507 are optimized for highest system efficiency when applying power to a linear PA in CDMA handsets. When transmitting at less than full power, the supply voltage to the PA is lowered in many steps from 3.4V to as low as 0.4V to greatly reduce battery current (see the *Typical Application Circuits*). The use of DC-DC converters such as the MAX8506/MAX8507 dramatically extends talk time in these applications.

The MAX8506/MAX8507s' output voltage is dynamically adjustable from 0.4V to 3.4V by the use of the REFIN input. The gain from V_{REFIN} to V_{OUT} is internally set to 1.76 (MAX8506) or 2.00 (MAX8507). V_{OUT} can be adjusted during operation by driving REFIN with an external DAC. The MAX8506/MAX8507 output responds to full-scale change in voltage and current in less than 30µs.

Using External Divider (MAX8508)

The MAX8508 is intended for two-step V_{CC} control applications where high efficiency is a priority. Select an output voltage between 0.75V and 3.4V by connecting FB to a resistive-divider between the output and GND (see the MAX8508 *Typical Application Circuit*). Select feedback resistor R2 in the 5kΩ to 50kΩ range. R1 is then given by:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.75V.

Input Capacitor Selection

Capacitor ESR is a major contributor to input ripple in high-frequency DC-DC converters. Ordinary aluminum-electrolytic capacitors have high ESR and should be avoided. Low-ESR tantalum or polymer capacitors are better and provide a compact solution for space-constrained surface-mount designs. Ceramic capacitors have the lowest overall ESR.

The input filter capacitor reduces peak currents and noise at the input voltage source. Connect a low-ESR bulk capacitor (2.2µF to 10µF) to the input. Select this bulk capacitor to meet the input ripple requirements and voltage rating rather than capacitance value. Use the following equation to calculate the maximum RMS input current:

$$I_{RMS} = \frac{I_{OUT}}{V_{IN}} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}$$

Compensation, Stability, and Output Capacitor

The MAX8506/MAX8507/MAX8508 are externally compensated by placing a resistor and a capacitor (see the *Typical Application Circuits*, R_C and C_C) in series from COMP to GND. An additional capacitor (C_f) may be required from COMP to GND if high-ESR output capacitors are used. The C_C capacitor integrates the current from the transimpedance amplifier, averaging output

Table 1. Suggested Inductors

SUPPLIER	PART NUMBER	INDUCTANCE (µH)	ESR (mΩ)	SATURATION CURRENT (A)	DIMENSIONS (mm)
Murata	LQH32C-53	4.7	150	0.650	2.5 x 3.2 x 1.7
Sumida	CDRH2D11	4.7	135	0.500	3.2 x 3.2 x 1.2
Taiyo Yuden	LBLQ2016	4.7	250	0.210	1.6 x 2.0 x 1.6
TOKO	D312C	4.7	200	0.790	3.6 x 3.6 x 1.2

capacitor ripple. This sets the device speed for transient response and allows the use of small ceramic output capacitors because the phase-shifted capacitor ripple does not disturb the current-regulation loop. The resistor sets the proportional gain of the output error voltage by a factor of $g_m \times R_C$. Increasing this resistor also increases the sensitivity of the control loop to output ripple.

The resistor and capacitor set a compensation zero that defines the system's transient response. The load creates a dynamic pole, shifting in frequency with changes in load. As the load decreases, the pole frequency shifts to the left. System stability requires that the compensation zero must be placed to ensure adequate phase margin (at least 30° at unity gain). With a 4.7µF output capacitor, the recommended C_C and R_C for the MAX8506 are 1500pF and 10kΩ, respectively. This provides adequate phase margin over the entire output voltage and load range and optimizes the output-voltage settling time for REFIN dynamic control. See the *Typical Application Circuits* for recommended C_C and R_C values for the MAX8507 and MAX8508.

Inductor Selection

A 4µH to 6µH inductor is recommended for most applications. For best efficiency, the inductor's DC resistance should be <400mΩ. Saturation current (I_{SAT}) should be greater than the maximum DC load at the PA's supply plus half the inductor current ripple. Two-step V_{CC} applications typically require very small inductors with I_{SAT} in the 200mA to 300mA region. See Tables 1 and 2 for recommended inductors and suppliers.

PC Board Layout and Routing

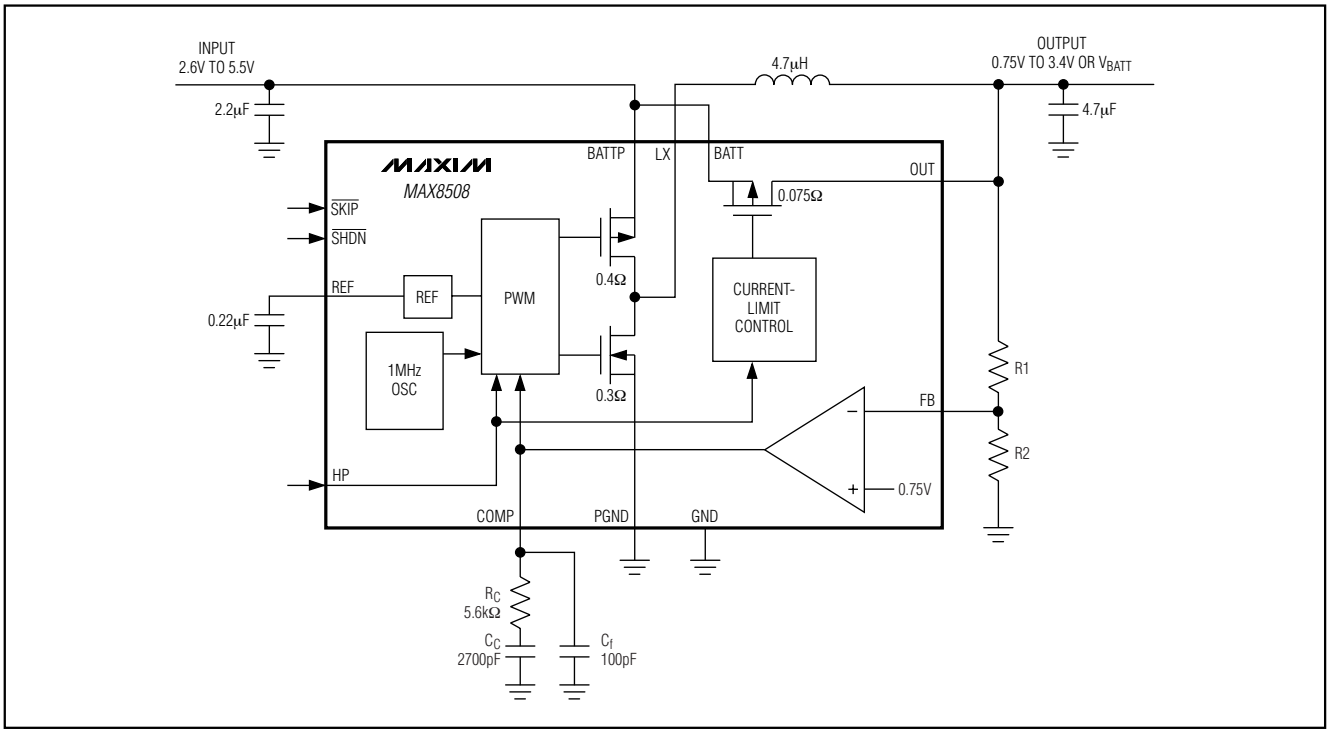
Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata	770-436-1300	www.murata.com
Sumida	847-956-0666	www.sumida.com
Taiyo Yuden	408-573-4150	www.t-yuden.com
TOKO	847-297-0070	www.tokoam.com

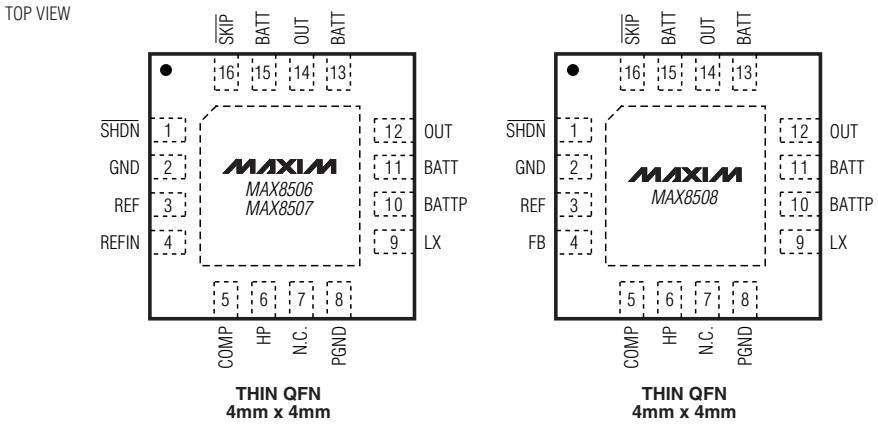
High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes EMI, noise on the feedback paths, and voltage gradients in the ground plane, all of which can result in instability or regulation errors. Connect the inductor, input filter capacitor, and output filter capacitor as close together as possible and keep their traces short, direct, and wide. The external voltage- feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces, such as those from the LX pin, away from the voltage-feedback network. Position the bypass capacitors as close as possible to their respective supply and ground pins to minimize noise coupling. For optimum performance, place input and output capacitors as close to the device as possible. Connect GND directly under the IC to the exposed paddle. Refer to the MAX8506 evaluation kit for an example PC board layout and routing scheme.

PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

Typical Application Circuits (MAX8508) (continued)



Pin Configurations



Chip Information

TRANSISTOR COUNT: 2020

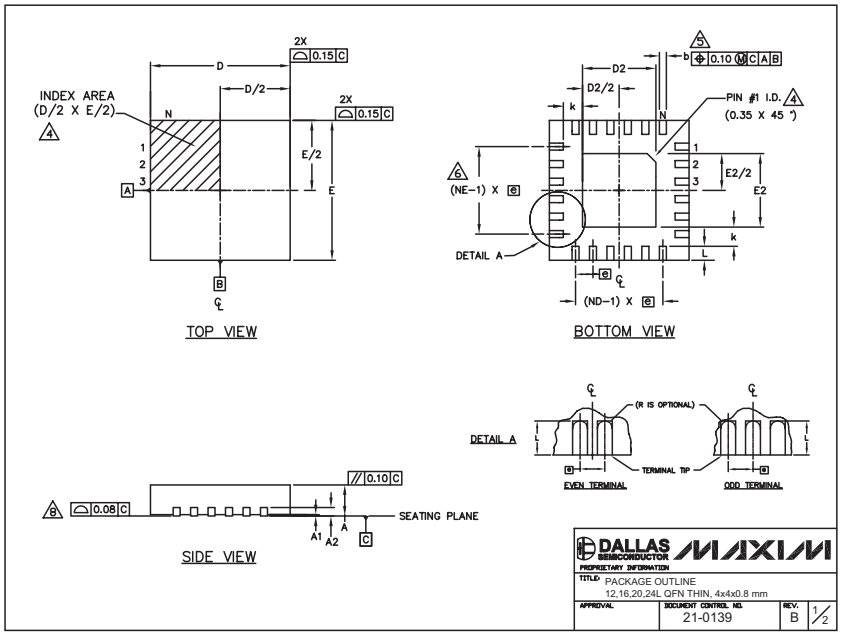
PROCESS: BiCMOS

PWM Step-Down DC-DC Converters with 75mΩ Bypass FET for WCDMA and cdmaOne Handsets

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. B | 1/2

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. B | 2/2