RELIABILITY REPORT

FOR

MAX8561ETA

PLASTIC ENCAPSULATED DEVICES

September 24, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX8561 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8561 step-down dc-dc converter is optimized for applications that prioritize small size and high efficiency. It utilizes a proprietary hysteretic-PWM control scheme that switches with fixed frequency and is adjustable up to 4MHz, allowing customers to trade efficiency for smaller external components. Output current is guaranteed up to 500mA, while quiescent current is only 40µA (typ).

Internal synchronous rectification greatly improves efficiency and eliminates the external Schottky diode required in conventional step-down converters. Built-in soft-start eliminates inrush current to reduce input capacitor requirements. The MAX8561 features logic-controlled output voltage.

The MAX8561 is available in space-saving 8-pin 3mm x 3mm Thin DFN packages.

B. Absolute Maximum Ratings

Item	Rating
IN, FB, SHDN, ODI, ODO to GND	-0.3V to +6V
LX to GND (Note 1)	-0.3V to (VIN + 0.3V)
PGND to GND	-0.3V to +0.3V
LX Current	1.27A
Output Short Circuit to GND (typical operating circuit)	10s
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin Thin DFN (3 x 3)	1951mW
Derates above +70°C	
8-Pin Thin DFN (3 x 3)	24.4mW/°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

II. Manufacturing Information

A. Description/Function: 4MHz, 500mA Synchronous Step-Down DC-DC Converters in SOT and TDFN

B. Process: B8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 1271

D. Fabrication Location: California, USA

E. Assembly Location: Thailand

F. Date of Initial Production: July, 200

III. Packaging Information

A. Package Type: **8-Pin Thin DFN**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epxoy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-9000-0685

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 40 x 59 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

B.

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$

$\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6205) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PN18-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8561ETA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

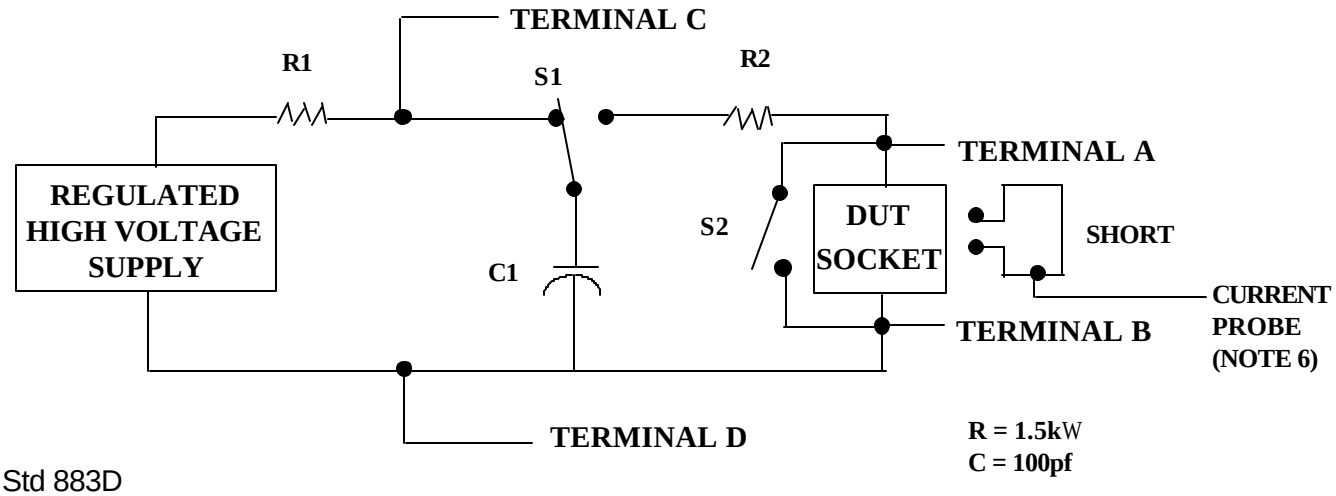
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

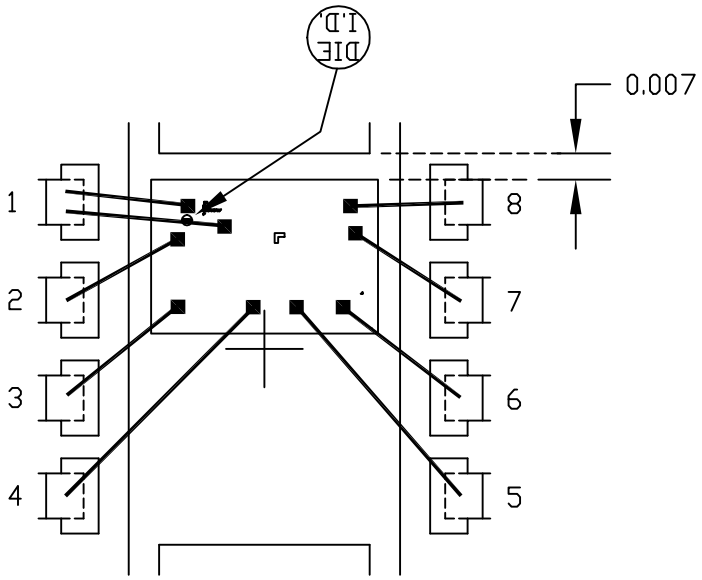
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



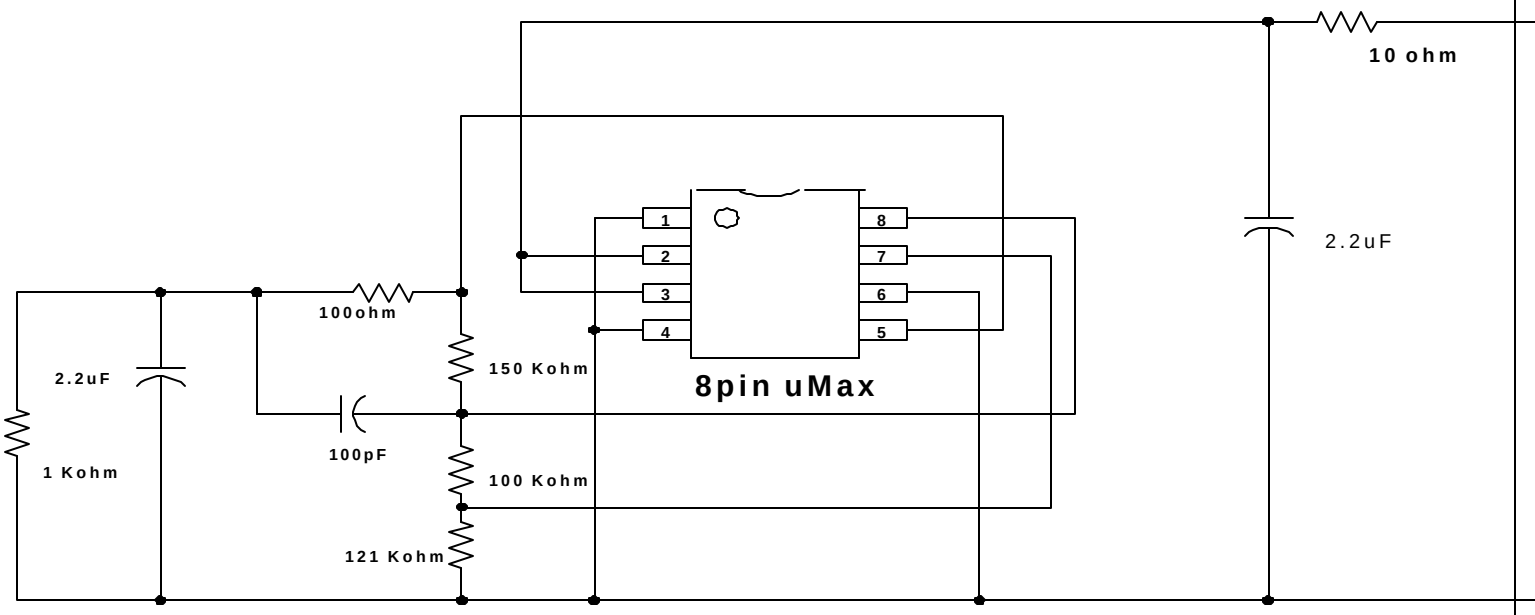
Mil Std 883D
Method 3015.7
Notice 8

3x3x0.8 MM QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T833-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71×102	PKG.			BOND DIAGRAM #: 05-9000-0685	REV: A
	DESIGN				

ONCE PER SOCKET



DEVICES: MAX8560/61/62 PN18 (Burn-In Board)
MAX. EXPECTED CURRENT = 5 mA (+5V)

DRAWN BY: Ge Gan
NOTES: This section to list different m
on die types, as well as special instruct

DOCUMENT I.D. 06-6205	REVISION A	*MAXIM* TITLE: **BI Circuit (MAX8560/8561/8562) PN18**