APPLICATION DEVELOPMENT SYSTEM
AVAILABLE
AN99 • AN115 • AN124 •AN133 • AN134 • AN135

Single Supply / Low Power / 256-tap / SPI bus

# X9251

## Quad Digitally-Controlled (XDCP™) Potentiometer

### FEATURES

- Four potentiometers in one package
- 256 resistor taps–0.4% resolution
- SPI Serial Interface for write, read, and transfer operations of the potentiometer
- Wiper resistance: 100Ω typical @ $V_{CC}$ = 5V
- 4 Non-volatile data registers for each potentiometer
- Non-volatile storage of multiple wiper positions
- Standby current < 5µA max
- $V_{CC}$: 2.7V to 5.5V Operation
- 50KΩ, 100KΩ versions of total resistance
- 100 yr. data retention
- Single supply version of X9250
- Endurance: 100,000 data changes per bit per register
- 24-lead SOIC, 24-lead TSSOP, 24-lead CSP (Chip Scale Package)
- Low power CMOS

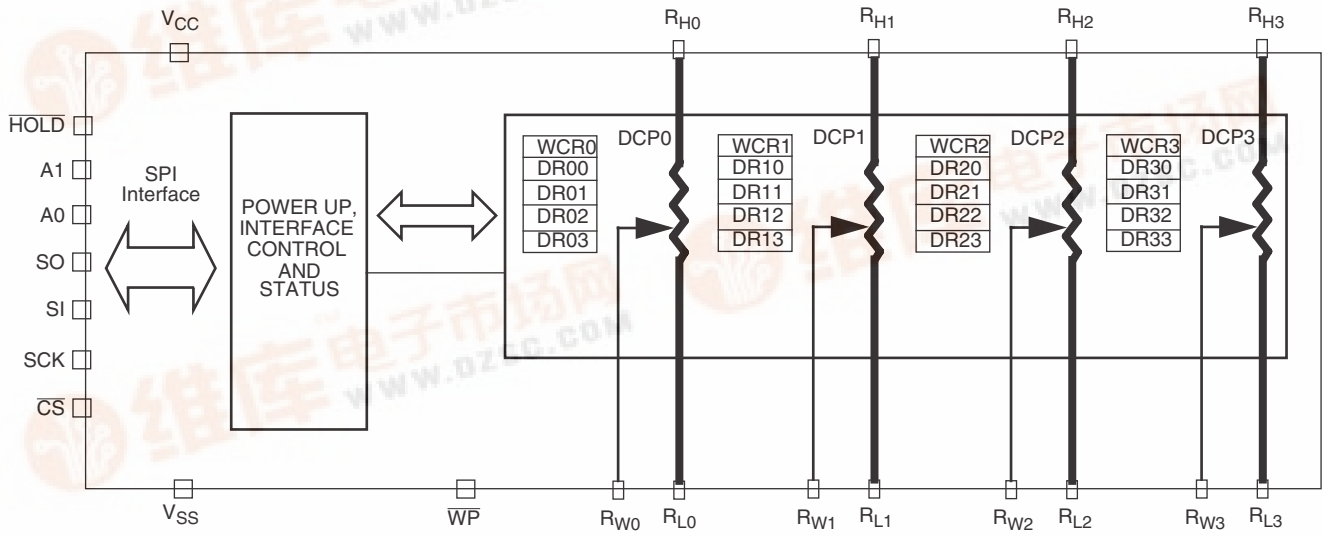
### DESCRIPTION

The X9251 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four non-volatile Data Registers that can be directly written to and read by the user. The content of the WCR controls the position of the wiper. At power-up, the device recalls the content of the default Data Registers of each DCP (DR00, DR10, DR20, and DR30) to the corresponding WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

### FUNCTIONAL DIAGRAM



## ORDERING INFO

| Ordering Number | Potentiomenter Organization | Package | Operating Temperature Range | $V_{CC}$ Limits |
|---|---|---|---|---|
| X9251US24 | 50kΩ | 24-lead SOIC | 0°C to 70°C | 5V±10% |
| X9251US24-2.7 | 50kΩ | 24-lead SOIC | 0°C to 70°C | 2.7 to 5.5V |
| X9251US24I | 50kΩ | 24-lead SOIC | -40°C to +85°C | 5V±10% |
| X9251US24I-2.7 | 50kΩ | 24-lead SOIC | -40°C to +85°C | 2.7 to 5.5V |
| X9251UV24 | 50kΩ | 24-lead TSSOP | 0°C to 70°C | 5V±10% |
| X9251UV24-2.7 | 50kΩ | 24-lead TSSOP | 0°C to 70°C | 2.7 to 5.5V |
| X9251UV24I | 50kΩ | 24-lead TSSOP | -40°C to +85°C | 5V±10% |
| X9251UV24I-2.7 | 50kΩ | 24-lead TSSOP | -40°C to +85°C | 2.7 to 5.5V |
| X9251UB24 | 50kΩ | 24-lead CSP | 0°C to 70°C | 5V±10% |
| X9251UB24-2.7 | 50kΩ | 24-lead CSP | 0°C to 70°C | 2.7 to 5.5V |
| X9251UB24I | 50kΩ | 24-lead CSP | -40°C to +85°C | 5V±10% |
| X9251UB24I-2.7 | 50kΩ | 24-lead CSP | -40°C to +85°C | 2.7 to 5.5V |
| X9251TS24 | 100kΩ | 24-lead SOIC | 0°C to 70°C | 5V±10% |
| X9251TS24-2.7 | 100kΩ | 24-lead SOIC | 0°C to 70°C | 2.7 to 5.5V |
| X9251TS24I | 100kΩ | 24-lead SOIC | -40°C to +85°C | 5V±10% |
| X9251TS24I-2.7 | 100kΩ | 24-lead SOIC | -40°C to +85°C | 2.7 to 5.5V |
| X9251TV24 | 100kΩ | 24-lead TSSOP | 0°C to 70°C | 5V±10% |
| X9251TV24-2.7 | 100kΩ | 24-lead TSSOP | 0°C to 70°C | 2.7 to 5.5V |
| X9251TV24I | 100kΩ | 24-lead TSSOP | -40°C to +85°C | 5V±10% |
| X9251TV24I-2.7 | 100kΩ | 24-lead TSSOP | -40°C to +85°C | 2.7 to 5.5V |
| X9251TB24 | 100kΩ | 24-lead CSP | 0°C to 70°C | 5V±10% |
| X9251TB24-2.7 | 100kΩ | 24-lead CSP | 0°C to 70°C | 2.7 to 5.5V |
| X9251TB24I | 100kΩ | 24-lead CSP | -40°C to +85°C | 5V±10% |
| X9251TB24I-2.7 | 100kΩ | 24-lead CSP | -40°C to +85°C | 2.7 to 5.5V |

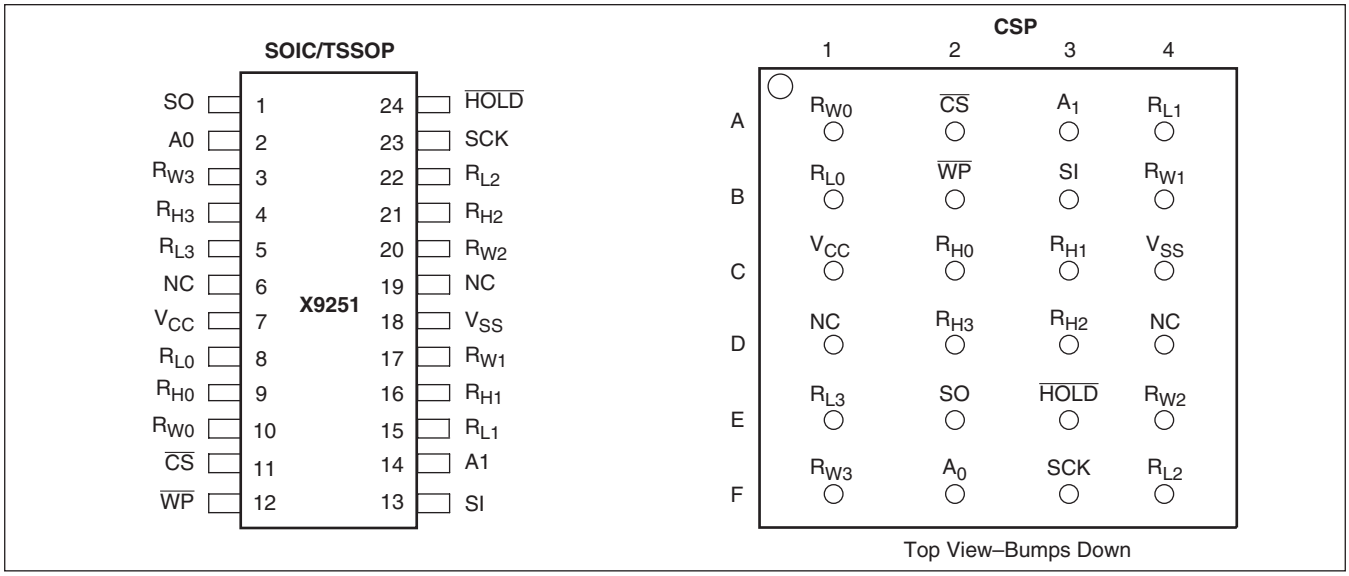
## CIRCUIT LEVEL APPLICATIONS

- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

## SYSTEM LEVEL APPLICATIONS

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

## PIN CONFIGURATION




## PIN ASSIGNMENTS

| Pin (SOIC) | Pin (CSP) | Symbol | Function |
|---|---|---|---|
| 1 | E2 | SO | Serial Data Output for SPI bus |
| 2 | F2 | A0 | Device Address for SPI bus. (See Note 1) |
| 3 | F1 | $R_{W3}$ | Wiper Terminal of DCP3 |
| 4 | D2 | $R_{H3}$ | High Terminal of DCP3 |
| 5 | E1 | $R_{L3}$ | Low Terminal of DCP3 |
| 7 | C1 | $V_{CC}$ | System Supply Voltage |
| 8 | B1 | $R_{L0}$ | Low Terminal of DCP0 |
| 9 | C2 | $R_{H0}$ | High Terminal of DCP0 |
| 10 | A1 | $R_{W0}$ | Wiper Terminal of DCP0 |
| 11 | A2 | $\overline{CS}$ | SPI bus. Chip Select active low input |
| 12 | B2 | $\overline{WP}$ | Hardware Write Protect – active low |
| 13 | B3 | SI | Serial Data Input for SPI bus |
| 14 | A3 | A1 | Device Address for SPI bus. (See Note 1) |
| 15 | A4 | $R_{L1}$ | Low Terminal of DCP1 |
| 16 | C3 | $R_{H1}$ | High Terminal of DCP1 |
| 17 | B4 | $R_{W1}$ | Wiper Terminal of DCP1 |
| 18 | C4 | $V_{SS}$ | System Ground |
| 20 | E4 | $R_{W2}$ | Wiper Terminal of DCP2 |
| 21 | D3 | $R_{H2}$ | High Terminal of DCP2 |
| 22 | F4 | $R_{L2}$ | Low Terminal of DCP2 |
| 23 | F3 | SCK | Serial Clock for SPI bus |
| 24 | E3 | $\overline{HOLD}$ | Device select. Pauses the SPI serial bus. |
| 6, 19 | D1, D4 | NC | No Connect |

**Note 1:** A0–A1 device address pins must be tied to a logic level.

## PIN DESCRIPTIONS

### Bus Interface Pins

#### Serial Output (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

#### Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the device registers are input on this pin. Data is latched by the rising edge of the serial clock.

#### Serial Clock (SCK)

The SCK input is used to clock data into and out of the X9251.

#### Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

#### Device Address (A1–A0)

The address inputs are used to set the two least significant bits of the slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9251. Device pins A1-A0 must be tie to a logic level which specify the internal address of the device, see Figures 2, 3, 4, 5 and 6.

#### Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9251 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device is in the standby state. $\overline{CS}$ LOW enables the X9251, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

### Potentiometer Pins

#### $R_H$, $R_L$

The $R_H$ and $R_L$ pins are equivalent to the terminal connections on a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of $R_H$ and $R_L$ such that $R_{H0}$ and $R_{L0}$ are the terminals of DCP0 and so on.

#### $R_W$

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of $R_W$ such that $R_{W0}$ is the terminals of DCP0 and so on.

### Supply Pins

#### System Supply Voltage ($V_{CC}$) and Supply Ground ($V_{SS}$)

The $V_{CC}$ pin is the system supply voltage. The $V_{SS}$ pin is the system ground.

### Other Pins

#### No Connect

No connect pins should be left floating. This pins are used for Xicor manufacturing and testing purposes.

#### Hardware Write Protect Input ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents non-volatile writes to the Data Registers.

## PRINCIPLES OF OPERATION

The X9251 is an integrated circuit incorporating four DCPs and their associated registers and counters, and a serial interface providing direct communication between a host and the potentiometers.

### DCP Description

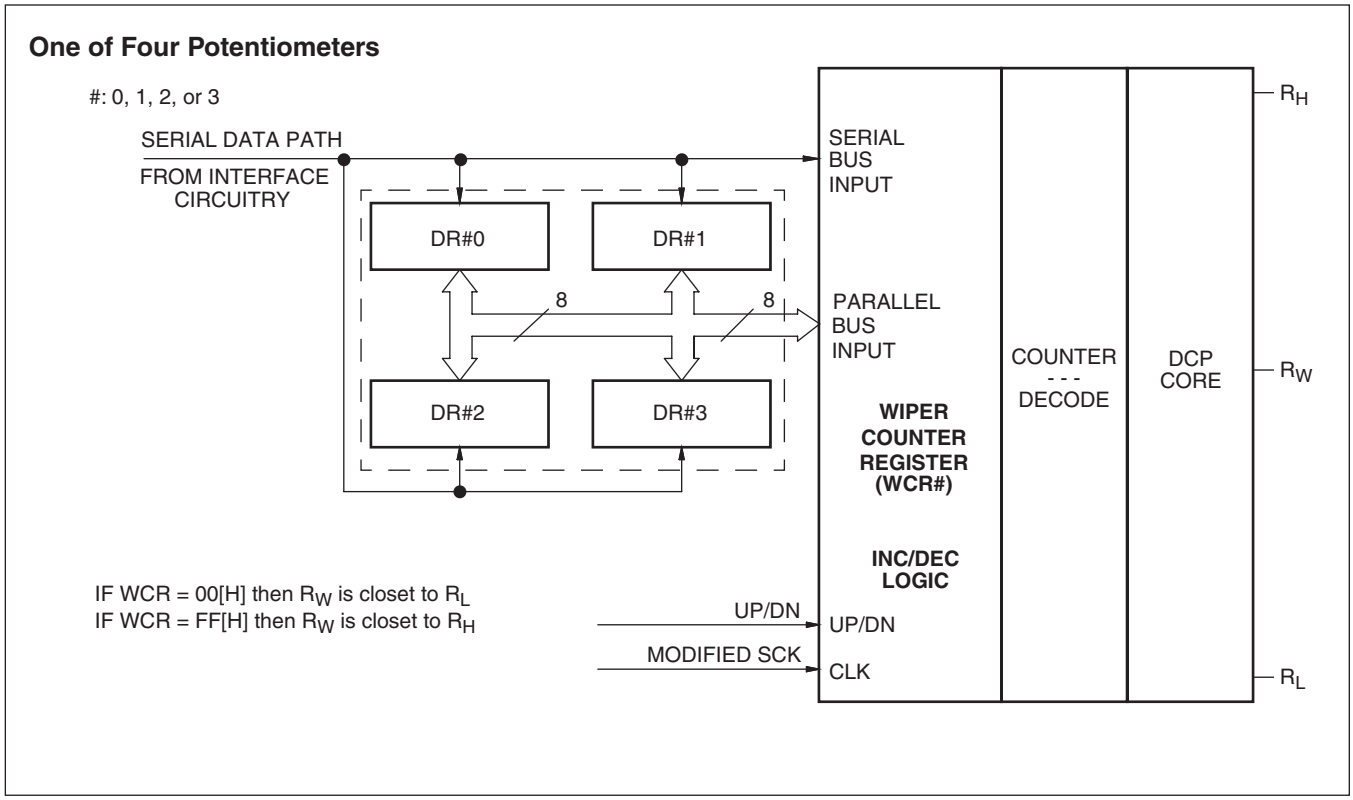
Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer ($R_H$ and $R_L$ pins). The RW pin is an intermediate node, equivalent to the wiper terminal of a mechanical potentiometer.

The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Counter Register (WCR).

### Power Up and Down Recommendations.

There are no restrictions on the power-up or power-down conditions of $V_{CC}$ and the voltages applied to the potentiometer pins provided that $V_{CC}$ is always more positive than or equal to $V_H$, $V_L$, and $V_W$, i.e., $V_{CC} \geq V_H$, $V_L$, $V_W$. The $V_{CC}$ ramp rate specification is always in effect.

**Figure 1. Detailed Potentiometer Block Diagram**



### Wiper Counter Register (WCR)

The X9251 contains four Wiper Counter Registers, one for each potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 wiper positions along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (see Instruction section for more details). Finally, it is loaded with the contents of its Data Register zero (DR#0) upon power-up. (See Figure 1.)

The wiper counter register is a volatile register; that is, its contents are lost when the X9251 is powered-down. Although the register is automatically loaded with the value in DR#0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR#0 value into the WCR#.

### Data Registers (DR)

Each of the four DCPs has four 8-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a non-volatile operation and takes a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bits [7:0] are used to store one of the 256 wiper positions or data (0~255).

### Status Register (SR)

This 1-bit Status Register is used to store the system status.

WIP: Write In Progress status bit, read only.

– When WIP=1, indicates that high-voltage write cycle is in progress.

– When WIP=0, indicates that no high-voltage write cycle is in progress.

**Table 1. Wiper counter Register, WCR (8-bit), WCR[7:0]:** Used to store the current wiper position (Volatile).

| WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 |
|---|---|---|---|---|---|---|---|
| (MSB) | | | | | | | (LSB) |

**Table 2. Data Register, DR (8-bit), DR[7:0]:** Used to store wiper positions or data (Non-volatile).

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| (MSB) | | | | | | | (LSB) |

## SERIAL INTERFACE

The X9251 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in, on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

### Identification Byte

The first byte sent to the X9251 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification Byte. The most significant four bits of the Identification Byte are a Device Type Identifier, ID[3:0]. For the X9251, this is fixed as 0101 (refer to Table 3).

The least significant four bits of the Identification Byte are the Slave Address bits, AD[3:0]. For the X9251, A3 is 0, A2 is 0, A1 is the logic value at the input pin A1, and A0 is the logic value at the input pin A0. Only the device which Slave Address matches the incoming bits sent by the master executes the instruction. The A1 and A0 inputs can be actively driven by CMOS input signals or tied to $V_{CC}$ or $V_{SS}$.

### Instruction Byte

The next byte sent to the X9251 contains the instruction and register pointer information. The four most significant bits are used provide the instruction opcode (I[3:0]). The RB and RA bits point to one of the four Data Registers of each associated XDCP. The least two significant bits point to one of four Wiper Counter Registers or DCPs.The format is shown below in Table 4.

**Table 3. Identification Byte Format**

| | Device Type Identifier | | | | Slave Address | | | |
|---|---|---|---|---|---|---|---|---|
| | ID3 | ID2 | ID1 | ID0 | A3 | A2 | A1 | A0 |
| | 0 | 1 | 0 | 1 | 0 | 0 | Pin A1 Logic Value | Pin A0 Logic Value |
| | (MSB) | | | | | | | (LSB) |

**Table 4. Instruction Byte Format**

| | Instruction Opcode | | | | Register Selection | | DCP Selection (WCR Selection) | |
|---|---|---|---|---|---|---|---|---|
| | I3 | I2 | I1 | I0 | RB | RA | P1 | P0 |
| | (MSB) | | | | | | | (LSB) |

**Data Register Selection**

| Register | RB | RA |
|---|---|---|
| DR#0 | 0 | 0 |
| DR#1 | 0 | 1 |
| DR#2 | 1 | 0 |
| DR#3 | 1 | 1 |

#: 0, 1, 2, or 3

**Table 5. Instruction Set**

| Instruction | Instruction Set | | | | | | | | Operation |
|---|---|---|---|---|---|---|---|---|---|
| | I3 | I2 | I1 | I0 | RB | RA | P1 | P0 | |
| Read Wiper Counter Register | 1 | 0 | 0 | 1 | 0 | 0 | 1/0 | 1/0 | Read the contents of the Wiper Counter Register pointed to by P1-P0 |
| Write Wiper Counter Register | 1 | 0 | 1 | 0 | 0 | 0 | 1/0 | 1/0 | Write new value to the Wiper Counter Register pointed to by P1-P0 |
| Read Data Register | 1 | 0 | 1 | 1 | 1/0 | 1/0 | 1/0 | 1/0 | Read the contents of the Data Register pointed to by P1-P0 and RB-RA |
| Write Data Register | 1 | 1 | 0 | 0 | 1/0 | 1/0 | 1/0 | 1/0 | Write new value to the Data Register pointed to by P1-P0 and RB-RA |
| XFR Data Register to Wiper Counter Register | 1 | 1 | 0 | 1 | 1/0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the Data Register pointed to by P1-P0 and RB-RA to its associated Wiper Counter Register |
| XFR Wiper Counter Register to Data Register | 1 | 1 | 1 | 0 | 1/0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the Wiper Counter Register pointed to by P1-P0 to the Data Register pointed to by RB-RA |
| Global XFR Data Registers to Wiper Counter Registers | 0 | 0 | 0 | 1 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of the Data Registers pointed to by RB-RA of all four pots to their respective Wiper Counter Registers |
| Global XFR Wiper Counter Registers to Data Register | 1 | 0 | 0 | 0 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by RB-RA of all four pots |
| Increment/Decrement Wiper Counter Register | 0 | 0 | 1 | 0 | 0 | 0 | 1/0 | 1/0 | Enable Increment/decrement of the Control Latch pointed to by P1-P0 |

**Note:** 1/0 = data is one or zero

### Instructions

Four of the nine instructions are three bytes in length. These instructions are:

– **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer,

– **Write Wiper Counter Register** – change current wiper position of the selected potentiometer,

– **Read Data Register** – read the contents of the selected Data Register,

– **Write Data Register** – write a new value to the selected Data Register,

– **Read Status** – this command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The basic sequence of the three byte instructions is illustrated in Figure 3. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action is delayed by $t_{WRL}$. A transfer from the WCR (current wiper position), to a Data Register is a write to non-volatile memory and takes a minimum of $t_{WR}$ to complete. The transfer can occur between one of the four potentiometer's WCR, and one of its associated registers, DRs; or it may occur globally, where the transfer occurs between all potentiometers and one associated register. The Read Status Register instruction is the only unique format (see Figure 5).

Four instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9251; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

– **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.

– **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.

– **Global XFR Data Register to Wiper Counter Register** – This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.

– **Global XFR Wiper Counter Register to Data Register** – This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

### INCREMENT/DECREMENT COMMAND

The final command is Increment/Decrement (see Figures 6 and 7). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9251 has responded with an Acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCK clock pulse ($t_{HIGH}$) while SI is HIGH, the selected wiper moves one wiper position towards the $R_H$ terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper moves one wiper position towards the $R_L$ terminal. A detailed illustration of the sequence and timing for this operation are shown. See Instruction format for more details.

**Figure 2. Two-Byte Instruction Sequence**

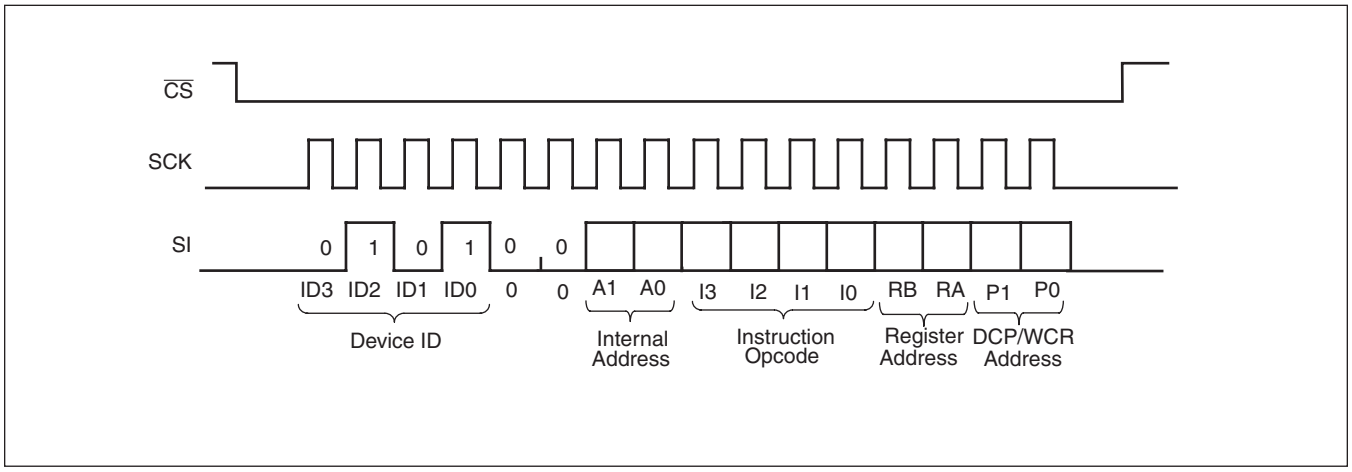



**Figure 3. Three-Byte Instruction Sequence SPI Interface; Write Case**

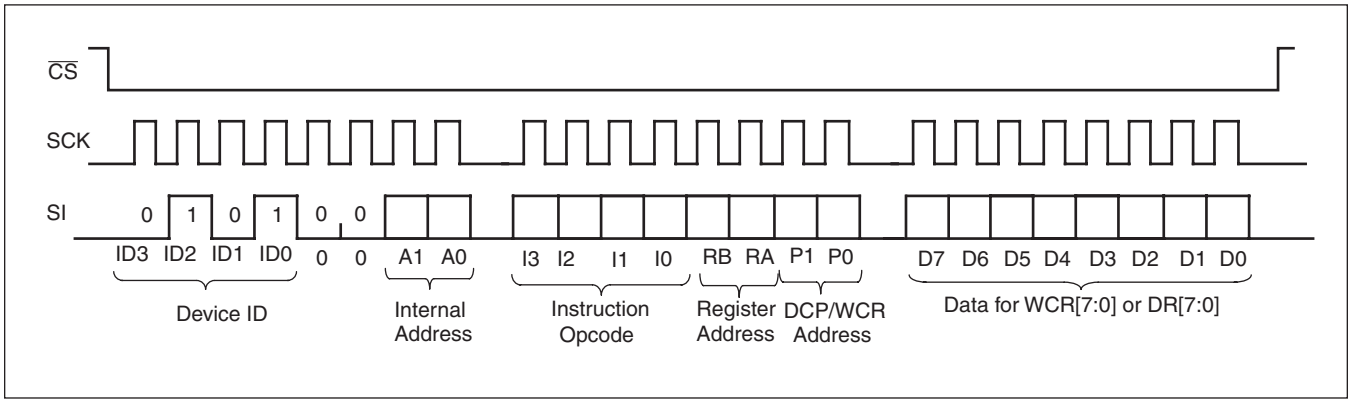



**Figure 4. Three-Byte Instruction Sequence SPI Interface, Read Case**

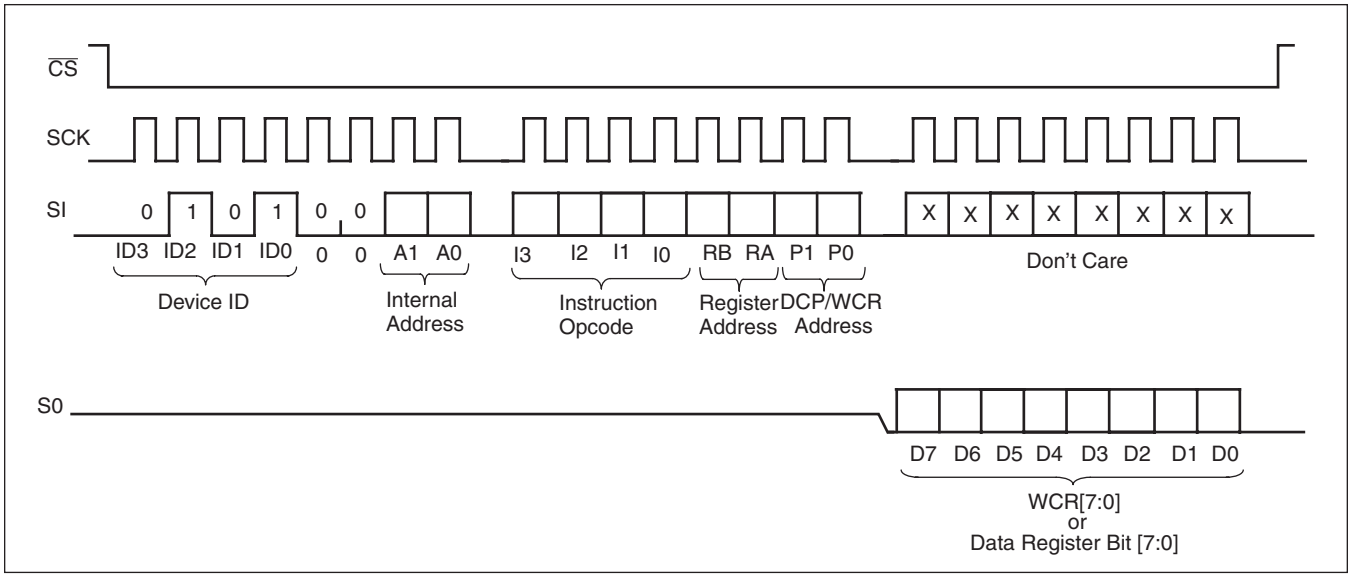


**Figure 5. Three-Byte Instruction Sequence (Read Status Register)**

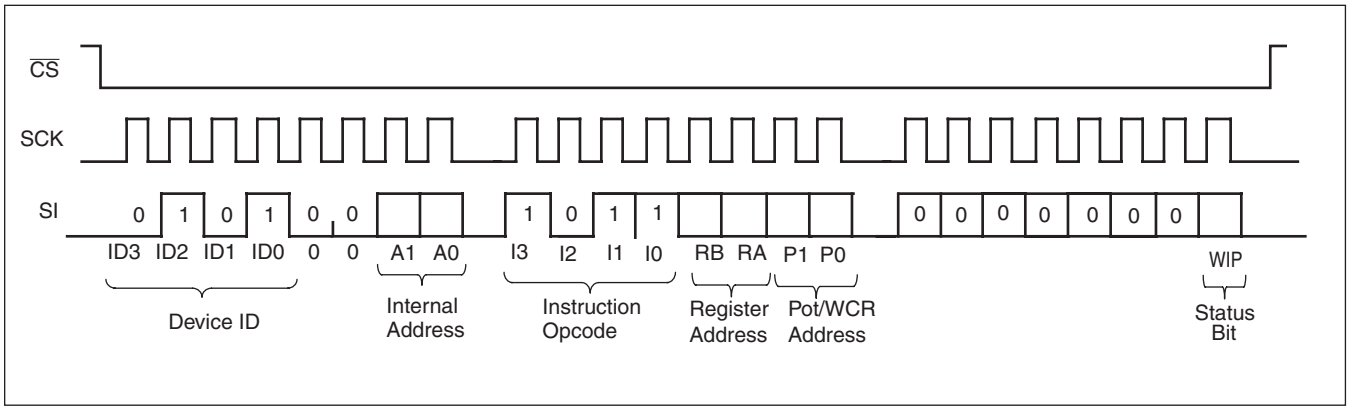



**Figure 6. Increment/Decrement Instruction Sequence**

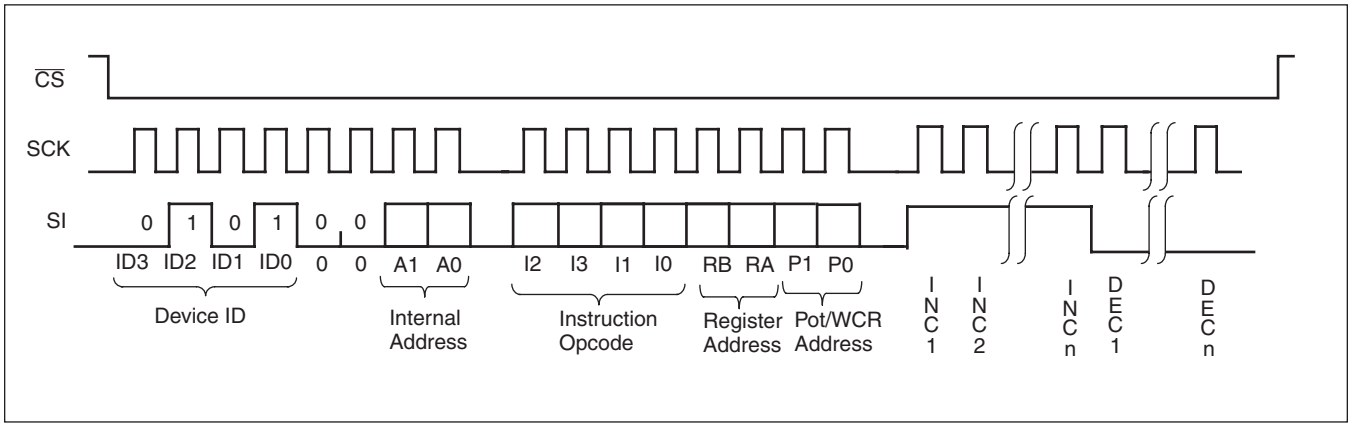
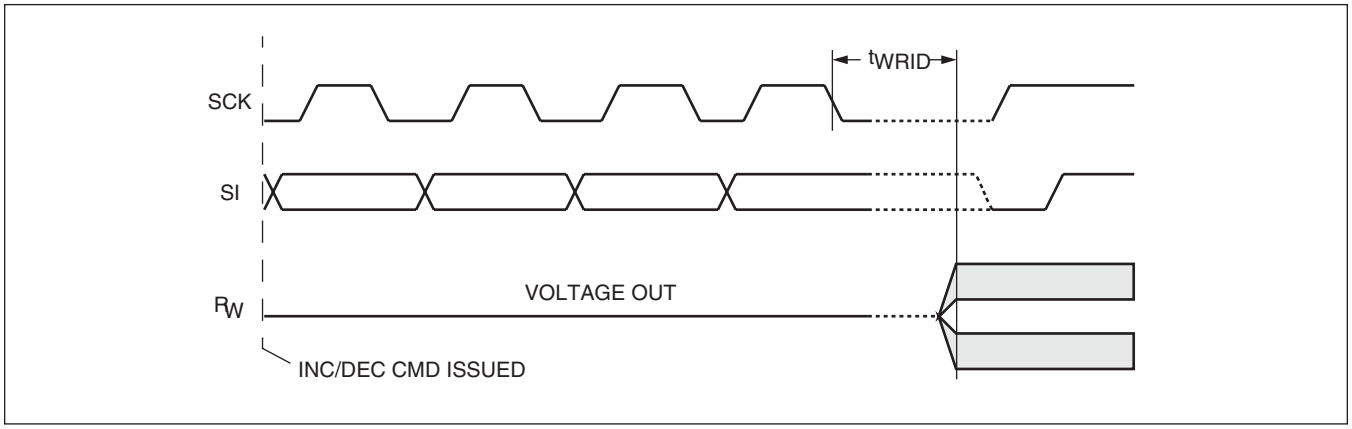



**Figure 7. Increment/Decrement Timing Spec**



## INSTRUCTION FORMAT

### Read Wiper Counter Register (WCR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Wiper Position (Sent by X9251 on SO) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 | |

### Write Wiper Counter Register (WCR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Data Byte (Sent by Host on SI) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 | |

### Read Data Register (DR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | Data Byte (Sent by X9271 on SO) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 1 | 1 | RB | RA | P1 | P0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

### Write Data Register (DR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | Data Byte (Sent by Host on SI) | | | | | | | | $\overline{CS}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 0 | 0 | RB | RA | P1 | P0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |

### Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR Addresses | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 0 | 0 | 1 | RB | RA | 0 | 0 | |

**Notes:** (1) "A1 ~ A0": stands for the device addresses sent by the master.
(2) WPx refers to wiper position data in the Counter Register
(2) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).
(3) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

### Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR Addresses | | | | $\overline{CS}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 0 | 0 | RB | RA | 0 | 0 | | |

### Transfer Wiper Counter Register (WCR) to Data Register (DR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | $\overline{CS}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 1 | 0 | RB | RA | 0 | 0 | | |

### Transfer Data Register (DR) to Wiper Counter Register (WCR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 0 | 1 | RB | RA | 0 | 0 | |

### Increment/Decrement Wiper Counter Register (WCR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Increment/Decrement (Sent by Master on SI) | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 0 | 1 | 0 | X | X | 0 | 0 | I/D | I/D | . | . | I/D | I/D | |

### Read Status Register (SR)

| $\overline{CS}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Data Byte (Sent by X9251 on SO) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WIP | |

**Notes:** (1) "A1 ~ A0": stands for the device addresses sent by the master.
(2) WPx refers to wiper position data in the Counter Register
(2) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).
(3) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

## ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....–65°C to +135°C
Storage temperature .....–65°C to +150°C
Voltage on SCK, any address input, $V_{CC}$
with respect to $V_{SS}$.....–1V to +7V
$\Delta V = | (V_H – VL) |$ ..... 5.5V
Lead temperature (soldering, 10 seconds).....300°C
$I_W$ (10 seconds) ..... ±6mA

## COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Temp | Min. | Max. |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | –40°C | +85°C |

| Device | Supply Voltage ($V_{CC}$)(4) Limits |
|---|---|
| X9251 | 5V ±10% |
| X9251-2.7 | 2.7V to 5.5V |

**ANALOG CHARACTERISTICS** (Over recommended industrial operating conditions unless otherwise stated.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | |
| $R_{TOTAL}$ | End to End Resistance | | 100 | | kΩ | T version |
| $R_{TOTAL}$ | End to End Resistance | | 50 | | kΩ | U version |
| | End to End Resistance Tolerance | | | ±20 | % | |
| | Power Rating | | | 50 | mW | 25°C, each pot |
| $I_W$ | Wiper Current | | | ±3 | mA | |
| $R_W$ | Wiper Resistance | | | 300 | Ω | $I_W = \frac{V(V_{CC})}{R_{TOTAL}}$ @ $V_{CC}$ = 3V |
| | | | | 150 | Ω | $I_W = \frac{V(V_{CC})}{R_{TOTAL}}$ @ $V_{CC}$ = 5V |
| $V_{TERM}$ | Voltage on any $R_H$ or $R_L$ Pin | $V_{SS}$ | | $V_{CC}$ | V | $V_{SS}$ = 0V |
| | Noise | | -120 | | dBV/√Hz | Ref: 1V |
| | Resolution | | 0.4 | | % | |
| | Absolute Linearity (1) | -1 | | +1 | MI(3) | $R_{w(n)(actual)} – R_{w(n)(expected)}$(5) |
| | Relative Linearity (2) | -0.6 | | +0.6 | MI(3) | $R_{w(n+1)} – [R_{w(n)} + MI]$(5) |
| | Temperature Coefficient of $R_{TOTAL}$ | | ±300 | | ppm/°C | |
| | Ratiometric Temp. Coefficient | -20 | | +20 | ppm/°C | |
| $C_H/C_L/C_W$ | Potentiometer Capacitances | | 10/10/25 | | pF | See Macro model |

**Notes:** (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT / 255 or ($R_H – R_L$) / 255, single pot
(4) During power up $V_{CC} > V_H$, $V_L$, and $V_W$.
(5) n = 0, 1, 2, …,255; m =0, 1, 2, …, 254.

**D.C. OPERATING CHARACTERISTICS** (Over the recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | |
| $I_{CC1}$ | $V_{CC}$ supply current (active) | | | 400 | µA | $f_{SCK}$ = 2.5 MHz, SO = Open, $V_{CC}$=6V Other Inputs = $V_{SS}$ |
| $I_{CC2}$ | $V_{CC}$ supply current (non-volatile write) | | 1 | 5 | mA | $f_{SCK}$ = 2.5MHz, SO = Open, $V_{CC}$=6V Other Inputs = $V_{SS}$ |
| $I_{SB}$ | $V_{CC}$ current (standby) | | | 3 | µA | SCK = SI = $V_{SS}$, Addr. = $V_{SS}$, $\overline{CS}$ = $V_{CC}$ = 6V |
| $I_{LI}$ | Input leakage current | | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output leakage current | | | 10 | µA | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$ |
| $V_{IH}$ | Input HIGH voltage | $V_{CC}$ x 0.7 | | $V_{CC}$ + 1 | V | |
| $V_{IL}$ | Input LOW voltage | –1 | | $V_{CC}$ x 0.3 | V | |
| $V_{OL}$ | Output LOW voltage | | | 0.4 | V | $I_{OL}$ = 3mA |
| $V_{OH}$ | Output HIGH voltage | $V_{CC}$ - 0.8 | | | V | $I_{OH}$ = -1mA, $V_{CC} \geq$ +3V |
| $V_{OH}$ | Output HIGH voltage | $V_{CC}$ - 0.4 | | | V | $I_{OH}$ = -0.4mA, $V_{CC} \leq$ +3V |

**ENDURANCE AND DATA RETENTION**

| Parameter | Min. | Units |
|---|---|---|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention | 100 | years |

**CAPACITANCE**

| Symbol | Test | Max. | Units | Test Conditions |
|---|---|---|---|---|
| $C_{IN/OUT}$(6) | Input / Output capacitance (SI) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{OUT}$(6) | Output capacitance (SO) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$(6) | Input capacitance (A0, A1, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$, and SCK) | 6 | pF | $V_{IN}$ = 0V |

**POWER-UP TIMING**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_r V_{CC}$(6) | $V_{CC}$ Power-up rate | 0.2 | 50 | V/ms |
| $t_{PUR}$(7) | Power-up to initiation of read operation | | 1 | ms |
| $t_{PUW}$(7) | Power-up to initiation of write operation | | 50 | ms |

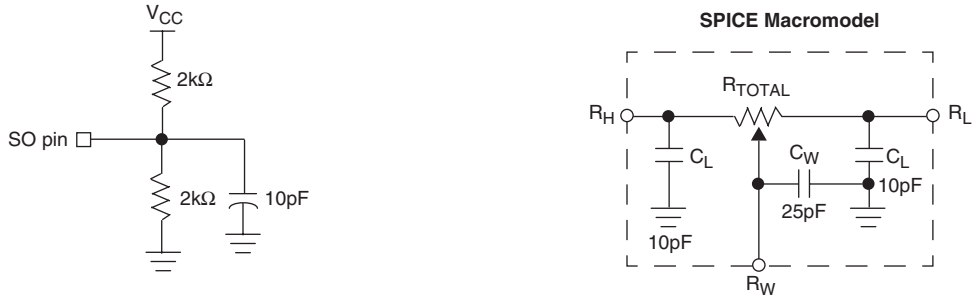
**A.C. TEST CONDITIONS**

| | |
|---|---|
| Input Pulse Levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing level | $V_{CC}$ x 0.5 |

**Notes:** (6) This parameter is not 100% tested

(7) $t_{PUR}$ and $t_{PUW}$ are the delays required from the time the (last) power supply ($V_{CC}$-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

## EQUIVALENT A.C. LOAD CIRCUIT




## AC TIMING

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{SCK}$ | SPI clock frequency | | 2 | MHz |
| $t_{CYC}$ | SPI clock cycle rime | 500 | | ns |
| $t_{WH}$ | SPI clock high rime | 200 | | ns |
| $t_{WL}$ | SPI clock low time | 200 | | ns |
| $t_{LEAD}$ | Lead time | 250 | | ns |
| $t_{LAG}$ | Lag time | 250 | | ns |
| $t_{SU}$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time | 50 | | ns |
| $t_H$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time | 50 | | ns |
| $t_{RI}$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time | | 2 | µs |
| $t_{FI}$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time | | 2 | µs |
| $t_{DIS}$ | SO output disable time | 0 | 250 | ns |
| $t_V$ | SO output valid time | | 200 | ns |
| $t_{HO}$ | SO output hold time | 0 | | ns |
| $t_{RO}$ | SO output rise time | | 100 | ns |
| $t_{FO}$ | SO output fall time | | 100 | ns |
| $t_{HOLD}$ | $\overline{HOLD}$ time | 400 | | ns |
| $t_{HSU}$ | $\overline{HOLD}$ setup time | 100 | | ns |
| $t_{HH}$ | $\overline{HOLD}$ hold time | 100 | | ns |
| $t_{HZ}$ | $\overline{HOLD}$ low to output in high Z | | 100 | ns |
| $t_{LZ}$ | $\overline{HOLD}$ high to output in low Z | | 100 | ns |
| $T_I$ | Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs | | 10 | ns |
| $t_{CS}$ | $\overline{CS}$ deselect time | 2 | | µs |
| $t_{WPASU}$ | $\overline{WP}$, A0 setup time | 0 | | ns |
| $t_{WPAH}$ | $\overline{WP}$, A0 hold time | 0 | | ns |

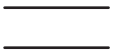
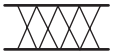
### HIGH-VOLTAGE WRITE CYCLE TIMING

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $t_{WR}$ | High-voltage write cycle time (store instructions) | 5 | 10 | ms |

### XDCP TIMING

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{WRPO}$ | Wiper response time after the third (last) power supply is stable | 5 | 10 | µs |
| $t_{WRL}$ | Wiper response time after instruction issued (all load instructions) | 5 | 10 | µs |

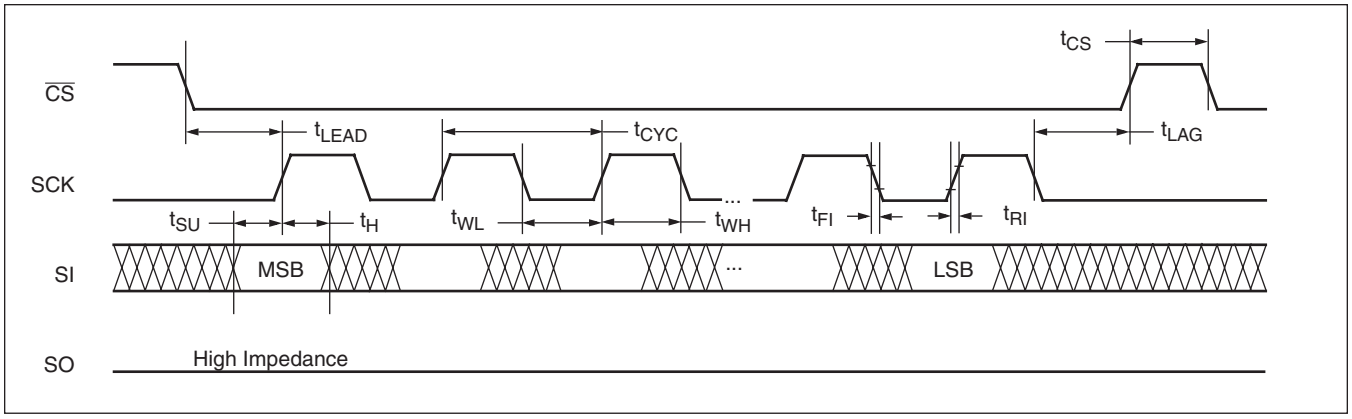
### SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Must be steady | Will be steady |
|  | May change from Low to High | Will change from Low to High |
|  | May change from High to Low | Will change from High to Low |
|  | Don't Care: Changes Allowed | Changing: State Not Known |
|  | N/A | Center Line is High Impedance |

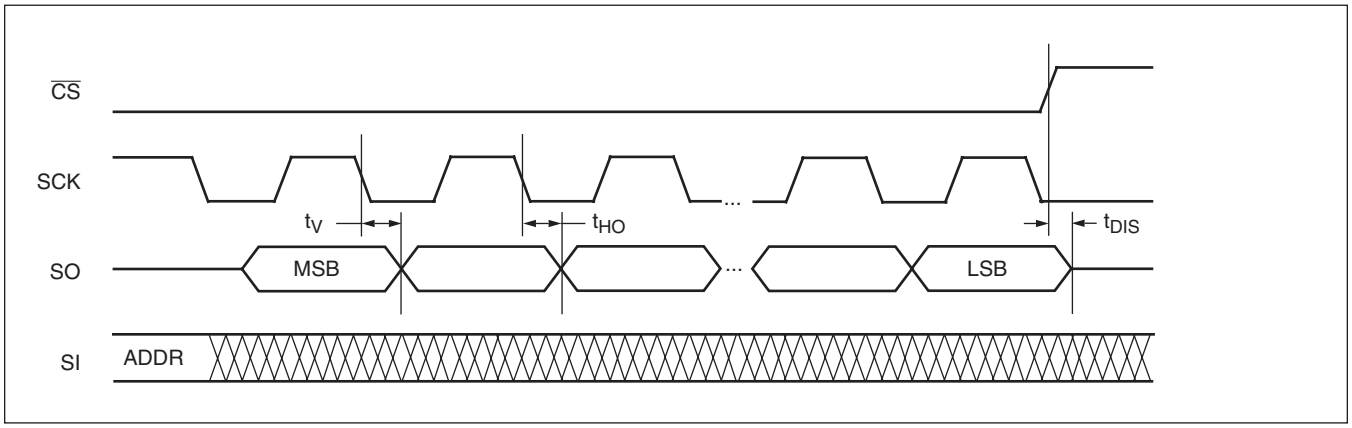
.

## TIMING DIAGRAMS

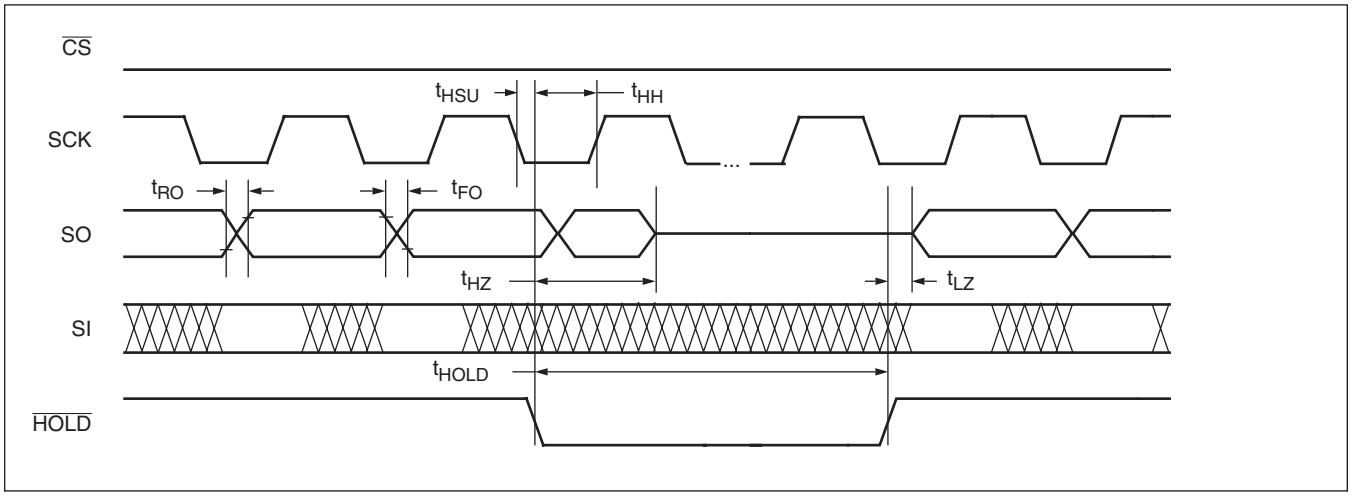
### Input Timing



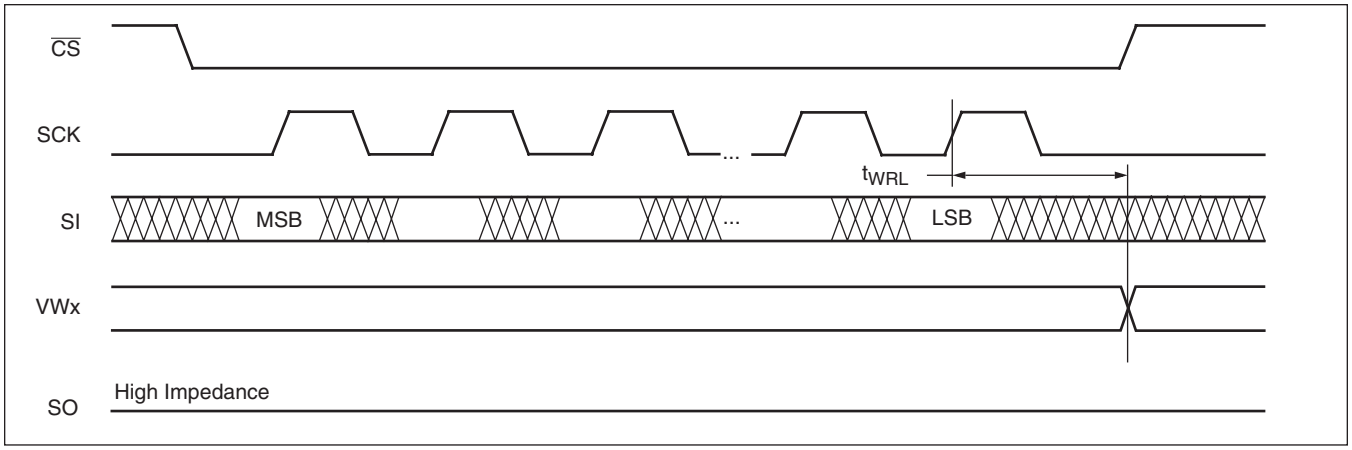

### Output Timing



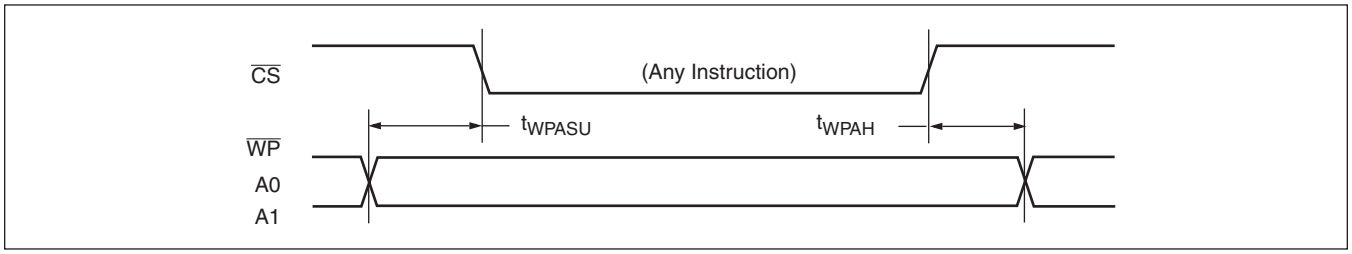

### Hold Timing



### XDCP Timing (for All Load Instructions)

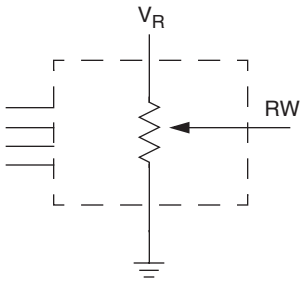



### Write Protect and Device Address Pins Timing

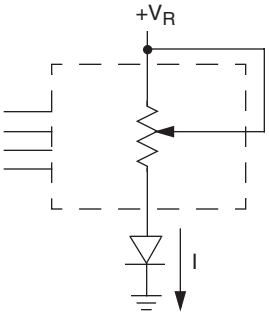


## APPLICATIONS INFORMATION

### Basic Configurations of Electronic Potentiometers



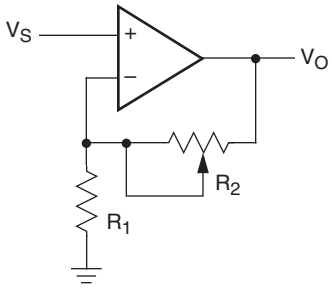

Three terminal Potentiometer;
Variable voltage divider




Two terminal Variable Resistor;
Variable current

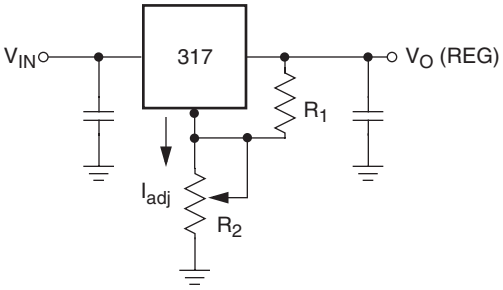
### Application Circuits

#### Noninverting Amplifier



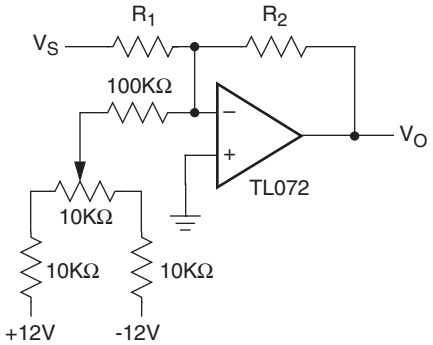

$V_O = (1+R_2/R_1)V_S$

#### Voltage Regulator

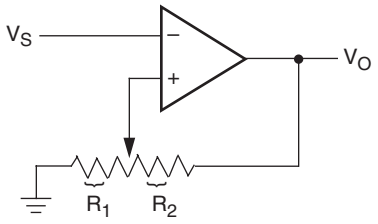



$V_O$ (REG) = 1.25V $(1+R_2/R_1)+I_{adj}\ R_2$

#### Offset Voltage Adjustment



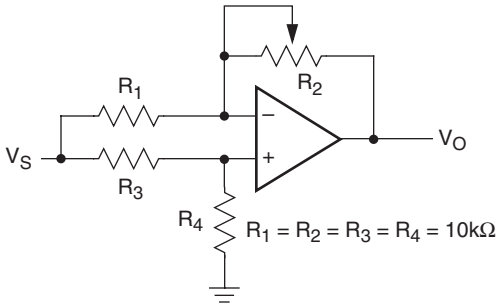

#### Comparator with Hysterisis




$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$RL_L = \{R_1/(R_1+R_2)\}\ V_O(min)$

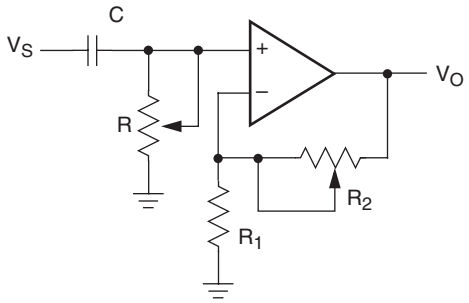
## Application Circuits (continued)

### Attenuator



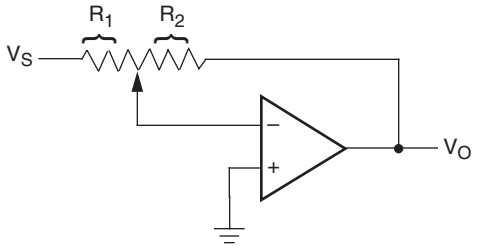

$V_O = G\,V_S$
$-1/2 \le G \le +1/2$

### Filter



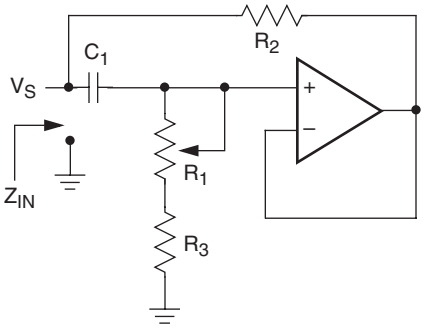

$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

### Inverting Amplifier



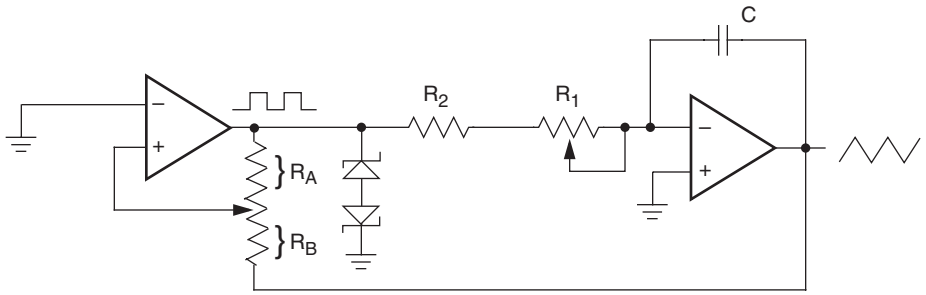

$V_O = G\,V_S$
$G = -R_2/R_1$

### Equivalent L-R Circuit




$Z_{IN} = R_2 + s\,R_2\,(R_1 + R_3)\,C_1 = R_2 + s\,Leq$
$(R_1 + R_3) >> R_2$

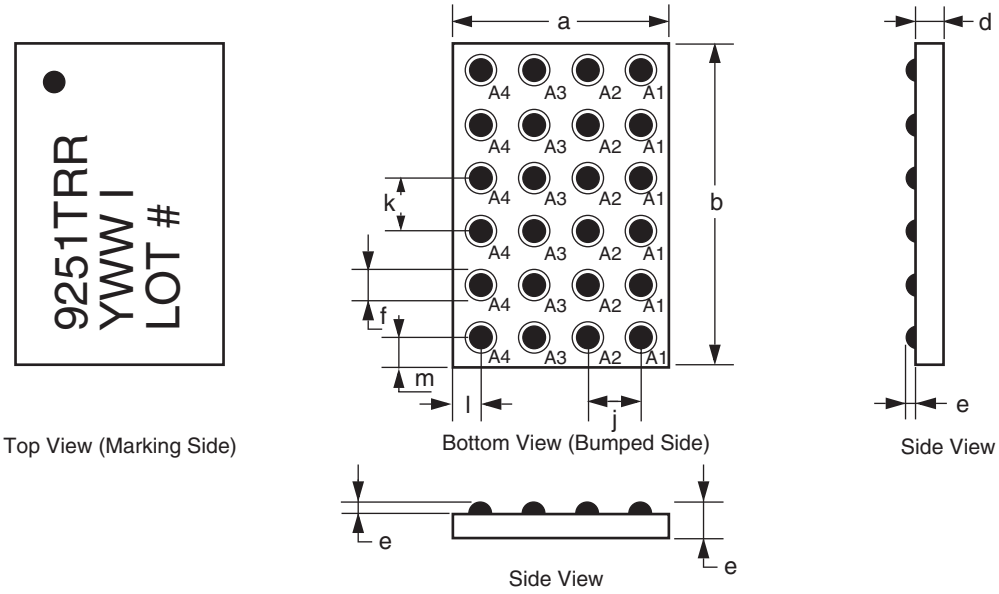
### Function Generator

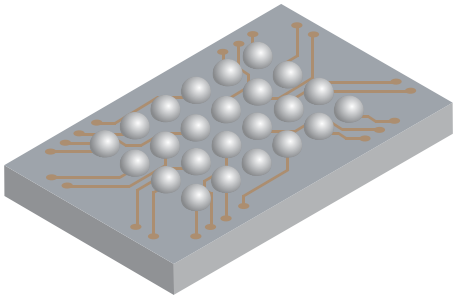



frequency ∝ $R_1$, $R_2$, C
amplitude ∝ $R_A$, $R_B$

**PACKAGING INFORMATION**

## 24-Bump Chip Scale Package (CSP B24)
## Package Outline Drawing



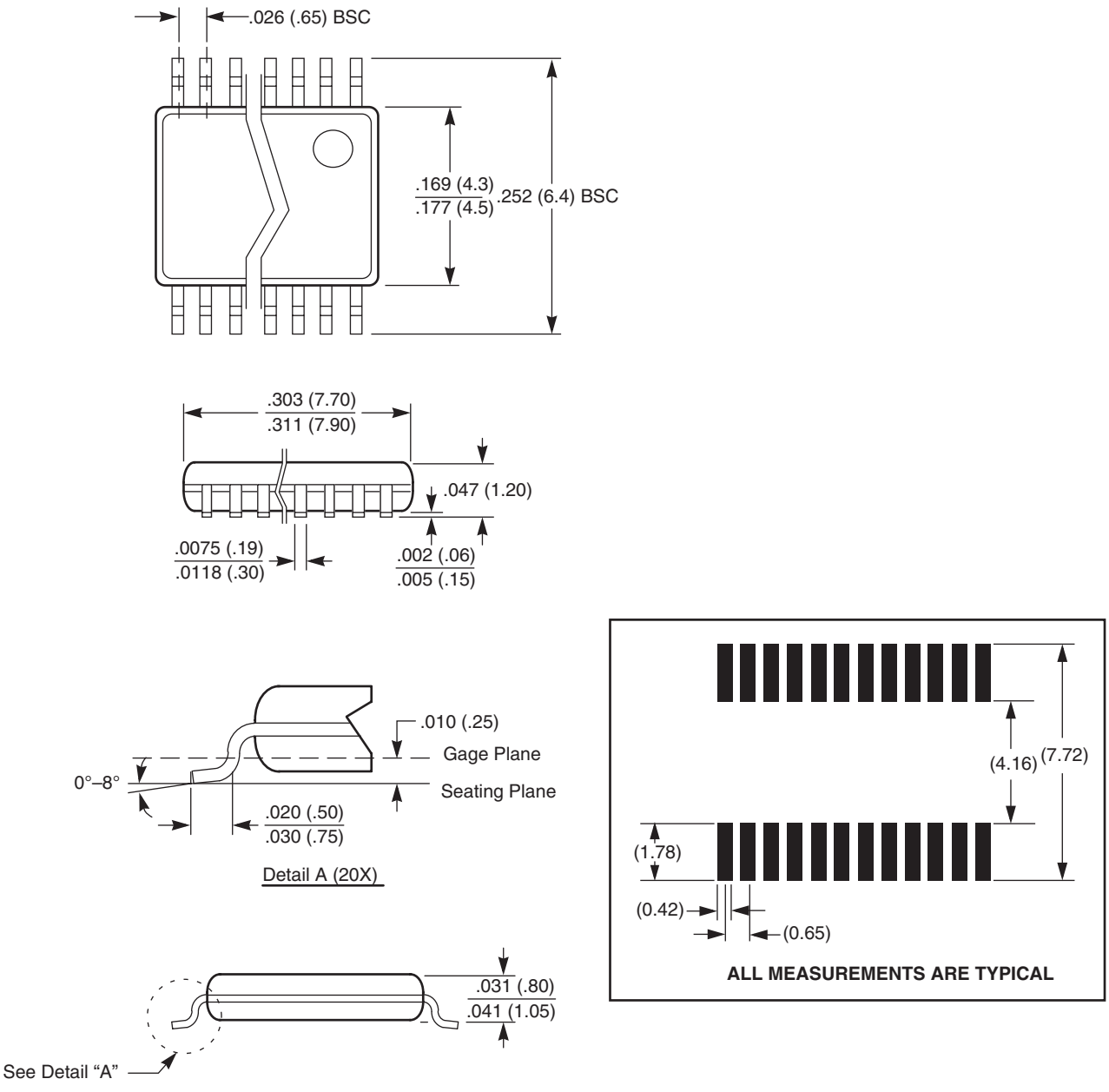
### Ball Matrix

| | 4 | 3 | 2 | 1 |
|---|---|---|---|---|
| **A** | $R_{L1}$ | A1 | $\overline{CS}$ | $R_{W0}$ |
| **B** | $R_{W1}$ | SI | $\overline{WP}$ | $R_{L0}$ |
| **C** | VSS | $R_{H1}$ | $R_{H0}$ | VCC |
| **D** | NC | $R_{H2}$ | $R_{H3}$ | NC |
| **E** | $R_{W2}$ | $\overline{HOLD}$ | SO | $R_{L3}$ |
| **F** | $R_{L2}$ | SCK | A0 | $R_{W3}$ |

| | Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|---|
| | | Min | Nom. | Max | Min | Nom. | Max |
| Package Width | A | 2.755 | 2.785 | 2.815 | | | |
| Package Length | B | 4.507 | 4.537 | 4.567 | | | |
| Package Height | C | 0.644 | 0.677 | 0.710 | | | |
| Body Thickness | D | 0.444 | 0.457 | 0.470 | | | |
| Ball Height | E | 0.200 | 0.220 | 0.240 | | | |
| Ball Diameter | F | 0.300 | 0.320 | 0.340 | | | |
| Ball Pitch – Width | J | | 0.5 | | | | |
| Ball Pitch – Length | K | | 0.5 | | | | |
| Ball to Edge Spacing – Width | L | 0.618 | 0.643 | 0.668 | | | |
| Ball to Edge Spacing – Length | M | 1.056 | 1.081 | 1.106 | | | |

## PACKAGING INFORMATION

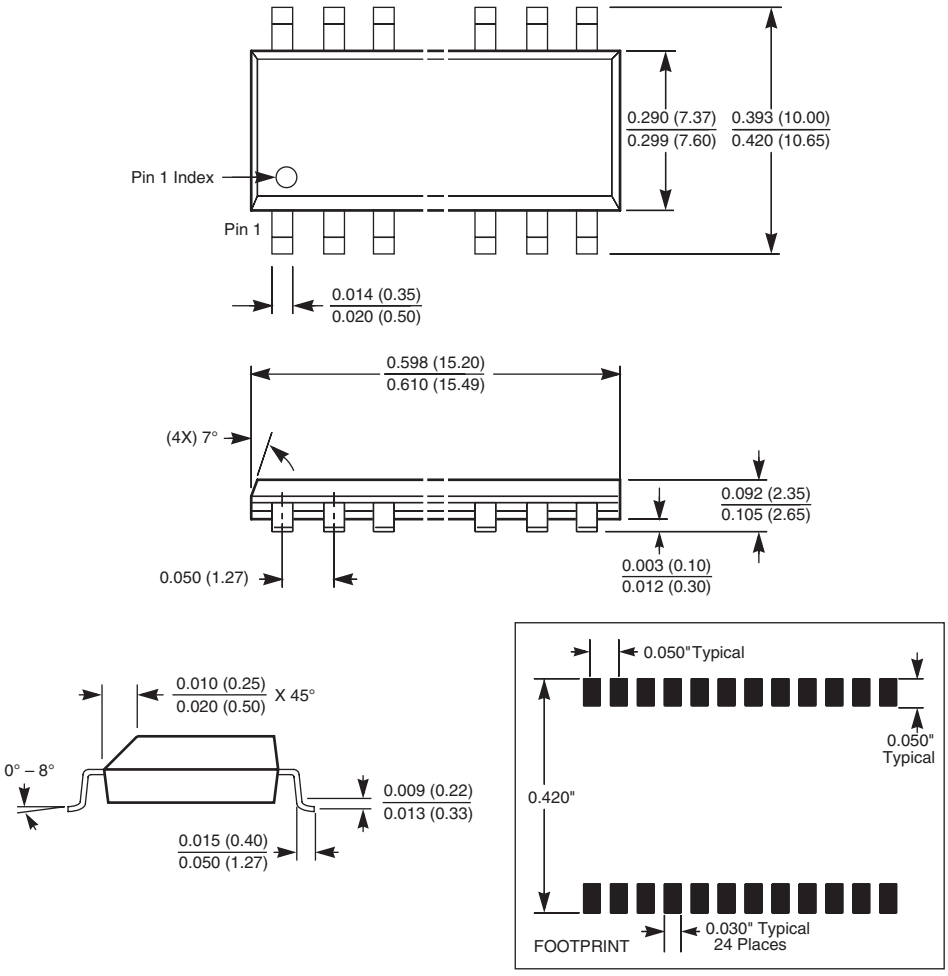
**24-Lead Plastic, TSSOP, Package Code V24**




**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## PACKAGING INFORMATION

### 24-Lead Plastic, SOIC, Package Code S24




**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**