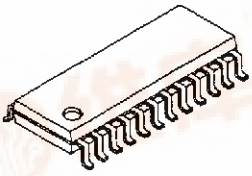
SONY®

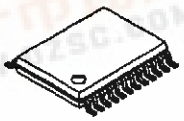
CXA1203M/N

8mm VCR PAL JOG

CXA1203M
24 pin SOP (Plastic)



CXA1203N
24 pin SSOP



Description

The CXA1203 compensates the color alignment in variable speed mode for PAL-system 8 mm VCRs. This IC is also available for the SECAM system with the built-in SECAM detector and BELL and C-BELL filters.

Features

- Color alignment compensation which does not require 1H delay line
- No AFC (fH) adjustment necessary
- Built-in SECAM detector
- Built-in BELL and C-BELL filters
- Available for the PAL-M system

Functions

V-Invert circuit, TH/DL APC, 2 fsc PLL, SQ DET, EX burst circuit, AFC (fH), Timing generator, SECAM detector, BELL filter, C-BELL filter.

Structure

Silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

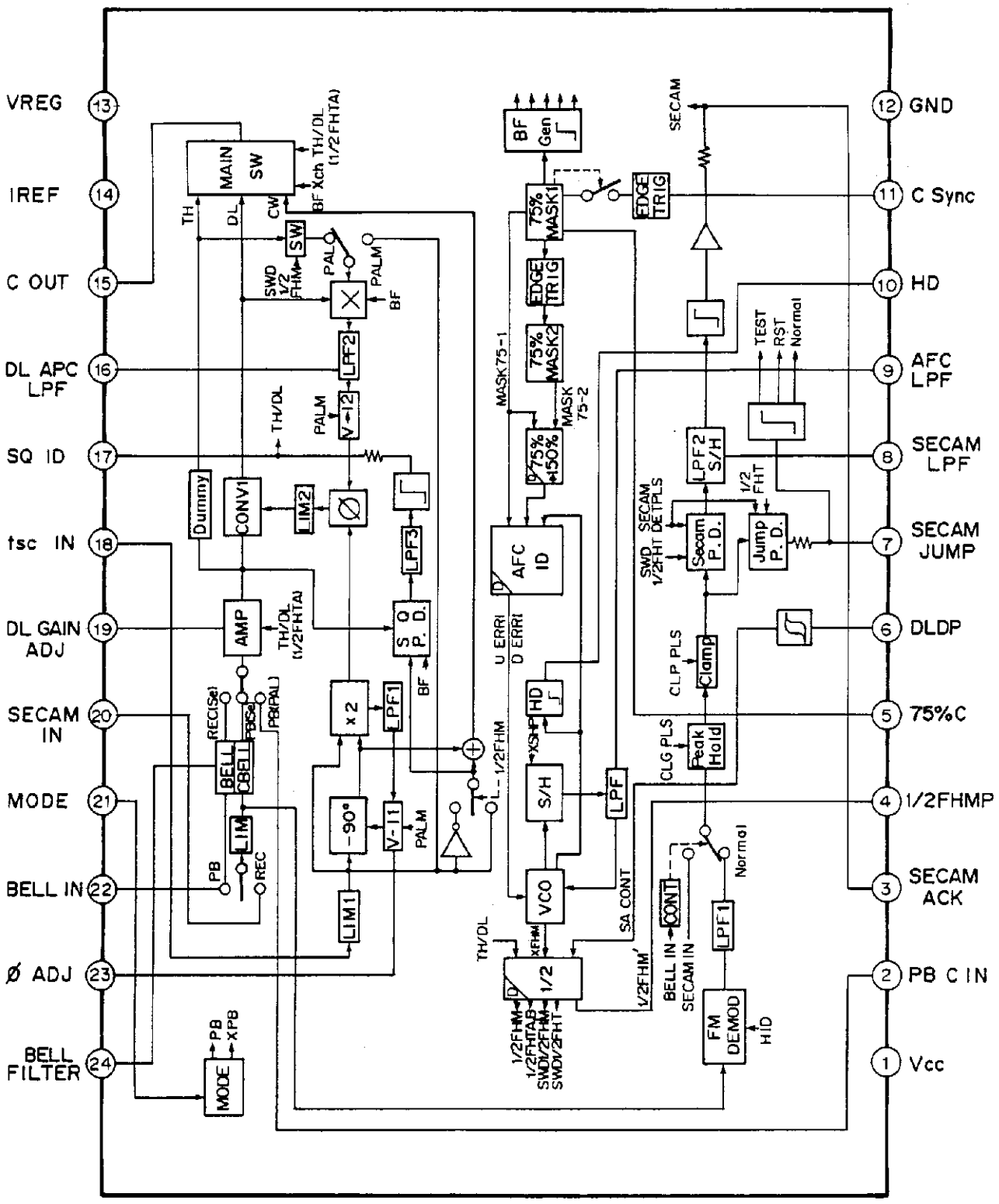
• Supply voltage	V_{CC}	7.0	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	CXA1203M 567	mW
		CXA1203N 536	mW

Recommended Operating Conditions

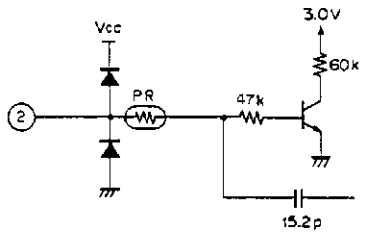
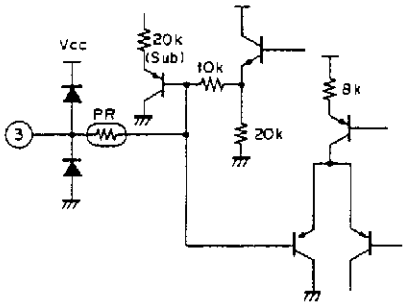
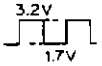
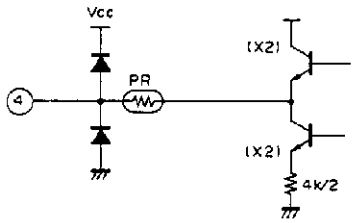
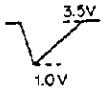
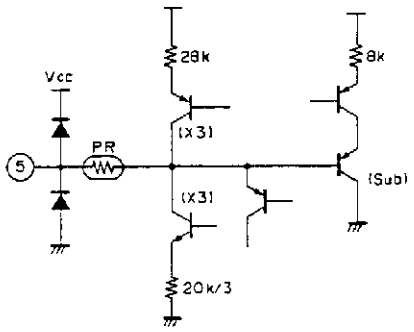
• Supply voltage	4.50 to 5.50 (5.0 V Typ.)	V

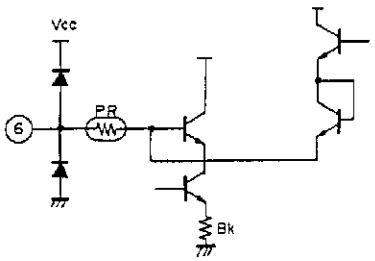
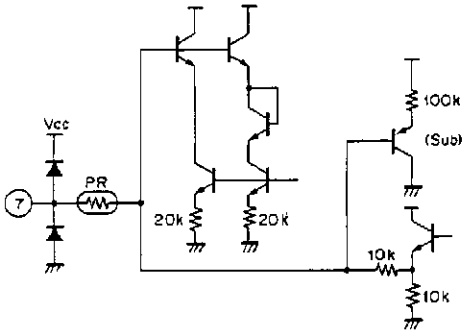
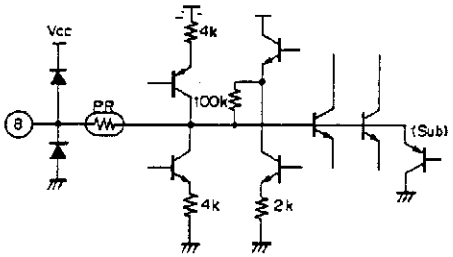
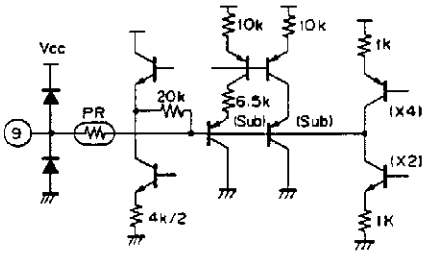
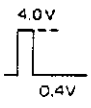
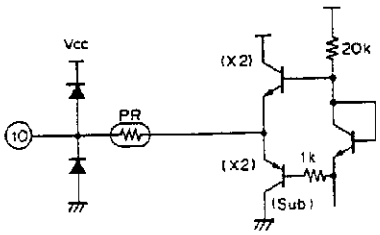
E89750A8X

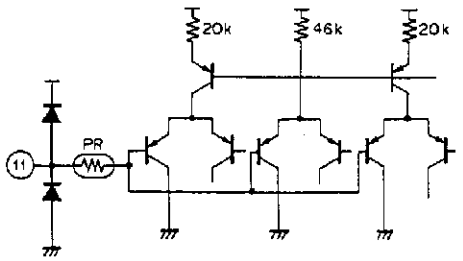
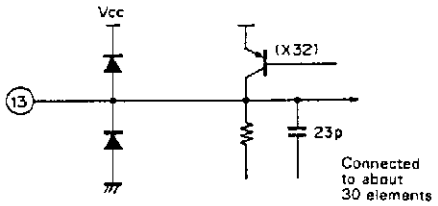
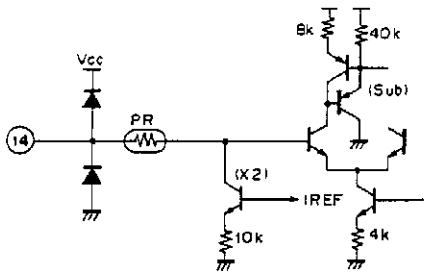
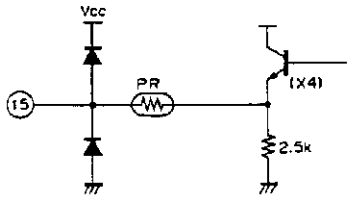
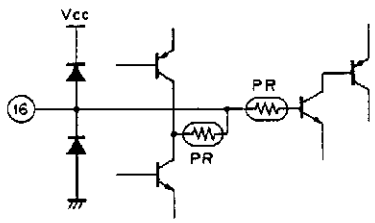
Block Diagram and Pin Configuration

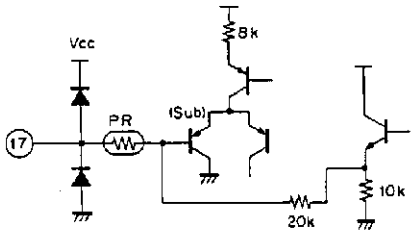
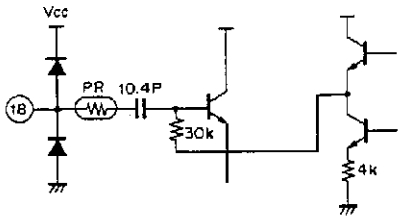
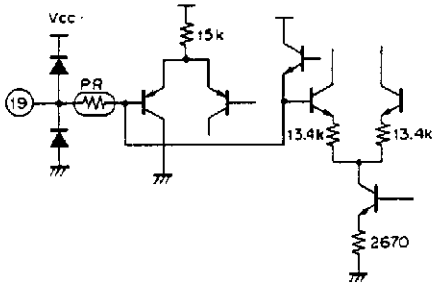
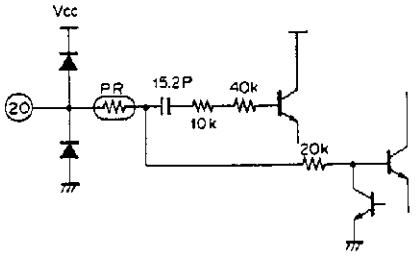


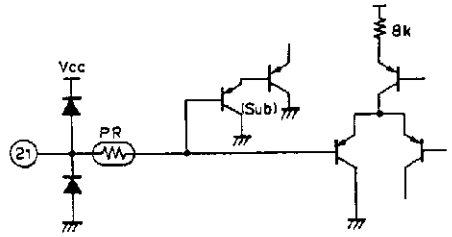
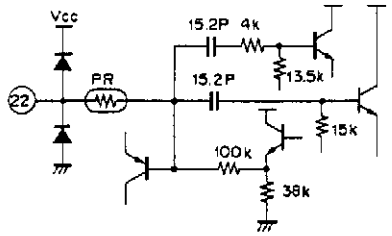
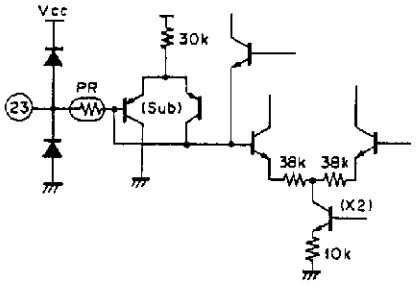
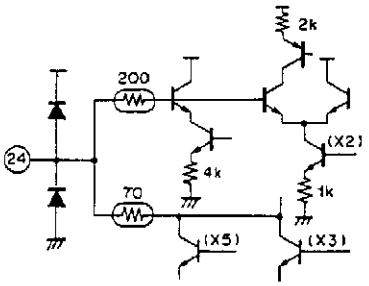
Pin Description

No.	Symbol	Voltage DC	Voltage AC	Equivalent circuit	Description
1	Vcc	5.0 V (typical)	–	–	Supply voltage pin
2	PB C IN		350mVp-p 150mVp-p (burst)		Input pin of PAL playback chrominance signal. The chroma ACK operates to cut off the output at pin 15 when the DC bias voltage at pin 2 is 0.7 V or less.
3	SECAM ACK	3.8V (H) 0V (L)	–		SECAM detector output pin. H → SECAM L → PAL The SECAM or PAL mode is fixed by applying an external DC voltage. SECAM: 3.0 to 5.0 V PAL: 0 to 1.0 V
4	1/2FHMP	–			Output pin of the pulse obtained by dividing down the AFC (fH-PLL) output by 2.
5	75% C	–			Connecting pin of the charging and discharging capacity to produce the triangular wave chronized with the C sync signal. All timing pulses used in the IC are produced from this triangular wave.

No.	Symbol	Voltage		Equivalent circuit	Description
		DC	AC		
6	DLDP	2.8V (H) 1.4V (L)	1.4Vp-p		Input pin to switch the polarity of the 1/2 FHT pulse for the SECAM detector. Ouptut pin of the AFC ID signal in TEST mode*1
7	SECAM JUMP	2.8V (H) 1.4V (L)	1.4Vp-p		Output pin to switch the polarity of the 1/2 FHT pulse. Mode selection*1 is possible by applying an external DC voltage. PAL-M: 0 to 0.5 V Normal: OPEN RESET: 3.6 to 4.1 V TEST: 4.3 to 5.0 V
8	SECAM LPF	2.5V	—		Connecting pin of the time constant of the LPF for the SECAM detector.
9	AFC LPF	2.0V	—		Connecting pin of the time constant of the LPF for the AFC (fH-PLL).
10	HD	—			Output pin of the HD pulse produced in the AFC (fH-PLL).

No.	Symbol	Voltage		Equivalent circuit	Description
		DC	AC		
11	C Sync		2.0V		Input pin of the composite sync signal. The internal threshold voltage is 2.0 V and the polarity is active HIGH.
12	GND	—	—		GND pin
13	VREG	4.2V	—		Output pin of the regulated voltage source in the IC (4.2 V).
14	IREF	2.1V	—		Connecting pin of the standard resistance to produce the reference current source in the IC.
15	C OUT	2.1V	In PAL mode 350mVp-p 150mVp-p (burst)		Output pin of the playback PAL signal (TH, DL and EX burst)*2, SECAM signal and PAL-M signal.
16	DLAPC LPF	2.4V	—		Connecting pin of the time constant of the LPF for the TH/DL APC loop. The TH/DL lock phase can be varied by applying an external DC current.

No.	Symbol	Voltage		Equivalent circuit	Description
		DC	AC		
17	SQ ID	4.0V (H) 0V (L)	—		Output pin of the SQ detector The TH or DL output signal at pin 15 can be selected by applying an external DC voltage. DL: 0 to 2.0 V TH: 3.0 to 5.0 V
18	fsc IN	—	350mVp-p		Input pin of the fsc. (chrominance subcarrier)
19	DL GAIN ADJ	5.0V (Typ.)			Control pin of the DL signal gain. The gain can be varied by applying an external DC voltage. The internally fixed gain is obtained at 5.0 V. Output pin of the S/H circuit in TEST mode.
20	SECAM IN	—	150mVp-p (burst)		Input pin of the SECAM detector in REC mode.

No.	Symbol	Voltage		Equivalent circuit	Description
		DC	AC		
21	MODE	—	—		Mode selection*1 is possible by applying an external DC voltage. REC: 0 to 1.3 V PB: 1.7 to 2.8 V JOG: 3.2 to 5.0 V
22	BELL IN	—	83mVp-p (SECAM burst) 117mVp-p (PAL burst)		Input pin of the SECAM signal. Input pin of the SECAM detector in playback mode.
23	ϕADJ	5.0V (typical)	—		EX burst phase adjustment pin. The phase can be varied by applying an external DC voltage. The internally fixed phase is obtained at 5.0 V. VCO output pin in TEST mode.
24	BELL FILTER	3.0V	—		Connecting pin of the time constant of the BELL and C-BELL filters.

Note) *1. Refer to Mode Description.

*2. PAL playback signal (TH, DL and EX burst)
The DL signal is symmetrical to the TH signal (PAL playback signal) about the B-Y axis.
The burst signal produced from the fsc (chrominance subcarrier) in the IC is known as the EX burst. The EX burst is inserted into the playback chrominance signal in JOG mode.

Mode Description

Mode	Control pin	Voltage	Description
PAL	3 pin	0 to 1.0 V	Fixed PAL mode
—		High impedance	Automatic selection of PAL or SECAM
SECAM		3.0 to 5.0 V	Fixed SECAM mode
PAL-M	7 pin	0 to 0.5 V	The PAL-M signal is output from pin 15 by inputting an NTSC signal to pin 2. (For details, see "Notes on Use".)
RESET		3.6 to 4.1 V	The logic block (AFC ID, 150% masking and 1/2 division) in the AFC (fH-PLL) is turned off.
TEST		4.3 to 5.0 V	The operation of the AFC ID, VCO and S/H blocks in the AFC (fH-PLL) is checked.
DL	17 pin	0 to 2.0 V	The DL signal is output from pin 15.
—		High impedance	The TH or DL signal selected by the SQ detector decision is output.
TH		3.0 to 5.0 V	The TH signal is output from pin 15.
REC	21 pin	0 to 1.3 V	REC mode
PB		1.7 to 2.8 V	Playback mode
JOG		3.2 to 5.0 V	The EX burst is inserted into the original burst signal portion in PAL playback mode.

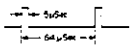
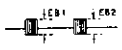
Electrical Characteristics

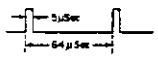
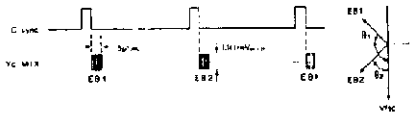
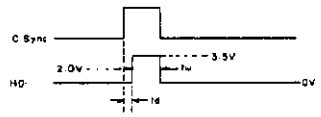
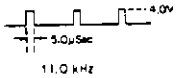
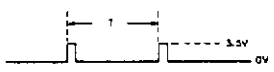
See Fig.1. Ta = 25°C, Vcc = 5.0V

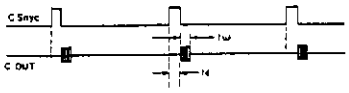
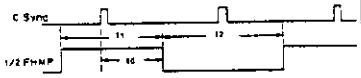
No.	Item	Symbol	Switch Condition ON: ○, OFF: blank					Bias Condition						Test Point	Output Waveform and Test Content		Min.	Typ.	Max.	Units
			SW 1	SW 2	SW 3	SW 4	SW 5	Vcc	V_2	V_3	V_7	V_{17}	V_{21}		Mode					
1	Circuit Current (PAL PB)	Icc (PP)						5.0V	2.5V	1.0V			1.7V	A	PAL PB	DC current test	17.5	25.5	32.5	mA
2	Circuit Current (SECAM REC)	Icc (SR)						↓	↓	3.0V			1.3V	A	SECAM REC	DC current test	20.0	27.0	34.0	mA
3	VREG (5.0V)	VREG (5.0)						↓	↓	1.0V			1.7V	E	PAL PB	DC voltage test	4.10	4.24	4.40	V
4	VREG (4.5V)	VREG (4.5)						4.5V	↓	↓			↓	↓			4.10	4.24	4.40	V
5	VREG (5.5V)	VREG (5.5)						5.5V	↓	↓			↓	↓			4.10	4.24	4.40	V
6	V (IREF)	V (IREF)						5.0V	↓	↓			↓	F			2.05	2.12	2.20	V
7	Input SW Crosstalk (SECAM REC)	I-CT (SR)				○		↓	↓	3.0V			1.3V	G	SECAM REC	C OUT output level test		−38.0	−35.0	dB
8	Input SW Crosstalk (SECAM PB)	I-CT (SP)						↓	↓	↓			1.7V	↓	SECAM PB	C OUT output level test		−53.0	−45.0	dB
9	BELL FILTER Gain	BF-G						↓	↓	↓			1.3V	↓	SECAM REC	C OUT output level test	11.0	14.0	16.0	dB
10	C-BELL FILTER Gain	CBF-G						↓	↓	↓			1.7V	↓	SECAM PB	C OUT output level test	−3.0	0	3.0	dB
11	TH Amp Gain	THA-G			○			↓	↓	1.0V		3.0V	2.8V	H	PAL PB	C OUT output level test (4.43MHz)	−2.5	−0.3	2.0	dB
12	TH/DL Amp Gain Ratio	DA-G			○			↓	↓	↓		2.0V	↓	↓			−0.6	0.4	1.4	dB
13	TH/DL Phase Difference	$\theta_{TH\text{-}DL}$			○			↓	↓	↓		↓	↓	G		C OUT phase test	50	90	120	deg
14	TH/EXB Level Ratio	$\Delta V_{TH\text{-}EXB}$						↓	↓	↓			3.2V	H	PAL JOG	C OUT Output level test	1.1	2.6	4.1	dB
15	EX Burst Level Ratio	ΔV_{EXB}						↓	↓	↓			↓	↓			−1.0	0	1.0	dB
16	EX Burst Phase Difference	$\Delta \theta_{EXB}$						↓	↓	↓			↓	G		C OUT Phase test	90	96	102	deg
17	TH-EX Burst Phase Difference	$\theta_{TH\text{-}EXB}$						↓	↓	↓			↓	↓			40	48	56	deg
18	PAL-M DL APC Loop Characteristics	DL-APC (PAL M)		○				↓	↓	↓	5.0V	0V	2.8V	↓	PAL-M PB	C OUT phase test	−100	−90	−80	deg
19	PAL-M EX Burst Level Ratio	ΔV_{EXB} (PAL M)		○				↓	↓	↓	↓	↓	↓	↓		C OUT output level test	−1.5	0	1.5	dB
20	PAL-M EX Burst Phase Difference	$\Delta \theta_{EXB}$ (PAL M)		○				↓	↓	↓	↓	↓	↓	↓		C OUT phase test	−104	−96	−88	deg
21	PAL-M DL-EX Burst Phase Difference	$\theta_{TH\text{-}EXB}$ (PAL M)		○				↓	↓	↓	↓	↓	↓	↓			−20	−10	0	deg

No.	Item	Symbol	Switch Condition ON: O, OFF: blank					Bias Condition						Test Point	Output Waveform and Test Content		Min.	Typ.	Max.	Units
			SW 1	SW 2	SW 3	SW 4	SW 5	Vcc	V_2	V_3	V_7	V_{17}	V_{21}		Mode					
22	SQ DET +V Detection	SQ (+)		O				5.0V	2.5V	1.0V	3.8V		2.8V	I	PAL RESET	DC voltage test at pin 17	−122		−98	deg
23	SQ DET −V Detection	SQ (−)		O				↓	↓	↓	↓		↓	↓			−35		−59	deg
24	Main SW Crosstalk (TH)	MSW-CT (TH)			O			↓	↓	↓		3.0V	1.7V	G	PAL PB	C OUT output level test		−49	−44	dB
25	AFC HD Timing	HD-D						↓	↓	↓			↓	D		Time test at pin 10	−3.0	−1.2	0.3	μs
26	AFC HD Width	HD-W						↓	↓	↓			↓	↓			4.4	5.3	6.2	μs
27	AFC Lock Range (1)	AFC-LR (1)						↓	↓	↓			↓	↓		Frequency test at pin 10	−55		55	Hz
28	AFC Lock Range (2)	AFC-LR (2)						↓	↓	↓			↓	↓			−55		55	Hz
29	TIMING EX Burst Delay	EXB-D						↓	↓	↓			3.2V	G	PAL JOG	Time test	4.5	5.2	5.8	μs
30	TIMING EX Burst Width	EXB-W						↓	↓	↓			↓	↓			3.9	4.4	5.1	μs
31	TIMING 1/2 FHMP Delay	1/2FH-D					O	↓	↓	↓			1.7V	C	PAL PB		32.0	36.0	40.0	μs
32	TIMING 1/2 FHMP Duty	1/2FH-DU					O	↓	↓	↓			↓	↓			44	50	56	%
33	SECAM DETECTOR DEMOD (PB)	SA (PB)	O					↓	↓				2.8V	B	PB	DC voltage test at pin 3	3.60	3.80	4.0	V
34	ACK Check	ACK			O			↓	0.5V	1.0V		5.0V	↓	G	PAL PB	C OUT output level test		−58	−49	dB

Test Methods of Electrical Characteristics

No.	Item	Input Signal				Test Content
		V_{PAL}	V_{SE}	V_{sync}	V_{fsc}	
1	Circuit current (PAL PB)					
2	Circuit current (SECAM REC)					
3	VREG (5.0V)					Test the DC voltage at pin 13.
4	VREG (4.5V)					Test the DC voltage at pin 13.
5	VREG (5.5V)					Test the DC voltage at pin 13.
6	V (IREF)					Test the DC voltage at pin 14.
7	Input SW Crosstalk (SECAM REC)		4.286MHz CW 350mV$_{P-P}$	15.625kHz, 4.0V$_{P-P}$ 		$20 \log \left\{ \frac{\text{C OUT (4.286MHz component)}}{V_{SE}} \right\}$
8	Input SW Crosstalk (SECAM PB)	4.286MHz CW 350mV$_{P-P}$		↓		$20 \log \left\{ \frac{\text{C OUT (4.286MHz component)}}{V_{PAL}} \right\}$
9	BELL FILTER Gain		4.286MHz CW 32mV$_{P-P}$	↓		$20 \log \left\{ \frac{\text{C OUT (4.286MHz component)}}{V_{SE}} \right\}$
10	C-BELL FILTER Gain		4.286MHz CW 83mV$_{P-P}$	↓		
11	TH Amp Gain	CW delayed by 135° from V_{fsc} 350mV$_{P-P}$		↓	4.43MHz CW 350mV$_{P-P}$	$20 \log \left\{ \frac{\text{C OUT (4.43MHz)}}{V_{PAL}} \right\}$
12	TH/DL Amp Gain Ratio	↓		↓	↓	$20 \log \left\{ \frac{\text{Output level of T11}}{\text{C OUT (4.43MHz)}} \right\}$
13	TH/DL Phase Difference	CW delayed by 135° from V_{fsc} 150mV$_{P-P}$		↓	↓	$\theta_{DL}-\theta_{TH}$
14	TH/EXB Level Ratio			↓	↓	$20 \log \left\{ \frac{\text{T11 (P-P)}}{(EB1+EB2)/2} \right\} - 7.4\text{dB}$ 
15	EX Burst Level Ratio			↓	↓	 $\Delta V(EB) = 20 \log \{ V(EB1)/V(EB2) \}$

No.	Item	Input Signal				Test Content
		V_{PAL}	V_{SE}	V_{sync}	V_{fsc}	
16	EX Burst Phase Difference			15.625kHz, 4.0V_{0-P} 	4.43MHz, CW 350mV_{P-P}	$\Delta\theta(EB)=\theta_2-\theta_1$
17	TH-EX Burst Phase Difference			↓	↓	$\frac{\theta_1+\theta_2}{2}-\theta_{TH}$ Phase difference between the center of EX burst and TH signal.
18	PAL-M DL APC Loop Characteristic	CW delayed by 90° from V_{fsc} 150mV_{P-P}		15.734kHz 4.0V_{0-P} 	3.58MHz CW 350mV_{P-P}	Test θ (DL) on the basis of V_{fsc}
19	PAL-M EX Burst Level Ratio			↓	↓	 $\Delta V(EB)=20\log\{V(EB1)/V(EB2)\}$
20	PAL-M EX Burst Phase Difference			↓	↓	$\Delta\theta(EB)=\lvert\theta_1-\theta_2\rvert$
21	PAL-M DL-EX Burst Phase Difference			↓	↓	$\frac{\theta_1+\theta_2}{2}-T18$ Phase difference between the center of EX burst and DL signal.
22	SQ DET +V Detection	Signal with the phase delayed from V_{fsc} 150mV_{P-P}		15.625kHz 4.0V_{0-P}	4.43MHz CW 350mV_{P-P}	Test the phase of V_{PAL} (on the basis of V_{fsc}) when DC is changed from L to H (4.0V) at pin 17.
23	SQ DET −V Detection	Singal with the phase delayed from V_{fsc} 150mV_{P-P}		↓	↓	Test the phase of V_{PAL} (on the basis of V_{fsc}) when DC is changed from H to L (0V) at pin 17.
24	Main SW Crosstalk (TH)			↓	↓	Test by TH signal timing.
25	AFC HD Timing			↓		td  Test the time at pin 10.
26	AFC HD Width			↓		tw
27	AFC Lock Range (1)					Test the frequency at pin 10. 
28	AFC Lock Range (2)			↓ 19.0kHz		(Input frequency $-\frac{1}{T}$)

No.	Item	Input Signal				Test Content	
		V_{PAL}	V_{SE}	V_{sync}	V_{fsc}		
29	TIMING EX Burst Delay			15.625kHz 4.0V_{o-p}	4.43MHz CW 350mV_{p-p}	td	Test the time at C OUT 
30	TIMING EX Burst width			↓	↓	tw	
31	TIMING 1/2 FHMP Delay			↓		td	Test the time at pin 4. 
32	TIMING 1/2 FHMP Duty			↓		$\frac{t_1}{(t_1+t_2)}$	
33	SECAM DETECTOR DEMOD (PB)		SECAM Signal (Burst level 83mV_{p-p})	15.625kHz 4.0V_{p-p}		Test the DC voltage at pin 3.	
34	ACK Check	4.43MHz CW, 350mV_{p-p}		↓		C OUT (4.43MHz) ⇒ V, 20 log (V/350mV)	

Electrical Characteristics Test Circuit

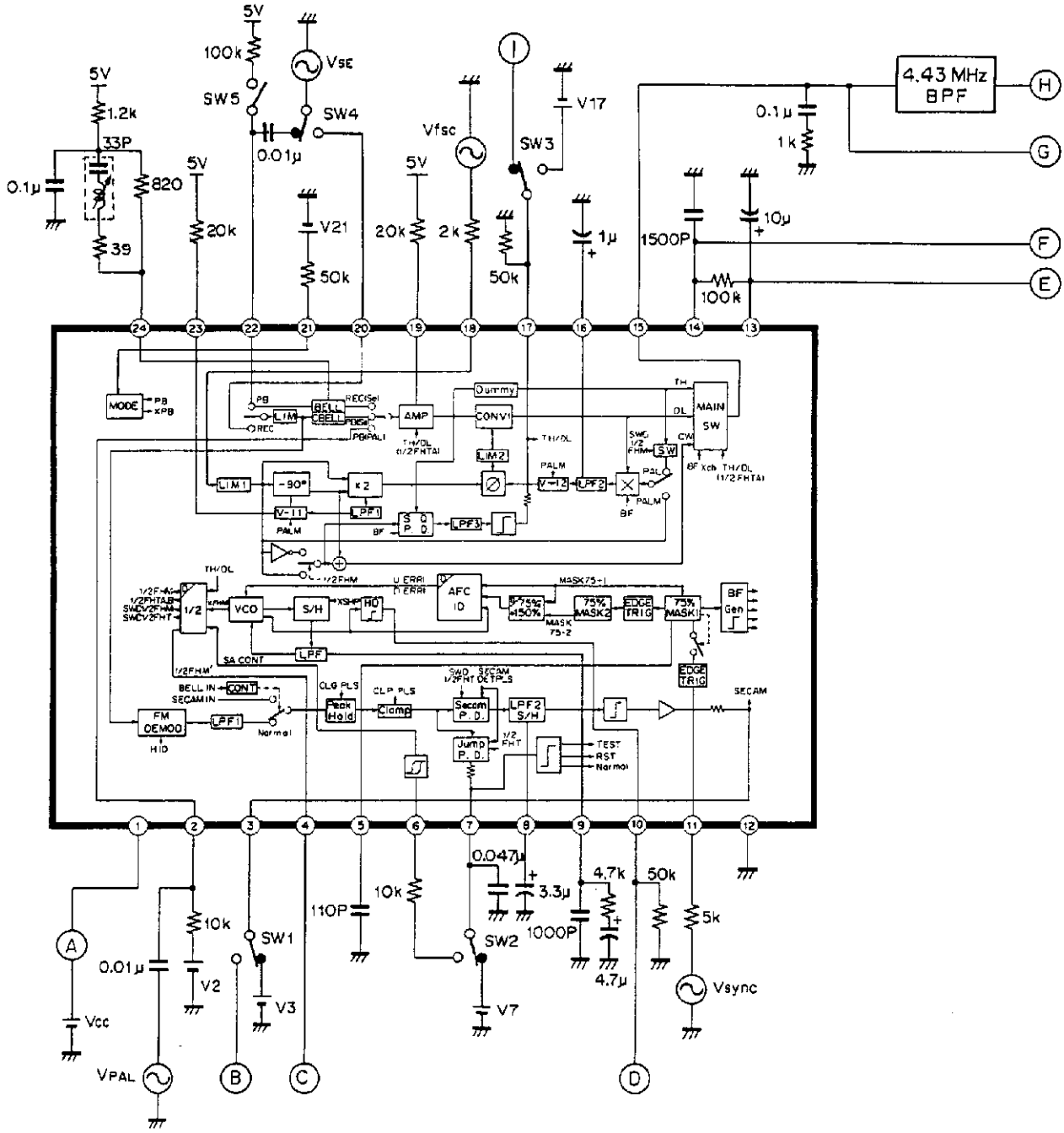


Fig. 1

Description of Functions

1. **Gain Adjustment Amplifier (DL Signal)**
   This amplifier adjusts the gain of the DL signal in PAL or PAL-M mode. The amplifier gain varies according to the DC voltage applied to pin 19. When 5 V is applied to pin 19, the internally fixed gain is obtained and the levels of the TH signal and the DL signal (4.43 MHz component in PAL mode, 3.58 MHz component in PAL-M mode) become the same.

2. **fsc −90° PLL, × 2 and EX Burst Block**

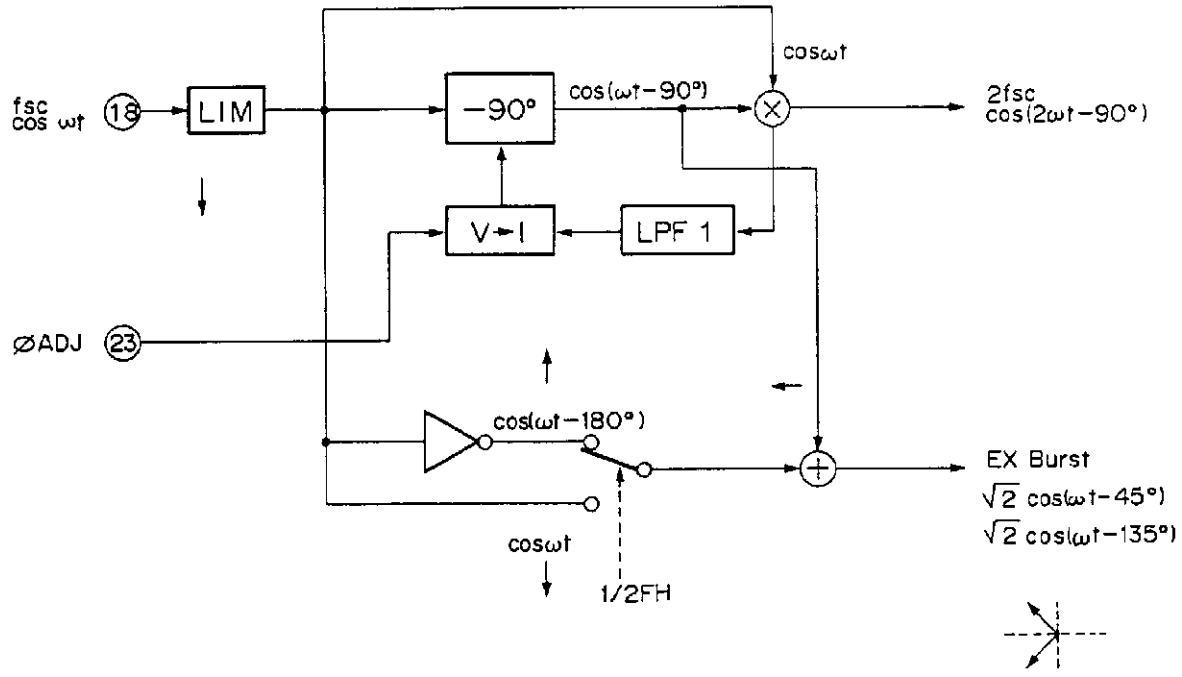


Fig. 2

The fsc −90° PLL consists of the −90° phase shifter, multiplier, LPF (low pass filter) 1 and V/I converter. A signal delayed by 90° to the fsc is obtained in this PLL. By changing the DC voltage at pin 23, the amount of phase shift is varied, allowing adjustment of the phase of the EX burst and the duty (DC offset) of the 2 fsc. By applying 5 V at pin 23, the internally fixed phase shift is obtained. The 2 fsc is produced from the multiplier output (× 2 output).

The EX burst is produced by adding the fsc (or inverted fsc) to the fsc with 90° delay produced in the −90° PLL.

The fsc and the inverted fsc are switched in a period of 1/2 fH, so the phase of the EX burst changes every 1 H.

3. SQ DET (Sequence Detector)

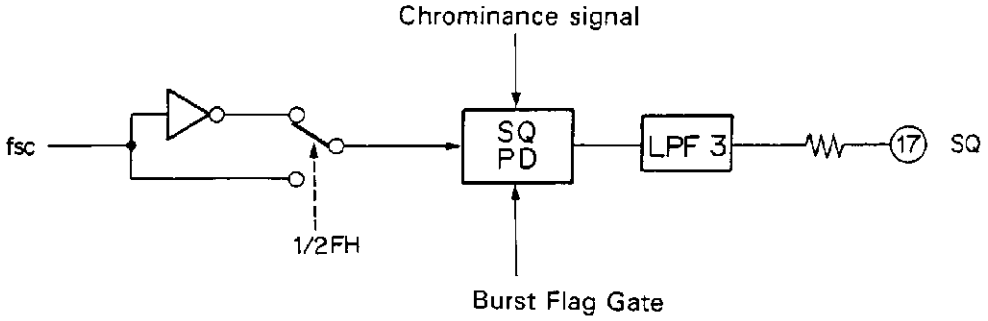
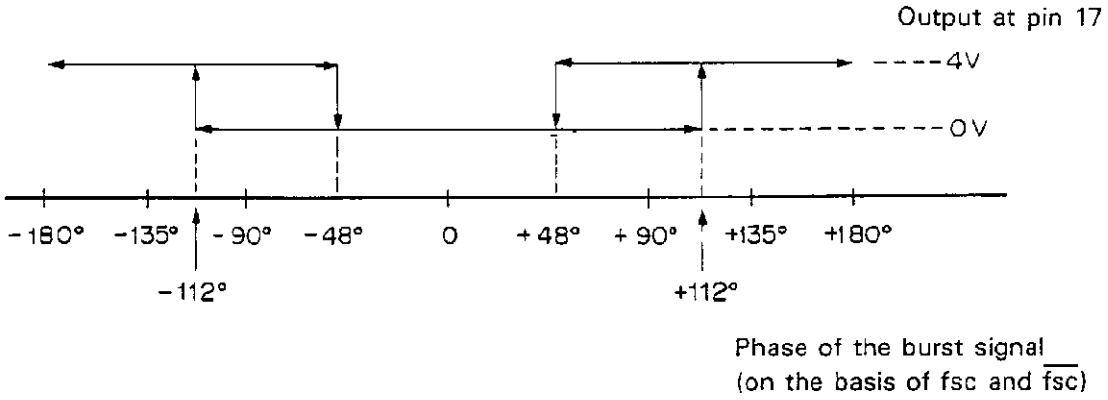


Fig. 3

The SQ DET detects the color alignment of the chrominance signal. The SQ PD is the phase detector which operates for a burst period only. This detects the color alignment by comparing the phase of the fsc signal inverted every 1 H with the phase of the burst of the chrominance signal.



The above figure shows the relation between the phase of the burst signal, the phase of the fsc ($\overline{fsc}$) and the output at pin 17 (SQ). As shown in the figure, the hysteresis angle is about 64°. If the relation is as shown in the figure below, the detector judges it as the correct sequence and set the output at pin 17 to HIGH.

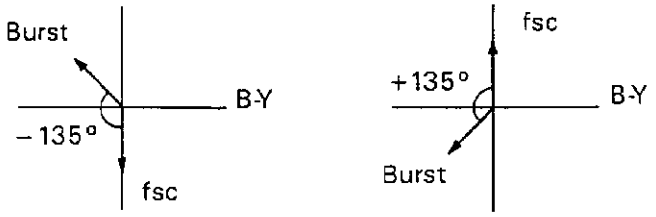


Fig. 5

Therefore, the center phase of the burst signal (about the B-Y axis) should be −90° to the fsc.

4. V-Invert (V Axis Inversion Circuit)

For color alignment, the DL signal which is produced by inverting the chrominance signal (TH signal) about the B-Y axis is necessary.

The V-Invert block produces the DL signal from the TH signal. Fig. 6 shows the principle of the V-Invert block.

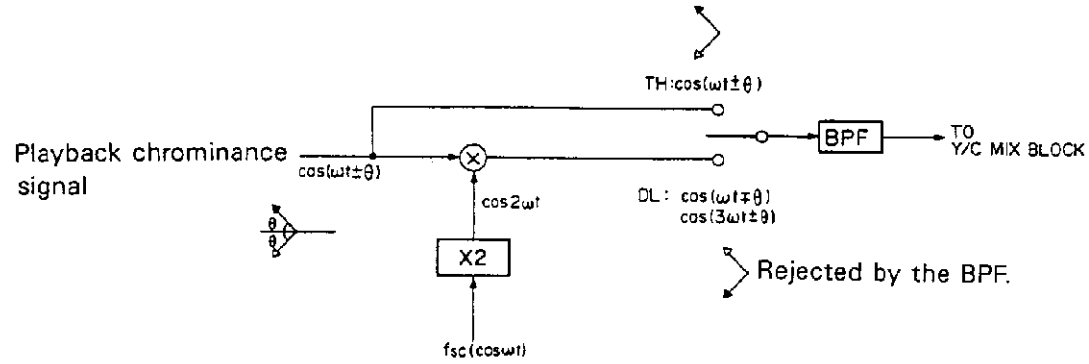


Fig. 6

Define the B-Y axis of the playback chrominance signal as cos ωt and input the playback chrominance signal and the 2 fsc (cos $2\omega t$) to the multiplier. By means of the frequency conversion of the 2 fsc, the input chrominance signal is inverted about the B-Y axis. The three fold frequency component (cos $3\omega t$) is also output, but this component is rejected by the BPF in a later stage.

Fig. 7 shows the actual V-Invert block.

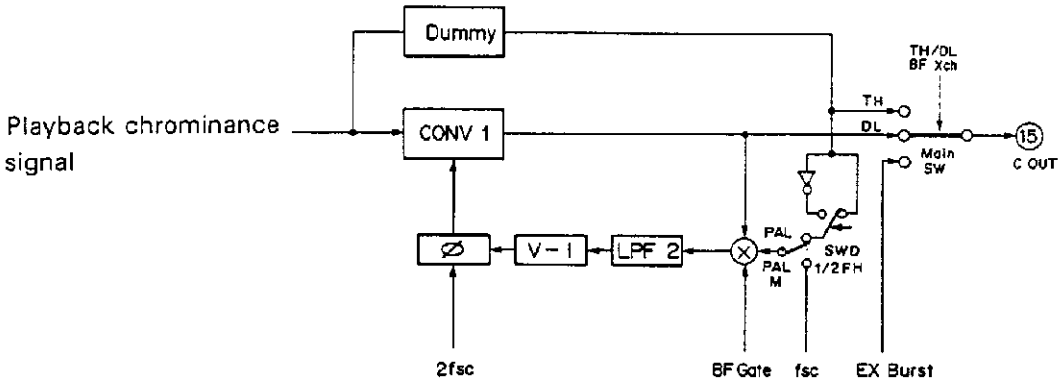


Fig. 7

The V-Invert circuit constructs the TH/DL APC loop that keep the phase difference between the burst of the TH signal and the burst of the DL signal to be 90°. This circuit detects the phase of the bursts of the TH and DL signals and varies the delay time of the phase shifter ϕ with reference to the error current of APC loop. In PAL-M mode, the APC is applied to the fsc and the DL signal. Therefore, the input burst signal has a phase of 90° to the fsc. The CONV 1 is a multiplier to obtain the DL signal.

The Dummy supplies the same gain loss and the same phase delay as produced in CONV 1 to the TH signal so that there is no gain and phase difference between the TH signal and the DL signal.

The main SW outputs the TH or DL signal according to the TH/DL select signal (output at pin 17). When a BF Xch pulse is supplied (in JOG mode only), the EX burst is output.

5. fH PLL

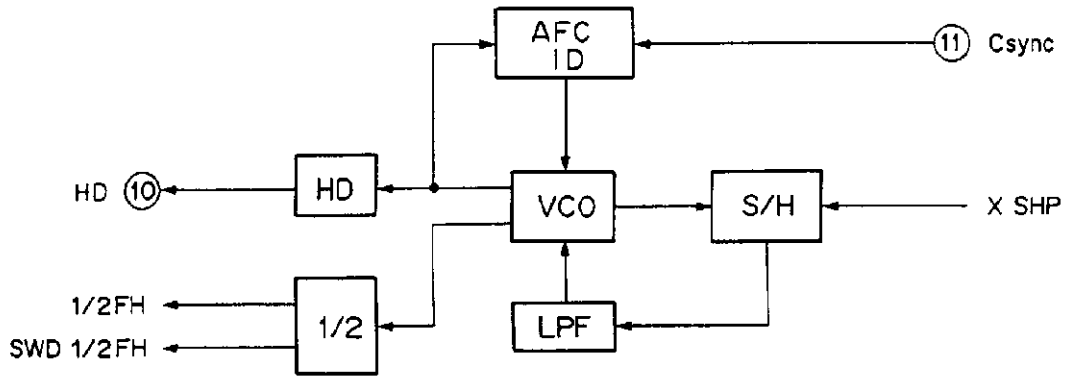


Fig. 8

The AFC ID compares the C sync frequency with the VCO frequency. When a frequency difference is present, the AFC ID outputs an up or down error and roughly compensates the VCO frequency. In this case, the AFC ID detects if the frequency difference continues for a period of 15H × 6 (5760 μs), and AFC ID error is available only when the frequency difference continues for that period.

The AFC ID also detects the existence of C sync. When the C sync is missing in various speed mode, the AFC ID cuts off its output and maintains the state immediately before the output cutout.

The phase lock of the C sync and VCO frequencies is carried out in the PLL loop composed of the S/H and LPF circuits.

6. BELL and C-BELL Filters

The Bell Filter is applied to the SECAM color TV signal to suppress the level near the chrominance subcarrier (F_{OR}, F_{OB}). In REC mode, the CXA1203 employs the BELL filter (having the inverted characteristics from the Bell Filter) to obtain the chrominance subcarrier of the same amplitude at every hue. The output signal from the BELL filter is sent to the record signal processing block of chrominance signal in the CXA1200.

In playback mode, the chrominance signal processed in the CXA1200 is input to the C-BELL (having the same characteristics as the Bell Filter) filter of the CXA1203 to equalize the input signal with the SECAM color TV signal. The output from the C-BELL filter is mixed with the Y signal in the CXA1200 and sent to the CXA1201. The typical input level of the BELL filter is 32 mVp-p, and that of the C-BELL filter is 83 mVp-p.

7. SECAM Detector Circuit

The SECAM detector circuit employed in the CXA1203 converts the chrominance subcarrier frequency* to a voltage, and detects the color system by the voltage variation: PAL system if no voltage variation is present, or SECAM system if the voltage varies every 1H. When the color alignment is carried out in SECAM mode, the SECAM ACK output (pin 3) is always set to HIGH by inputting the SECAM JUMP output (pin 7) to the DLDP (pin 6).

* PAL system: color burst signal (4.43361875 MHz)
SECAM system: line ID signal F_{OR}: 4.40625 MHz
F_{OB}: 4.25000 MHz

Application Circuit (For PAL/SECAM Mode)

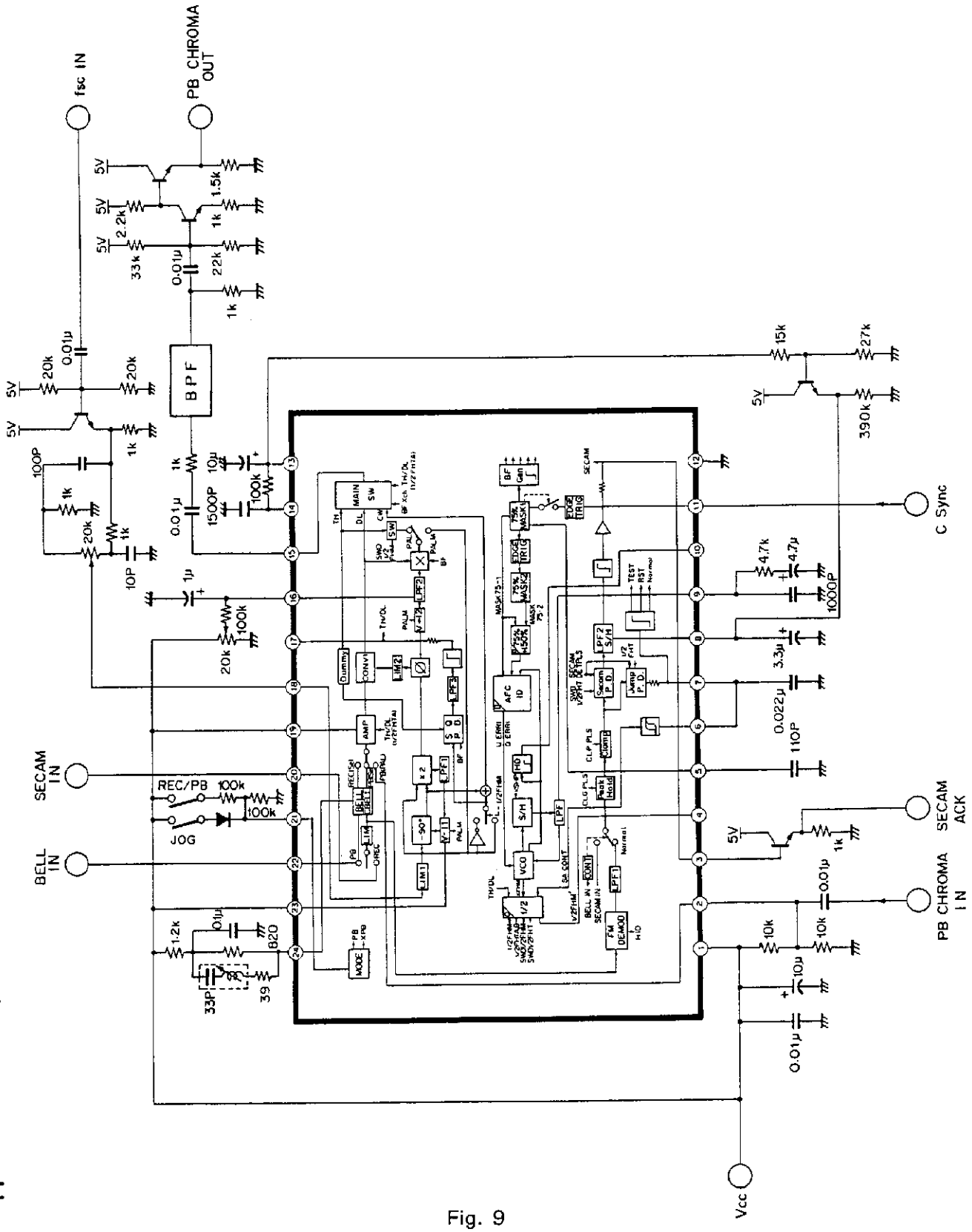


Fig. 9

Application Circuit (For PAL Mode Only)

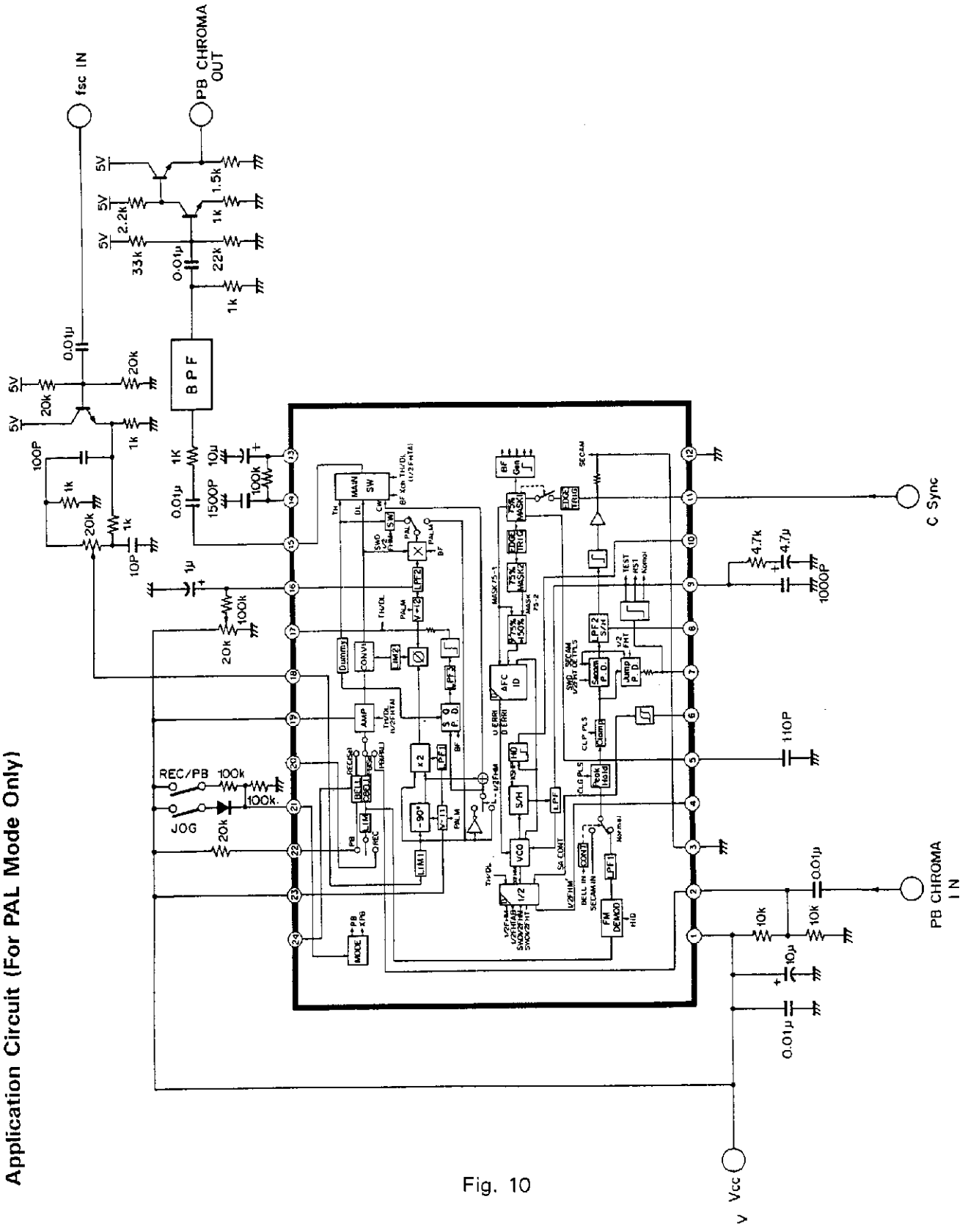


Fig. 10

Notes on Use

1. Phase Adjustment in PAL Playback Mode

The phase of the EX burst signal can be adjusted with the phase of the input fsc (chrominance subcarrier). The phase of the DL signal can be adjusted by applying a current to pin 16. Adjust the phase of the fsc so that the phase of the EX burst signal in JOG playback mode matches the phase of the color burst signal in normal playback mode at the PB CHROMA output (pin 15). Then, adjust the current to be applied to pin 16 so that the DL signal becomes symmetrical to the TH signal about the B-Y axis.

2. PAL-M mode

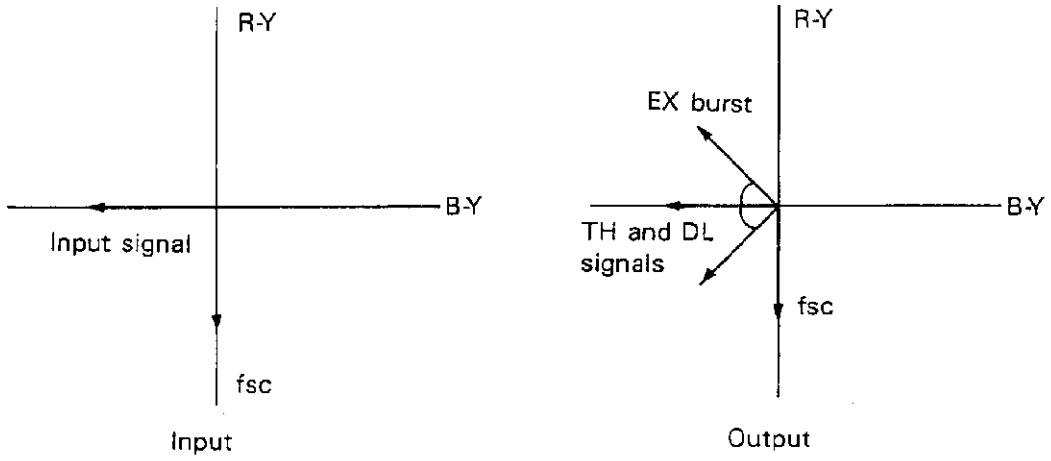


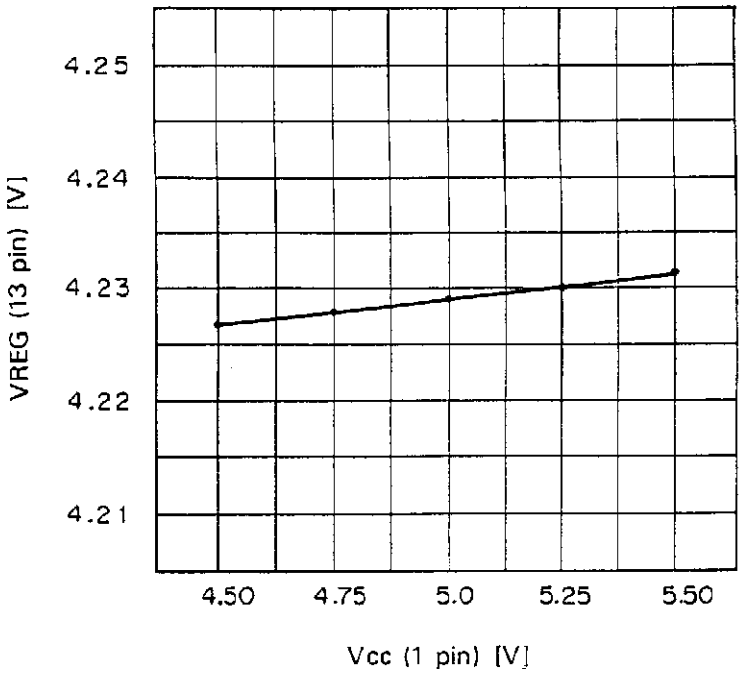
Fig. 11

Input an NTSC signal to pin 2, the fsc signal (3.58 MHz) to pin 18 and the C sync signal (15.75 MHz) to pin 11. Then the PAL-M playback signal is obtained at PB CHROMA output (pin 15). To adjust the phase, first input a burst signal with the same phase as the B-Y axis, and adjust the phase of the fsc to be input so that the phase of the TH signal matches the center phase of the EX burst at pin 15. Then adjust the current to be applied to pin 16 so that the phase of the DL signal matches the center phase of the EX burst. In PAL-M mode, pin 17 (SQ ID) should be fixed to L.

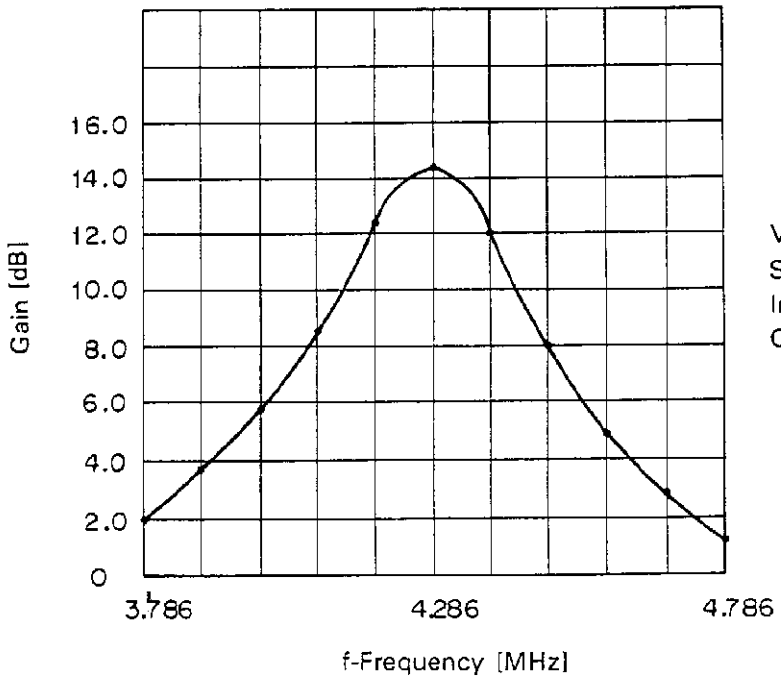
3. PAL Only Mode

In PAL only mode, a part of the SECAM detector block is turned off by fixing pin 22 (BELL IN) to H. This reduces the current consumption to 1.2 mA. The connections for other pins are the same as shown in Fig. 10 "Application Circuit (PAL only mode)".

V REG supply voltage characteristic

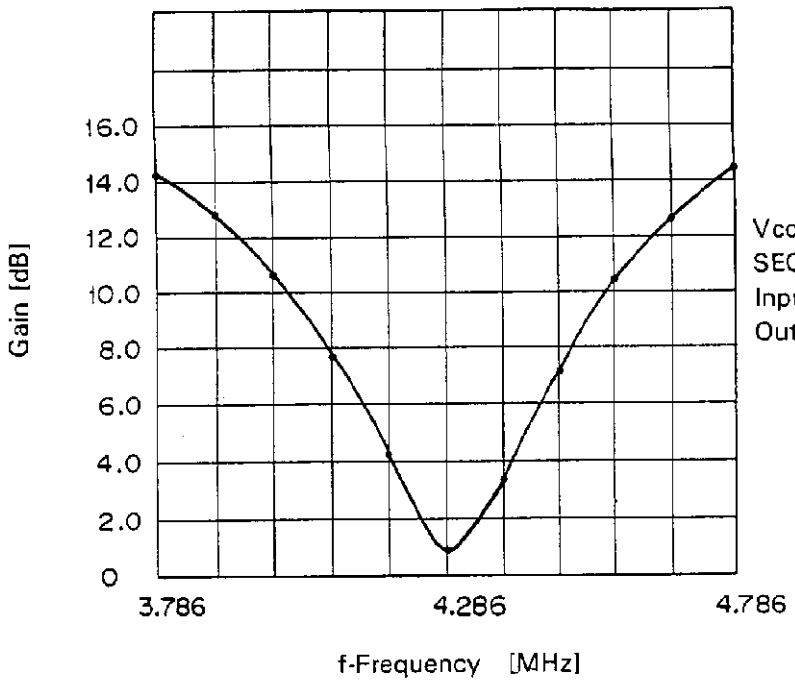


BELL filter characteristic



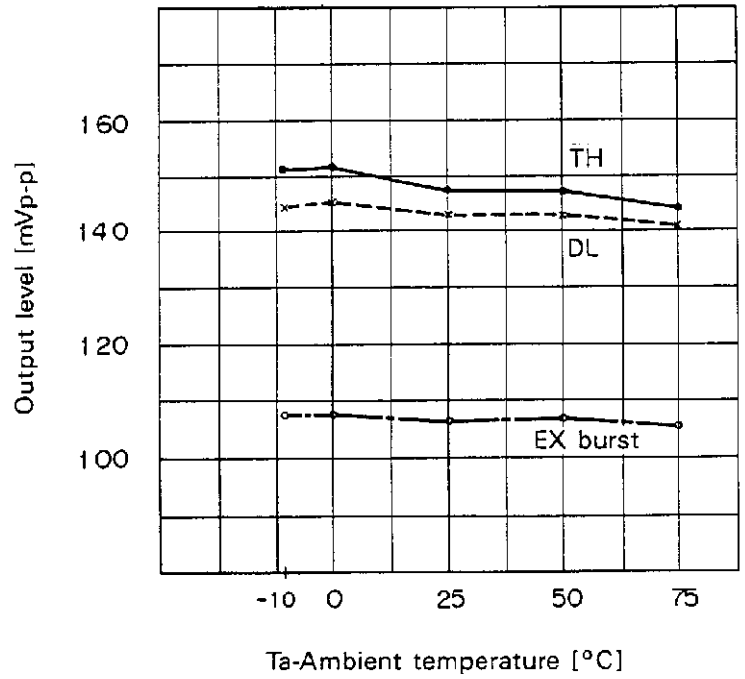
Vcc = 5.0 V
SECAM/REC mode
Input level: 32 mVp-p (BELL IN)
Output: C OUT (pin 15)

C-BELL filter characteristic



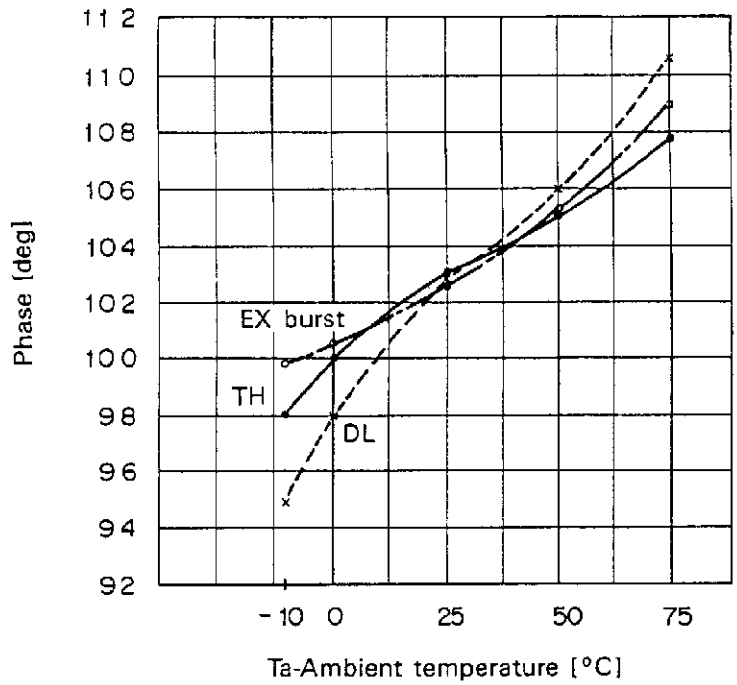
Vcc = 5.0 V
SECAM/PB mode
Input level: 83 mVp-p (BELL IN)
Output: C OUT (pin 15)

TH/DL/EX burst output levels vs. Ambient temperature



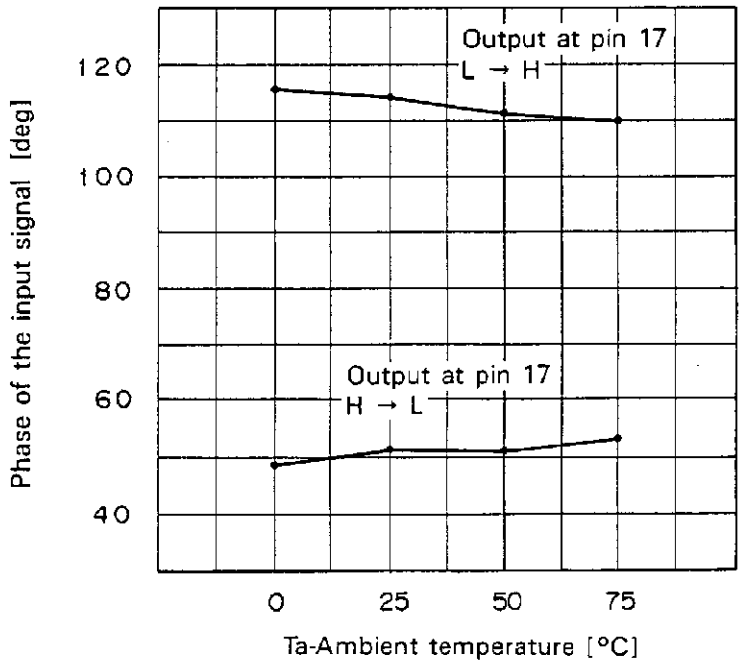
Vcc = 5.0 V
PAL/PB mode
Input level: 150 mVp-p (PB C IN)
fsc: 350 mVp-p
Output: 4.43 MHz BPF OUT
(The output level is the average during 2 H).

TH/DL/EX burst phases vs. Ambient temperature



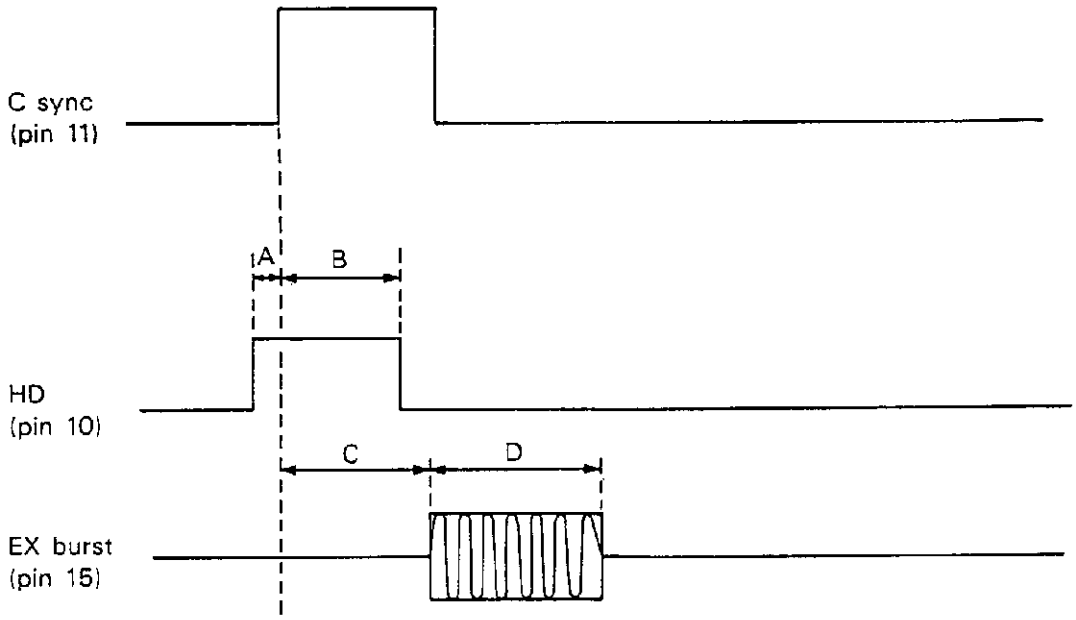
Vcc=5.0 V
PAL/PB mode
Input level: 150 mVp-p (PB C IN)
fsc: 350 mVp-p
Output: C OUT (pin 15)
The phase is the absolute value determined by measuring the center angle of the TL, DL or EX burst during 2 H with reference to the fsc (at pin 18).

SQ DET input/output vs. Ambient temperature

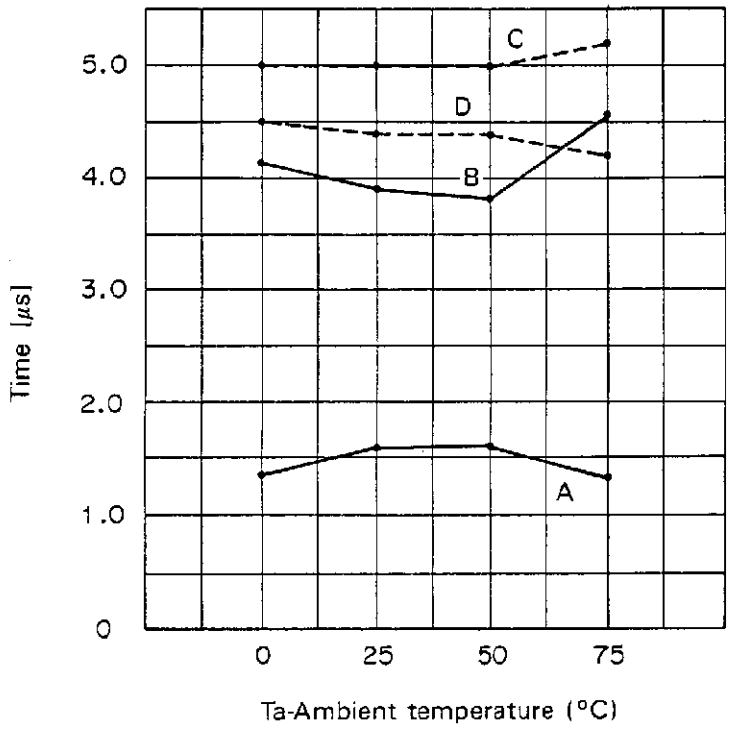


Vcc=5.0 V
PAL/RESET mode
Input level: 150 mVp-p (PB C IN)
fsc: 350 mVp-p
Output: SQ ID (pin 17)
(The phase of the input signal is the absolute value of the phase delay to the fsc. This is determined by delaying the phase of the input signal to the fsc and measuring the phase delay when the output changes.)

Relation of the phase of each pulse to the C sync singal



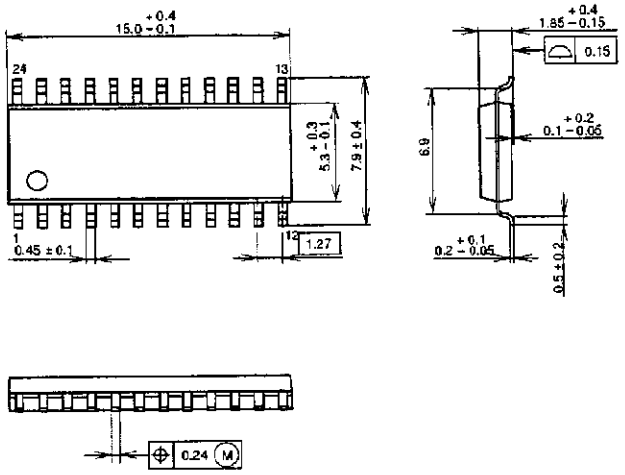
Phases of the HD and EX burst vs. Ambient temperature



Package Outline Unit : mm

CXA1203M

24PIN SOP (PLASTIC)



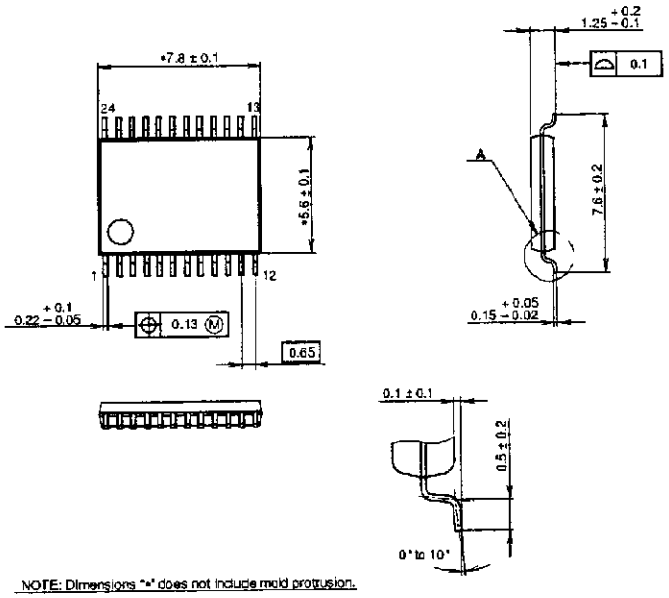
PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g

SONY CODE	SOP-24P-L01
EIAJ CODE	SOP024-P-0300
JEDEC CODE	———

CXA1203N

24PIN SSOP(PLASTIC)



NOTE: Dimensions "*" does not include mold protrusion.

DETAIL A

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	———

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).