

**SONY**

**CXA1737R**

**AFM Stereo Signal Processor for 8 mm VCR**

**Description**

The CXA1737R is a bipolar IC designed as an AFM stereo signal processor for 8mm VCR. All functions necessary for AFM stereo are concentrated onto a single 64-pin LQFP.

**Features**

- Low supply voltage (3.15V) design
- Low power consumption (Vcc = 3.15V)
  - Recording: 150mW
  - Playback: 240mW
- Built-in BPF (1.5MHz, 1.7MHz)
- Supports NTSC and PAL
- Enables both parallel and 3-line serial mode control
- Supports electronic volume (EVR) control

**Absolute Maximum Ratings**

- Supply voltage Vcc 5.25 V
- Operating temperature Topr -20 to +75 °C
- Storage temperature Tstg -65 to +150 °C
- Allowable power dissipation
 

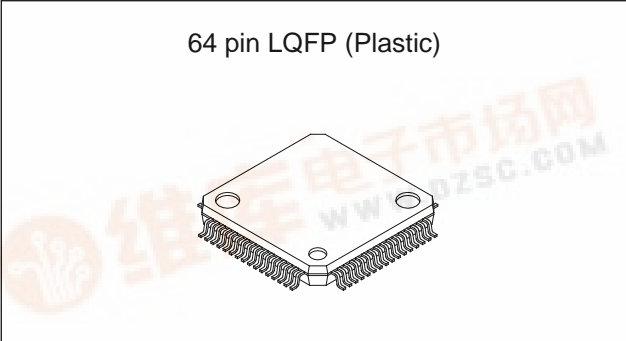
Pd	1500	mW
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**Operating Conditions**

- Recommended supply voltage
 

Vcc	3.15	V
VccH	4.75	V
- Supply voltage range
 

Vcc	3 to 5.25	V
VccH	4.5 to 5.25	V



**Structure**

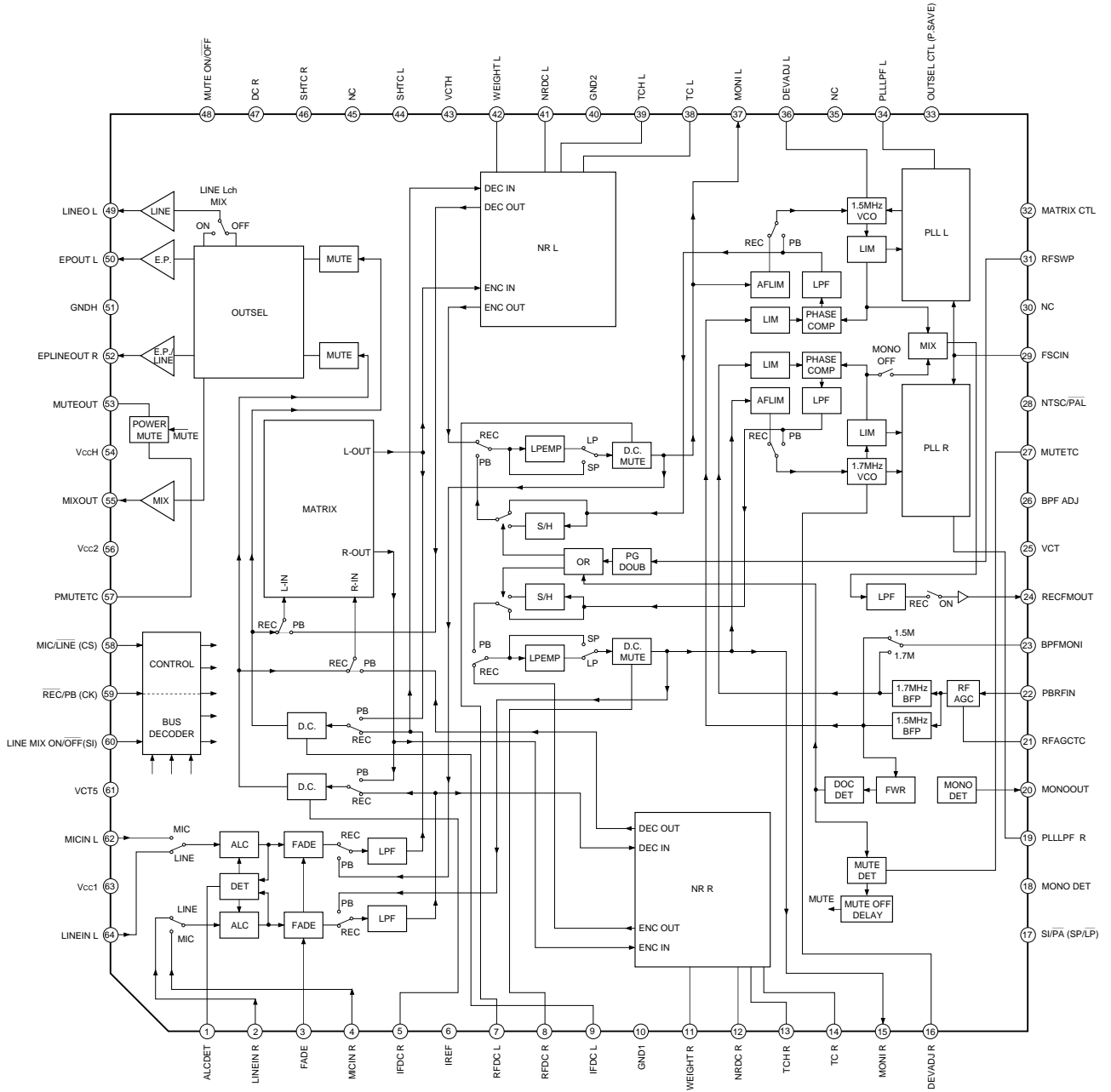
Bipolar silicon monolithic IC

**Applications**

8mm VCRs



Block Diagram



Pin Description

(Vcc1, Vcc2 = 3.15V, VccH = 4.75V, Ta = 27°C)

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
1	ALCDET	—	—		ALC time constant pin. ALC is OFF when this pin is low.
2	LINEIN R	1.23V	 Reference input -38dBm *1		Line input pin. Standard input level: -38dBm. This pin has a small input signal level and high input impedance. Therefore, be careful not to cause cross talk with other signals.
3	FADE	See Graph 1.	—		EVR control pin for fader. 0 to 0.5V with fixed gain. Increasing the applied voltage lowers the gain and causes the fader to operate.
4	MICIN R	1.23V	 Reference input -38dBm *1		Microphone input pin. Standard input level: -38dBm. This pin has a small input signal level and high input impedance. Therefore, be careful not to cause cross talk with other signals.

\*1 0dBm = 2.19Vp-p

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
5	IFDC R	1.90V	—		DC monitor pin of Rch signal path.
6	IREF	1.17V	—		Pin for generating the reference current. Connect a 47kΩ external resistor to GND. Be careful not to cause pin cross talk.
7	RFDC L	1.91V	—		DC monitor pin of Lch signal path.
8	RFDC R	1.91V	—		DC monitor pin of Rch signal path.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
9	IFDC L	1.90V	—		DC monitor pin of Lch signal path.
10	GND1	0V*1	—	—	Audio system GND pin.
11	WEIGHT R	1.23V	—		NR WEIGHT time constant pin.
12	NRDC R	1.73V	—		DC offset cancel pin of NR block.

\*1 Externally applied voltage


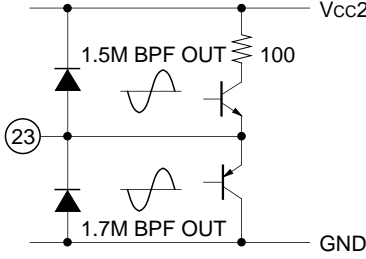

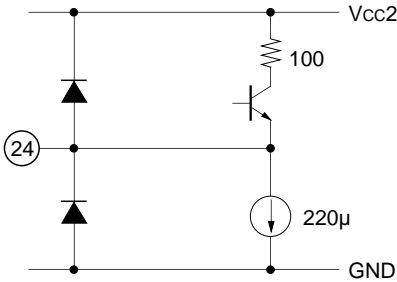
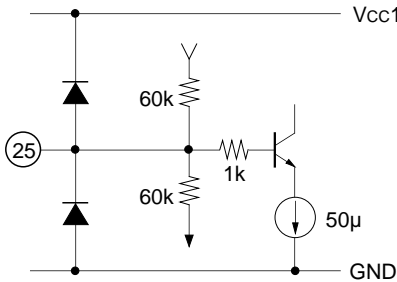
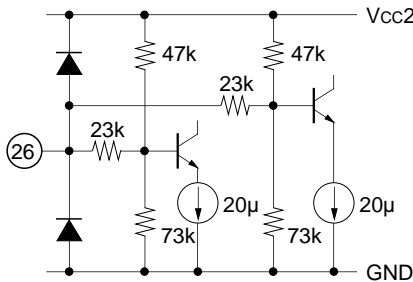
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
13	TCH R	0.56V	—		NR attack/ recovery time constant pins.
14	TC R	1.19V	—		
15	MONI R	1.89V	 Reference output -15dBm *1		
16	DEVADJ R	See Graph 4.	—		

\*1 0dBm = 2.19Vp-p

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description				
		DC	AC						
17	SI/ $\overline{\text{PA}}$ (SP/ $\overline{\text{LP}}$ )	—	—		<p>Serial/ parallel (SP/ <math>\overline{\text{LP}}</math>) mode switching pin. When this pin is 4.3V or more, the IC operates in serial control mode and mode control for the IC is performed by CS, CK and SI of Pins 58, 59 and 60. When this pin is 3.5V or less, the IC operates in parallel control mode as follows.</p> <table border="1"> <tr> <td>L (0 to 1V)</td> <td>LP</td> </tr> <tr> <td>H (2 to 3.5V) or OPEN</td> <td>SP</td> </tr> </table>	L (0 to 1V)	LP	H (2 to 3.5V) or OPEN	SP
L (0 to 1V)	LP								
H (2 to 3.5V) or OPEN	SP								
18	MONO DET	2.47V	—		MONO DET time constant pin.				
19	PLLLPF R	—	—		PLL time constant pin. Since this pin has a small attraction and discharge current, signals should be received with high impedance when monitoring this pin. Also, be careful not to cause pin cross talk.				

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
20	MONOOUT	—	—		<p>MONODET discrimination output pin. This pin is open collector, and it is pulled up to Vcc with 100kΩ resistor. During parallel mode, this pin is also recording bilingual control input pin.</p> <ul style="list-style-type: none"> <li>• Specification for parallel CTL</li> </ul> <p>During recording: Bilingual recording mode when this pin is set to low (0 to 1 V) during low of Pin 32 (REC MONO mode).</p> <p>During playback: Outputs MONO discrimination result. Open for MONO; Low for others.</p> <ul style="list-style-type: none"> <li>• Specification for serial CTL</li> </ul> <p>See Mode Control Tables of 3) SO control mode table.</p>
21	RFAGCTC	2.48V	—		RFAGC time constant pin.
22	PBRFIN	—	 Reference input AFM 15mVp-p (1.5MHz)		<p>Input pin for PB RF signal. The reference input level is approximately 200mVp-p (Y + C + AFM). Note that the reference input level of AFM 1.5MHz component is 15mVp-p.</p>



Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
23	BPFMONI	During 1.5M BPF monitoring 1.09V  During 1.7M BPF monitoring 2.51V	 Reference output 1.5M BPF = 180mVp-p 1.7M BPF = 190mVp-p		This pin is for measurement which monitors the BPF output. For monitoring 1.5M BPF characteristics, connect 4.7kΩ resistor to GND. For monitoring 1.7M BPF characteristics, connect 4.7kΩ resistor to Vcc.
24	RECFMOUT	0.96V	 1.5M + 1.7M reference output		Recording FM modulated output pin. Reference output is 220mVp-p for 1.5M component; 175mVp-p for 1.7M component.
25	VCT	1.89V	—		IC internal bias pin. Connect a decoupling capacitor.
26	BPF ADJ	See Graph 2.	—		Pin for varying the BPF fo. The variable width is 0 to Vcc.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description				
		DC	AC						
27	MUTETC	2.43V	—		<p>Time constant pin for determining the MUTE OFF delay time. MUTE ON when drop out (T) continues approximately 1ms (during 680pF externally).</p>				
28	NTSC/ PAL	—	—		<p>NTSC/<math>\overline{\text{PAL}}</math> switching pin during parallel mode.</p> <table border="1"> <tr> <td>L (0 to 1V)</td> <td>PAL</td> </tr> <tr> <td>H (2V to Vcc)</td> <td>NTSC</td> </tr> </table>	L (0 to 1V)	PAL	H (2V to Vcc)	NTSC
L (0 to 1V)	PAL								
H (2V to Vcc)	NTSC								
29	FSCIN	1.68V	 Reference input 200mVp-p		<p>fsc input pin. The input level is approximately 200mVp-p. During NTSC: 3.579545MHz During PAL: 4.433619MHz</p>				
30	NC	—	—		—				
31	RFSWP	—	 Reference input 30Hz		<p>RFSWP input pin.</p>				

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description																		
		DC	AC																				
32	MATRIX CTL	—	—		<p>MATRIX control input pin during parallel mode.</p> <table border="1"> <thead> <tr> <th rowspan="2">Pin 32</th> <th colspan="2">During parallel</th> <th rowspan="2">During serial</th> </tr> <tr> <th>REC</th> <th>PB</th> </tr> </thead> <tbody> <tr> <td>L (0 to 0.7V)</td> <td>MONO</td> <td>Bilingual/ MONO Auto</td> <td>REC MONO</td> </tr> <tr> <td>M (1.3 to 1.7V) or OPEN</td> <td>STEREO</td> <td>STEREO/ MONO Auto</td> <td>—</td> </tr> <tr> <td>H (2.3V to Vcc)</td> <td>STEREO</td> <td>STEREO</td> <td>—</td> </tr> </tbody> </table>	Pin 32	During parallel		During serial	REC	PB	L (0 to 0.7V)	MONO	Bilingual/ MONO Auto	REC MONO	M (1.3 to 1.7V) or OPEN	STEREO	STEREO/ MONO Auto	—	H (2.3V to Vcc)	STEREO	STEREO	—
Pin 32	During parallel		During serial																				
	REC	PB																					
L (0 to 0.7V)	MONO	Bilingual/ MONO Auto	REC MONO																				
M (1.3 to 1.7V) or OPEN	STEREO	STEREO/ MONO Auto	—																				
H (2.3V to Vcc)	STEREO	STEREO	—																				
33	OUTSEL CTL (P.SAVE)	—	—		<p>OUTPUT SEL control input pin during parallel mode.</p> <table border="1"> <thead> <tr> <th>Pin 33</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>L (0 to 0.7V)</td> <td>Lch/ Rch</td> </tr> <tr> <td>M (1.3 to 1.7V) or OPEN</td> <td>Lch/ Rch (Main)</td> </tr> <tr> <td>H (2.3 to 3.5V)</td> <td>Lch/ Rch (SUB)</td> </tr> <tr> <td>H2 (4.3V to VccH)</td> <td>Power save 1.5M BPF through</td> </tr> </tbody> </table>	Pin 33	Mode	L (0 to 0.7V)	Lch/ Rch	M (1.3 to 1.7V) or OPEN	Lch/ Rch (Main)	H (2.3 to 3.5V)	Lch/ Rch (SUB)	H2 (4.3V to VccH)	Power save 1.5M BPF through								
Pin 33	Mode																						
L (0 to 0.7V)	Lch/ Rch																						
M (1.3 to 1.7V) or OPEN	Lch/ Rch (Main)																						
H (2.3 to 3.5V)	Lch/ Rch (SUB)																						
H2 (4.3V to VccH)	Power save 1.5M BPF through																						
34	PLLLPF L	1.75V	—		<p>PLL time constant pin. Since this pin has a small attraction and discharge current, signals should be received with high impedance when monitoring this pin. Also, be careful not to cause pin cross talk.</p>																		
35	NC	—	—		—																		
36	DEVADJ L	See Graph 3.	—		<p>Deviation adjusting pin. The variable width is from 0 to Vcc.</p>																		

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
37	MONI L	1.88V	Reference output -15dBm <sup>*1</sup>		Pin for monitoring the signal before modulation during recording and after demodulation during playback of Lch.
38	TC L	1.19V	—		NR attack/ recovery time constant pins.
39	TCH L	0.56V	—		
40	GND2	0V <sup>*2</sup>	—	—	RF system GND pin.
41	NRDC L	1.74V	—		NR block DC offset cancel pin.

\*1 0dBm = 2.19Vp-p

\*2 Externally applied voltage

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
42	WEIGHT L	1.23V	—		NR WEIGHT time constant pin.
43	VCTH	1.89V	—		RF system reference bias pin. Connect a decoupling capacitor.
44	SHTC L	1.89V	—		S/H time constant pin.
45	NC	—	—	—	—
46	SHTC R	1.89V	—		S/H time constant pin.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description				
		DC	AC						
47	DC R	1.92V	—		<p>Rch DC check pin. Be careful not to cause pin cross talk.</p>				
48	MUTE ON/ OFF	—	—		<p>Mute control pin.</p> <table border="1"> <tr> <td>L (0 to 1V)</td> <td>MUTE OFF</td> </tr> <tr> <td>H (2V to Vcc) or OPEN</td> <td>MUTE ON</td> </tr> </table> <p>Mute control is possible during both serial and parallel modes.</p>	L (0 to 1V)	MUTE OFF	H (2V to Vcc) or OPEN	MUTE ON
L (0 to 1V)	MUTE OFF								
H (2V to Vcc) or OPEN	MUTE ON								
49	LINE OUT L	2.04V	 Reference output -7dBm *1		<p>LINEOUT pin. Set the load to 47kΩ or more.</p>				
50	EPOUT L	2.04V	 Reference output -7dBm *1		<p>EPOUT pin. This pin can drive a load of 120Ω.</p>				

\*1 0dBm = 2.19Vp-p


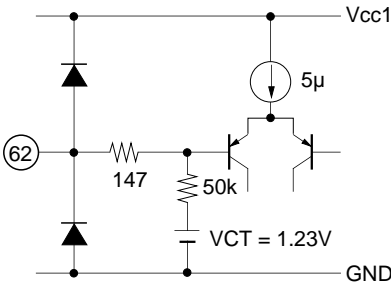

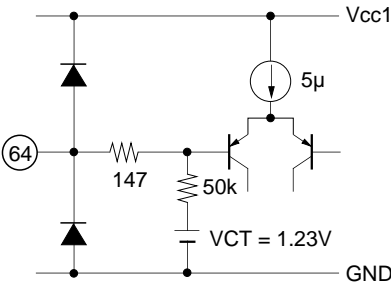
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
51	GNDH	0V*2	—	—	Output buffer system GND pin.
52	EPLINEOUT R	2.04V	Reference output -7dBm *1		LINE/ EPOUT pin. This pin can drive a load of 120Ω.
53	MUTEOUT	0V	—		MUTEOUT pin. This pin outputs current during muting and power ON/OFF to operate the external SW Tr.
54	VccH	4.75V*2	—	—	Output buffer system power supply pin.
55	MIXOUT	2.06V	Reference output -7dBm *1		MIXOUT pin. Set the load to 47kΩ or more.
56	Vcc2	3.15V*2	—	—	RF system power supply pin.
57	PMUTETC	4.70V	—		Time constant pin for deciding the power ON/OFF mute time.

\*1 0dBm = 2.19Vp-p

\*2 Externally applied voltage

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description				
		DC	AC						
58	MIC/ $\overline{\text{LINE}}$ (CS)	—	—		<p>MIC/ <math>\overline{\text{LINE}}</math> switching pin during parallel mode.</p> <table border="1"> <tr> <td>L (0 to 1V) or OPEN</td> <td>LINE</td> </tr> <tr> <td>H (2V to Vcc)</td> <td>MIC</td> </tr> </table> <p>CS input pin during serial mode.</p>	L (0 to 1V) or OPEN	LINE	H (2V to Vcc)	MIC
L (0 to 1V) or OPEN	LINE								
H (2V to Vcc)	MIC								
59	$\overline{\text{REC}}$ / PB (CK)	—	—		<p><math>\overline{\text{REC}}</math>/ PB switching pin during parallel mode.</p> <table border="1"> <tr> <td>L (0 to 1V) or OPEN</td> <td>REC</td> </tr> <tr> <td>H (2V to Vcc)</td> <td>PB</td> </tr> </table> <p>CK input pin during serial mode.</p>	L (0 to 1V) or OPEN	REC	H (2V to Vcc)	PB
L (0 to 1V) or OPEN	REC								
H (2V to Vcc)	PB								
60	LINE MIX ON/ $\overline{\text{OFF}}$ (SI)	—	—		<p>LINE MIX ON/ <math>\overline{\text{OFF}}</math> switching pin during parallel mode.</p> <table border="1"> <tr> <td>L (0 to 1V) or OPEN</td> <td>MIX OFF</td> </tr> <tr> <td>H (2V to Vcc)</td> <td>MIX ON</td> </tr> </table> <p>SI input pin during serial mode.</p>	L (0 to 1V) or OPEN	MIX OFF	H (2V to Vcc)	MIX ON
L (0 to 1V) or OPEN	MIX OFF								
H (2V to Vcc)	MIX ON								
61	VCT5	2.00V	—		<p>IC internal bias pin. Connect a decoupling capacitor.</p>				



Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
62	MICIN L	1.23V	 Reference input -38dBm *1		Microphone input pin. Standard input level: -38dBm. This pin has a small input signal level and high input impedance. Therefore, be careful not to cause cross talk with other signals.
63	Vcc1	3.15V*2	—	—	Audio system power supply pin.
64	LINEIN L	1.23V	 Reference input -38dBm *1		Line input pin. Standard input level: -38dBm. This pin has a small input signal level and high input impedance. Therefore, be careful note to cause cross talk with other signals.

\*1 0dBm = 2.19Vp-p

\*2 Externally applied voltage

(Vcc1, Vcc2 = 3.15V, VccH = 4.75V, Ta = 27°C) (Unless otherwise specified, SW 1, 2, 3, 4, 16, 22, 23, 26, 29, 31, 36, 44, 46, 52, 62, and 64 are b.)

**Electrical Characteristics**

No.	Item	Symbol	Measurement input signal conditions			Reference signal source		Control voltage	Switch condition	Mode condition	Measurement point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level									
1	Current consumption 1 during recording Vcc1 + Vcc2 systems	IREC1					—		A	11	During serial mode no signal	25	35	45	mA	
2	Current consumption 2 during recording VccH system	IREC2					—		A	12	During serial mode no signal	6	9	12	mA	
3	Current consumption 1 during playback Vcc1 + Vcc2 systems	IPB1					—		B	11	During serial mode no signal	47	63	79	mA	
4	Current consumption 2 during playback VccH system	IPB2					—		B	12	During serial mode no signal	6	9	12	mA	
5	MIC IN reference output level	VLNOL VLNOR	SG62	-38dBm	1kHz		—	4, 62 = a	A	Pin 49			-8	-7	-6	dBm
			SG4						Pin 52							
6	MIC IN reference output level R/L difference	BAC1	SG62	-38dBm	1kHz		—	4, 62 = a	A	—	VLNOR/VLNOL	-0.55	0	+0.55	dB	
			SG4													
7	MIC IN reference output distortion factor	HLNOL HLNOR	SG62	-38dBm	1kHz		—	4, 62 = a	A	Pin 49	Measure the THD to the 10th		—	0.02	0.1	%
			SG4						Pin 52							
8	MIC IN output noise	NLNL NLNR					—		A	Pin 49	A weight		—	-72	-70	dBm
									Pin 52							
9	LINE IN reference output level	VLNOLL VLNOLR	SG64	-38dBm	1kHz		—	2, 64 = a	G	Pin 49			-8	-7	-6	dBm
			SG2						Pin 52							
10	LINE IN reference output level R/L difference	BACL1	SG64	-38dBm	1kHz		—	2, 64 = a	G	—	VLNOLR/VLNOLL	-0.55	0	+0.55	dB	
			SG2													
11	LINE IN reference output distortion factor	HLNOLL HLNOLR	SG64	-38dBm	1kHz		—	2, 64 = a	G	Pin 49	Measure the THD to the 10th		—	0.02	0.1	%
			SG2						Pin 52							
12	LINE IN output noise	NLNLL NLNLR					—		G	Pin 49	A weight		—	-72	-70	dBm
									Pin 52							
13	ALC level 1 (REF + 20dB)	VALCL20 VALCR20	SG62	-18dBm	1kHz		—	4, 62 = a	A	Pin 49			-5.0	-2.1	+1.0	dBm
			SG4						Pin 52							

No.	Item	Symbol	Measurement input signal conditions			Reference signal source			Control voltage	Switch condition	Mode condition	Measure-ment point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level	Frequency									
14	ALC level 2 (REF + 36dB)	VALCL36	SG62	-2dBm	1kHz					A	Pin 49		-3.0	-1.9	+3.0	dBm	
		VALCR36	SG4							Pin 52							
15	ALC maximum input distortion factor (REF + 36dB)	HALCHL	SG62	-2dBm	1kHz					A	Pin 49	Measure the THD to the 10th	0.0	0.35	1.0	%	
		HALCHR	SG4							Pin 52							
16	ALC effects (+36dB/+20dB)	VALCL23	SG62	-2dBm	1kHz					A		VALCL36/VALCL20 VALCR36/VALCR20	0.0	0.2	—	dB	
		VALCR23	SG4	-18dBm													
17	E-E system maximum output level	VLNMXL	SG62	VAL	1kHz					A	Pin 49	Output level when THD = 1%	—	—	0.5	dBm	
		VLNMXR	SG4							Pin 52							
18	FADER maximum attenuation	VFAL	SG62	-38dBm	1kHz			V3 = 2.5V		A	Pin 49	A weight	—	-74	-69	dBm	
		VFAR	SG4							Pin 52							
19	FADER dead voltage level	VFALOL	SG62	-38dBm	1kHz			V3 = 0.5V		A	Pin 49	VFALOL/VLNOL	-0.5	0	0.5	dB	
		VFALOR	SG4							Pin 52	VFALOR/VLNOR						
20	E-E system frequency response 1 (20kHz/1kHz)	FLNL20	SG62	-38dBm	20kHz /1kHz					A	Pin 49	FLNL20/VLNOL	-3	-0.5	1	dB	
		FLNR20	SG4							Pin 52	FLNR20/VLNOR						
21	E-E system frequency response 2 (50kHz/1kHz)	FLNL50	SG62	-38dBm	50kHz /1kHz					A	Pin 49	FLNL50/VLNOL	—	-11	-5	dB	
		FLNR50	SG4							Pin 52	FLNR50/VLNOR						
22	Input cross talk 1 between MIC and LINE	VCTL1	SG62	-28dBm	1kHz					G	Pin 49	Cross talk of MIC → LINE	—	-71	-66	dBm	
		VCTR1	SG4							Pin 52	A weight						
23	Input cross talk 2 between MIC and LINE	VCTL2	SG64	-28dBm	1kHz					A	Pin 49	Cross talk of LINE → MIC	—	-71	-66	dBm	
		VCTR2	SG2							Pin 52	A weight						
24	E-E system channel input cross talk 1	VCTLR1	SG62	-28dBm	1kHz					A	Pin 52	Cross talk of L → R	—	-73	-67	dBm	
		VCTLR2	SG4							Pin 49	A weight						
25	E-E system channel input cross talk 2	VCTLRR	SG4	-28dBm	1kHz					A	Pin 49	Cross talk of R → L	—	-73	-67	dBm	
		VCTLRL	SG4							Pin 52	A weight						
26	E-E system MUTE attenuation	VLNML	SG62	-28dBm	1kHz					E	Pin 49	Output level during MUTE ON	—	-90	-80	dBm	
		VLNMR	SG4							Pin 52	A weight						
27	E-E system MUTE switching level output difference	VMDCL								A/E	TP49	E-E system output DC level difference during MUTE ON/OFF.	-100	0	+100	mVpp	
		VMDCR								P52A							

No.	Item	Symbol	Measurement input signal conditions			Reference signal source			Control voltage	Switch condition	Mode condition	Measurement point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level	Frequency									
28	NR encode reference output level	VNRL38 VNRR38	SG62	-38dBm	1kHz					4, 62 = a	H	Pin 37	BIL REC mode	-17	-15	-13	dBm
			SG4									Pin 15					
29	NR encode linearity (-78dBm/-38dBm)	VNRL78 VNRR78	SG62	-78dBm	1kHz					4, 62 = a	H	Pin 37	BIL REC mode VNRL78/VNRL38 VNRR78/VNRR38	-23	-22	-21	dB
			SG4	-38dBm								Pin 15					
30	NR encode frequency response during SP (10kHz/1kHz)	FNRL10 FNRR10	SG62	-38dBm	10kHz					4, 62 = a	H	Pin 37	BIL REC mode FNRL10/VNRL38 FNRR10/VNRR38	3.7	4.9	5.8	dB
			SG4		/1kHz							Pin 15					
31	NR LP emphasis frequency response 1 during LP 2kHz (LP/SP)	FLPL2 FLPR2	SG62	-38dBm	2kHz					4, 62 = a	I/H	Pin 37	BIL REC mode Ratio of LP/SP	1	2	3	dB
			SG4									Pin 15					
32	NR LP emphasis frequency response 2 during LP 10kHz (LP/SP)	FLPL10 FLPR10	SG62	-38dBm	10kHz					4, 62 = a	I/H	Pin 37	BIL REC mode Ratio of LP/SP	2.5	3	3.5	dB
			SG4									Pin 15					
33	REC FM oscillation frequency 1.5MHz (NTSC)	FVCOL1	SG29	200mVp-p	3.579545MHz				29 = a	A	Pin 24		1.4995	1.5	1.5005	MHz	
34	REC FM oscillation frequency 1.7MHz (NTSC)	FVCOR1	SG29	200mVp-p	3.579545MHz				29 = a	A	Pin 24		1.6995	1.7	1.7005	MHz	
35	REC FM oscillation frequency 1.5MHz (PAL)	FVCOL2	SG29	200mVp-p	4.433619MHz				29 = a	D	Pin 24		1.4995	1.5	1.5005	MHz	
36	REC FM oscillation frequency 1.7MHz (PAL)	FVCOR2	SG29	200mVp-p	4.433619MHz				29 = a	D	Pin 24		1.6995	1.7	1.7005	MHz	
37	REC FM output level Lch (1.5MHz)	VFML	SG29	200mVp-p	3.579545MHz				29 = a	A	Pin 24	Measure 1.5MHz carrier level	198	220	245	mVp-p	
38	REC FM output secondary distortion Lch (1.5MHz)	VFMHL2	SG29	200mVp-p	3.579545MHz				29 = a	A	Pin 24	More than 10kΩ load VFMHL2/VFML	—	-50	-25	dB	
39	REC FM output ternary distortion Lch (1.5MHz)	VFMHL3	SG29	200mVp-p	3.579545MHz				29 = a	A	Pin 24	More than 10kΩ load VFMHL3/VFML	—	-45	-30	dB	

No.	Item	Symbol	Measurement input signal conditions			Reference signal source			Control voltage	Switch condition	Mode condition	Measure-ment point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level	Frequency									
40	REC FM output level Rch (1.7MHz)	VFMR	SG29	200mVp-p	3.579545MHz			—	29 = a	A	Pin 24	Measure 1.7MHz carrier level	157	175	194	mVp-p	
41	REC FM output secondary distortion Rch (1.7 MHz)	VFMHR2	SG29	200mVp-p	3.579545MHz			—	29 = a	A	Pin 24	More than 10kΩ load VFMHR2/VFMR	—	-45	-25	dB	
42	REC FM output ternary distortion Rch (1.7MHz)	VFMHR3	SG29	200mVp-p	3.579545MHz			—	29 = a	A	Pin 24	More than 10kΩ load VFMHR3/VFMR	—	-45	-30	dB	
43	REC FM output level L/R mix ratio	VCOMIX	SG29	200mVp-p	3.579545MHz			—	29 = a	A	Pin 24	Stereo VFML/VFMR	1.25	1.7	2.35	dB	
44	BPF ADJ voltage	VBPAJ	SG22	15mVp-p	1.625MHz	SG29	200mVp-p	V26 = VAL	22, 26, 29 = a	B	TP26	Monitor Pin 23. Adjustment method noted separately.	0.1	—	2.9	V	
45	BPF MONI level 1.5 MHz	VBPML	SG22	15mVp-p	1.5MHz	SG29	200mVp-p	V26 = VBPAJ	22, 26, 29 = a	B	Pin 23		137	194	274	mVp-p	
46	BPF frequency response 0.8MHz/1.5MHz	FBPL08	SG22	15mVp-p	0.8MHz	SG29	200mVp-p	V26 = VBPAJ	22, 26, 29 = a	B	Pin 23	FBPL08/VBPML	—	-31	-28	dB	
47	BPF frequency response 1.4MHz/1.5MHz	FBPL14	SG22	15mVp-p	1.4MHz	SG29	200mVp-p	V26 = VBPAJ	22, 26, 29 = a	B	Pin 23	FBPL14/VBPML	-6	-3	—	dB	
48	BPF frequency response 1.6MHz/1.5MHz	FBPL16	SG22	15mVp-p	1.6MHz	SG29	200mVp-p	V26 = VBPAJ	22, 26, 29 = a	B	Pin 23	FBPL16/VBPML	-6	-3	—	dB	
49	BPF frequency response 1.7MHz/1.5MHz	FBPL17	SG22	15mVp-p	1.7MHz	SG29	200mVp-p	V26 = VBPAJ	22, 26, 29 = a	B	Pin 23	FBPL17/VBPML	—	-20	-12	dB	
50	BPF frequency response 2.5MHz/1.5MHz	FBPL25	SG22	15mVp-p	2.5MHz	SG29	200mVp-p	V26 = VBPAJ	22, 26, 29 = a	B	Pin 23	FBPL25/VBPML	—	-44	-28	dB	
51	BPF MONI level 1.7MHz	VBPMR	SG22	12mVp-p	1.7MHz	SG29	200mVp-p	V26 = VBPAJ	22, 23, 26, 29 = a	B	Pin 23		137	210	290	mVp-p	
52	BPF frequency response 1.5MHz/1.7MHz	FBPR15	SG22	12mVp-p	1.5MHz	SG29	200mVp-p	V26 = VBPAJ	22, 23, 26, 29 = a	B	Pin 23	FBPR15/VBPML	—	-28	-23	dB	
53	BPF frequency response 1.6MHz/1.7MHz	FBPR16	SG22	12mVp-p	1.6MHz	SG29	200mVp-p	V26 = VBPAJ	22, 23, 26, 29 = a	B	Pin 23	FBPR16/VBPML	—	-15	-10	dB	

No.	Item	Symbol	Measurement input signal conditions			Reference signal source			Control voltage	Switch condition	Mode condition	Measurement point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level	Frequency									
54	BPF frequency response 1.65MHz/1.7MHz	FBPR165	SG22	12mVpp	1.65MHz	SG29	200mVpp	3.579545MHz	V26 = VBPAJ V26 = VBPAJ	22, 23, 26, 29 = a	B	Pin 23	FBPR165/VBPMR	-6	-3	—	dB
55	BPF frequency response 1.75MHz/1.7MHz	FBPR175	SG22	12mVpp	1.75MHz	SG29	200mVpp	3.579545MHz	V26 = VBPAJ V26 = VBPAJ	22, 23, 26, 29 = a	B	Pin 23	FBPR175/VBPMR	-6	-3	—	dB
56	BPF frequency response 1.9MHz/1.7MHz	FBPL19	SG22	12mVpp	1.9MHz	SG29	200mVpp	3.579545MHz	V26 = VBPAJ V26 = VBPAJ	22, 23, 26, 29 = a	B	Pin 23	FBPR19/VBPMR	—	-29	-25	dB
57	DEV variable width 1.5M	VDEVL	SG62	-38dBm	400Hz	SG29	200mVpp	3.579545MHz	V26 = VBPAJ V36 = VAL	26, 29, 36, 62 = a	H	TP36	BIL REC mode. Monitor Pin 24. Adjustment method noted separately.	0.1	—	2.9	V
58	DEV variable width 1.7M	VDEVR	SG4	-38dBm	400Hz	SG29	200mVpp	3.579545MHz	V16 = VAL V26 = VBPAJ V36 = VDEVL	4, 16, 26, 29, 36 = a	H	TP16	BIL REC mode. Monitor Pin 24. Adjustment method noted separately.	0.1	—	2.9	V
59	AF LIM characteristics Lch	VAFMLL	SG62	-24Bm	10kHz	SG29	200mVpp	3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 36, 62 = a	H	Pin 24	BIL REC mode maximum deviation width	84	100	116	±kHz
60	AF LIM characteristics Rch	VAFMLR	SG4	-24Bm	10kHz	SG29	200mVpp	3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	4, 16, 26, 29, 36 = a	H	Pin 24	BIL REC mode maximum deviation width	42	50	58	±kHz
61	Reference FM modulation distortion factor Lch, Rch stereo	VRECHL VRECHR	SG62 SG4	-38dBm	1kHz	SG29	200mVpp	3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	4, 16, 26, 29, 36, 62 = a	A	TP-P49 TP-P52	Measure the output of Pin 24 after demodulation at standard demodulator.	—	0.2	0.4	%
62	Output level during OA Lch stereo	VSLPL	SG-R62	-38dBm	1kHz	SG31 SG29	0 to 3V 200mVpp	30Hz 3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 31, 36 = a 22 = c	B	Pin 49	Use standard modulator	-9.0	-7.0	-5.0	dBm
63	Output distortion factor during OA Lch stereo	THBLPL	SG-R62	-38dBm	1kHz	SG31 SG29	0 to 3V 200mVpp	30Hz 3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 31, 36 = a 22 = c	B	Pin 49	Use standard modulator to the 10th THD	—	0.3	0.55	%
64	Output level during OA Rch stereo	VSLPR	SG-R4	-38dBm	1kHz	SG31 SG29	0 to 3V 200mVpp	30Hz 3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 31, 36 = a 22 = c	B	Pin 52	Use standard modulator	-9.0	-7.0	-5.0	dBm
65	Output distortion factor during OA Rch stereo	THBLPR	SG-R4	-38dBm	1kHz	SG31 SG29	0 to 3V 200mVpp	30Hz 3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 31, 36 = a 22 = c	B	Pin 52	Use standard modulator to 10th THD	—	0.15	0.55	%

No.	Item	Symbol	Measurement input signal conditions			Reference signal source			Control voltage	Switch condition	Mode condition	Measurement point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level	Frequency									
66	Output level during OA R/L difference	BBRP	SG-R62	-38dBm	1kHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 31, 36 = a	B	VSLPR/VSLPL	-1.5	0.0	+1.5	dB	
			SG-R4			SG29	200mVpp	3.579545MHz									22 = c
67	Playback FM demodulation output noise Lch, Rch	VNLPL VNLPR	SG22	15mVpp	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 22, 26, 29, 31, 36 = a	J	A weight	-	-79	-74	dBm	
				12mVpp	1.7MHz	SG29	200mVpp	3.579545MHz									36 = a
68	Playback system MUTE switching output level difference	VPBCL VPBDCR	SG22	15mVpp	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 22, 26, 29, 31, 36 = a	B/F	DC level difference during MUTE ON/ OFF of playback line output	-100	-	+100	mVpp	
				12mVpp	1.7MHz	SG29	200mVpp	3.579545MHz									36 = a
69	Separation during OA L → R stereo	SSRPR	SG-R62	-38dBm	400Hz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 31, 36 = a	B	L → R separation SSRPR/VSLPL Use standard modulator	-	-30	-26.5	dB	
						SG29	200mVpp	3.579545MHz									22 = c
70	Separation during OA R → L stereo	SSRPL	SG-R4	-38dBm	400Hz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 26, 29, 31, 36 = a	B	R → L separation SSRPL/VSLPR Use standard modulator	-	-30	-26.5	dB	
						SG29	200mVpp	3.579545MHz									22 = c
71	DOC detection sensitivity ON level	VDOCSL	SG22	See Fig. 1	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL V44, V46 = 2.4V	16, 22, 26, 29, 31, 36, 44, 46 = a	B	Value of Fig. 1-a when 15mVpp is assumed 0dB	-15	-10	-7	dB	
						SG29	200mVpp	3.579545MHz									46 = a
72	DOC detection sensitivity OFF level hysteresis width	VDOHSL	SG22	See Fig. 1	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL V44, V46 = 2.4V	16, 22, 26, 29, 31, 36, 44, 46 = a	B	Ratio of Fig. 1-b/ Fig. 1-a VDOHSL/VDOCSL	-	-	1	dB	
						SG29	200mVpp	3.579545MHz									46 = a
73	ON level during DOC detection sensitivity LP	VDOCLL	SG22	See Fig. 1	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL V44, V46 = 2.4V	16, 22, 26, 29, 31, 36, 44, 46 = a	K	Value of Fig. 1-a when 15mVpp is assumed 0dB	-17	-12	-9	dB	
						SG29	200mVpp	3.579545MHz									46 = a
74	MUTE OFF DELAY T1	TMUON	SG22	See Fig. 2	Tone Burst	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 22, 26, 29, 31, 36 = a	J	Delay time from carrier lack to MUTE start T1 (during 680p)	1	1.36	1.7	ms	
						SG29	200mVpp	3.579545MHz									36 = a
75	MUTE hold time T2	TMUOF	SG22	See Fig. 2	Tone Burst	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 22, 26, 29, 31, 36 = a	J	MUTE hold time during MUTE cancel T2	113	1.33	153	ms	
						SG29	200mVpp	3.579545MHz									36 = a
76	PG doubler width Lch	TPGHL	See Fig. 3	15mVpp	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL V44, V46 = 2.4V	16, 22, 26, 29, 31, 36, 44, 46 = a	J	Measure the T2 time of Fig. 3	6	8.4	10	μs	
						SG29	200mVpp	3.579545MHz									46 = a

No.	Item	Symbol	Measurement input signal conditions			Reference signal source			Control voltage	Switch condition	Mode condition	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level	Frequency								
77	PG doubler width Rch	TPGHR	See Fig. 3	15mVp-p	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL V44, V46 = 2.4V	16, 22, 26, 29, 31, 36, 44, 46 = a	J	Measure T2 time of Fig. 3	10	12.2	14	$\mu$ s
			SG22	12mVp-p	1.7MHz	SG29	200mVp-p	3.579545MHz								
78	PG doubler delay Lch, Rch	TPGD	See Fig. 3	15mVp-p	1.5MHz	SG31	0 to 3V	30Hz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL V44, V46 = 2.4V	16, 22, 26, 29, 31, 36, 44, 46 = a	J	Measure T1 time of Fig. 3	2	2.6	3.2	$\mu$ s
			SG22	12mVp-p	1.7MHz	SG29	200mVp-p	3.579545MHz								
79	Monaural auto detection ON level	AMOON	See Fig. 4	15mVp-p	1.5MHz, fs = non, DEV = $\pm$ 60kHz	SG29	200mVp-p	3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 22, 26, 29, 31, 36 = a	J	Value of Fig. 4-a when 12mVp-p of 1.7M component is set to 0dB	-12	-9	-5.3	dB
			SG22	VAL	1.7MHz, fs = 1kHz, DEV = $\pm$ 30kHz											
80	Monaural auto detection OFF hysteresis width	AMOFF	See Fig. 4	15mVp-p	1.5MHz, fs = non, DEV = $\pm$ 60kHz	SG29	200mVp-p	3.579545MHz	V16 = VDEVR V26 = VBPAJ V36 = VDEVL	16, 22, 26, 29, 31, 36 = a	J	Value of Fig. 4-b when 12mVp-p of 1.7M component is set to 0dB	-	-	1	dB
			SG22	VAL	1.7MHz, fs = 1kHz, DEV = $\pm$ 30kHz											
81	CS, CK and SIN input low level	VSIL	58, 59, 60	VAL	DC							0	-	1	V	
82	CS, CK and SIN input high level	VSIH	58, 59, 60	VAL	DC							2	-	Vcc	V	
83	Serial/ parallel low level (parallel)	V17SL	17	VAL	DC							0	-	3.5	V	
84	Serial/ parallel high level (serial)	V17SH	17	VAL	DC							4.3	-	VccH	V	
85	SP/ LP low level (LP)	V17L	17	VAL	DC							0	-	1	V	
86	SP/ LP high level (SP)	V17H	17	VAL	DC							2	-	3.5	V	
87	NTSC/ PAL low level (PAL)	V28L	28	VAL	DC							0	-	1	V	
88	NTSC/ PAL high level (NTSC)	V28H	28	VAL	DC							2	-	Vcc	V	
89	Recording system MATRIX low level (MONO)	V32L	32	VAL	DC							0	-	0.7	V	



No.	Item	Symbol	Measurement input signal conditions			Reference signal source			Control voltage	Switch condition	Mode condition	Measurement point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level	Frequency									
90	Recording system MATRIX high level (STEREO)	V32H	32	VAL	DC				—	—	Pin 32	Parallel mode check stereo	2.3	—	V <sub>CC</sub>	V	
91	Playback system MATRIX low level (BIL/MONO auto)	V32PBL	32	VAL	DC				—	—	Pin 32	Parallel mode check BIL/monaural auto	0	—	0.7	V	
92	Playback system MATRIX middle level (ST/MONO auto)	V32PBM	32	VAL	DC				—	—	Pin 32	Parallel mode check stereo/monaural auto	1.3	—	1.7	V	
93	Playback system MATRIX high level (forced STEREO)	V32PBH	32	VAL	DC				—	—	Pin 32	Parallel mode check forced stereo	2.3	—	V <sub>CC</sub>	V	
94	E-E system output switching low level (L/R)	V33L	33	VAL	DC				—	—	Pin 33	Parallel mode check MAIN/SUB (L/R)	0	—	0.7	V	
95	E-E system output switching middle level (L/L)	V33M	33	VAL	DC				—	—	Pin 33	Parallel mode check MAIN/MAIN (L/L)	1.3	—	1.7	V	
96	E-E system output switching high level (R/R)	V33H	33	VAL	DC				—	—	Pin 33	Parallel mode check SUB/SUB (R/R)	2.3	—	3.5	V	
97	BPF through switching high level 2 (BPF OFF)	V33H2	33	VAL	DC				—	—	Pin 33	Parallel mode check BPF through (OFF)/POWER SAVE ON	4.3	—	V <sub>CC</sub> H	V	
98	MUTE ON/OFF low level (MUTE OFF)	V48L	48	VAL	DC				—	—	Pin 48	Parallel mode check MUTE OFF	0	—	1	V	
99	MUTE ON/OFF high level (MUTE ON)	V48H	48	VAL	DC				—	—	Pin 48	Parallel mode check MUTE ON	2	—	V <sub>CC</sub>	V	
100	MIC/LINE low level (LINE)	V58L	58	VAL	DC				—	—	Pin 58	Parallel mode check LINE	0	—	1	V	
101	MIC/LINE high level (MIC)	V58H	58	VAL	DC				—	—	Pin 58	Parallel mode check MIC	2	—	V <sub>CC</sub>	V	
102	PB/REC low level (REC)	V59L	59	VAL	DC				—	—	Pin 59	Parallel mode check REC	0	—	1	V	
103	PB/REC high level (PB)	V59H	59	VAL	DC				—	—	Pin 59	Parallel mode check PB	2	—	V <sub>CC</sub>	V	

No.	Item	Symbol	Measurement input signal conditions		Reference signal source			Control voltage	Switch condition	Mode condition	Measurement point	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency	Input pin	Level									
104	LINEOUT MIX ON/OFF low level (MIX OFF)	V60L	60	VAL	DC						Pin 60	Parallel mode check LINE Lch MIX OFF	0	—	1	V
105	LINEOUT MIX ON/OFF high level (MIX ON)	V60H	60	VAL	DC						Pin 60	Parallel mode check LINE Lch MIX ON	2	—	V <sub>CC</sub>	V

\* fsc recommended input level is normally 200mVp-p and the recommended input range is 100mVp-p to 1000mVp-p.

**Mode Condition Table**  
**Electrical Characteristics Measurement Circuit Mode Table**

Mode condition	BUS DECODER condition table during serial														Condition table during parallel									
	Value bit 0 to 4	bit 5	bit 6	bit 7	bit 8	bit 9	bit 10	bit 11	bit 12	bit 13	bit 14	bit 15	Value	V17	V20	V28	V32	V33	V48	V58	V59	V60		
	0	—	MAT RIX2	MAT RIX1	OUT SEL2	OUT SEL1	MIX	LINE MIC	LP SP	NTSC PAL	MUTE	REC PB	L H	LP SP	BIL —	PAL NTSC	MAT RIX	OUT SEL	MUTE	LINE MIC	REC PB	MIX		
A REC	0	0	1	1	0	0	0	1	1	1	0	0	0	H	OPEN	H	H	L	L	H	L	L	L	
B PB	0	0	1	1	0	0	0	1	1	1	0	1	H	OPEN	H	H	L	L	L	H	H	L	L	
C REC/LP	0	0	1	1	0	0	0	1	0	1	0	0	L	OPEN	H	H	L	L	L	H	L	L	L	
D REC/PAL	0	0	1	1	0	0	0	1	1	0	0	0	H	OPEN	L	H	L	L	L	H	L	L	L	
E REC/MUTE	0	0	1	1	0	0	0	1	1	1	1	0	H	OPEN	H	H	L	L	H	H	L	L	L	
F PB/MUTE	0	0	1	1	0	0	0	1	1	1	1	1	H	OPEN	H	H	L	L	H	H	H	L	L	
G REC/LINE	0	0	1	1	0	0	0	0	1	1	0	0	H	OPEN	H	H	L	L	L	L	L	L	L	
H REC/BIL	0	0	1	0	0	0	0	1	1	1	0	0	H	L	L	H	L	L	L	H	L	L	L	
I REC/BIL/LP	0	0	1	0	0	0	0	1	0	1	0	0	L	L	L	H	L	L	L	H	L	L	L	
J PB/BIL	0	0	0	0	0	0	0	1	1	1	0	1	H	OPEN	H	L	L	L	L	H	H	L	L	
K PB/LP	0	0	1	1	0	0	0	1	0	1	0	1	L	OPEN	H	H	L	L	L	H	H	L	L	
L																								
M																								
N																								
O																								

\* During serial control, set switches 58, 59 and 60 to "a", and V17 to 4.3V to Vcch.

During parallel control, set switches 58, 59 and 60 to "b", and set according to the mode table.

L: 0 to 1V

M: 1.3 to 1.7V

H: 2 to 3.5V

H2: 4.3V to Vcch

Mode Control Tables

1. Parallel CTL mode table

Pin No.	Symbol		Control voltage					Remarks
			LOW (0 to 1V)	OPEN	HIGH1 (2V to V <sub>CC</sub> )	HIGH2 (2V to 3.5V)	HIGH3 (4.3V to V <sub>CC</sub> H)	
17	SP/LP		LP	SP	—	SP	Serial mode *1	
20	REC BIL CTL	REC	BIL REC (during Pin 32 low)	—	—	—	—	CTL IN during REC
	PB MONODET OUT	PB	STEREO/BIL	MONO	—	—	—	DET OUT during PB
28	NTSC/PAL		PAL	—	NTSC	—	—	
32	MATRIX CTL		REC	Forced MONO	STEREO	STEREO	—	—
			PB	Bilingual/MONO auto detection	STEREO/MONO auto detection	Forced STEREO	—	—
33	OUTSEL CTL		Lch/Rch	Lch/Lch	—	Rch/Rch	—	
	POWER SAVE		OFF	OFF	—	OFF	ON	
	BPF ON/OFF		ON	ON	—	ON	OFF (only 1.5M BPF is through)	
48	MUTE		MUTE OFF	MUTE ON	MUTE ON	—	—	
58	MIC/LINE		LINE	LINE	MIC	—	—	
59	REC/PB		REC	REC	PB	—	—	
60	RFU (MIX)		OFF	OFF	ON	—	—	

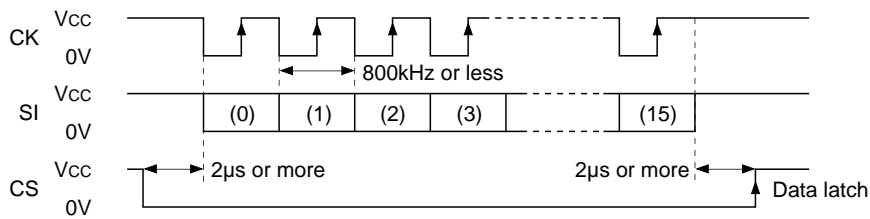
\*1 When Pin 17 is 4.3V or more, the IC operates in serial control mode.

2. Serial control

\* When Pin 17 is 4.3V or more, the IC operates in serial control mode.

1) Input condition

Item	Symbol	Min.	Typ.	Max.	Unit	Pin No.	Symbol	CTL voltage		
								LOW (0 to 1V)	OPEN	HIGH (2V to Vcc)
Clock frequency	fck			800	kHz					
Setup time	t <sub>su</sub>	400			ns					
Hold time	t <sub>HLD</sub>	400			ns	58	CS	L	L	H
CS rise time to SI start time	t <sub>1</sub>	2			μs	59	CK	L	L	H
Final CS rise time to CS fall time	t <sub>2</sub>	2			μs	60	SIN	L	L	H



2) Serial CTL mode table

Bit No.	Control name	CTL value	Mode
0	—	L	—
1	—	L	—
2	—	L	—
3	—	L	—
4	—	L	—
5	POWER SAVE	L H	OFF ON
6	MATRIX2	See Table 1	See Table 1
7	MATRIX1		
8	OUTSEL2	See Table 2	See Table 2
9	OUTSEL1		
10	LINEOUT MIX	L H	OFF ON
11	LINE/MIC switching	L H	LINE MIC
12	LP/SP switching	L H	LP SP
13	PAL/NTSC switching	L H	PAL NTSC
14	MUTE	L H	OFF ON
15	REC/PB switching	L H	REC PB

Table 1

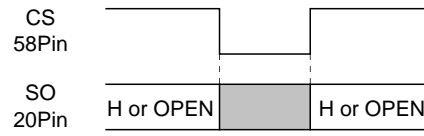
OUTSEL1 (bit 9)	OUTSEL2 (bit 8)	
H	H	Rch/Rch
L	H	Lch/Lch
—	L	Lch/Rch

Table 2

MATRIX1 (bit 7)	MATRIX2 (bit 6)	during REC	during PB
H	L	MATRIX ON	MATRIX ON
H	H	MATRIX ON	MATRIX (AUTO)
L	H	BIL REC	MATRIX (AUTO)
L	L	REC MONO	MATRIX OFF BIL/MONO (AUTO)

3) SO control mode table

Mode (only the shaded period as shown in the figure right)		Pin 20 (SO)
REC	During Pin 32 = L	OPEN
	During Pin 32 = H	L
PB	$\overline{\text{MONO}}$	L
	MONO	OPEN



The result of detection is output during CS period.  
H or OPEN other than CS period.

I/O Waveform

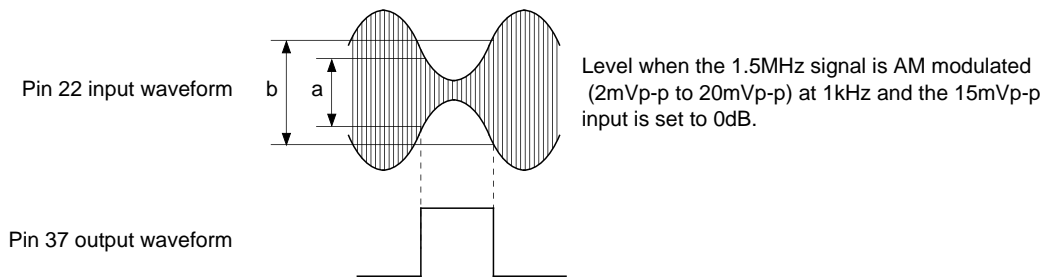


Fig. 1

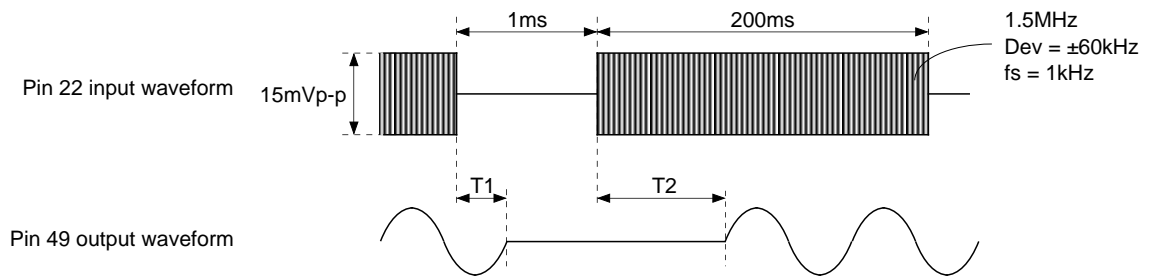


Fig. 2

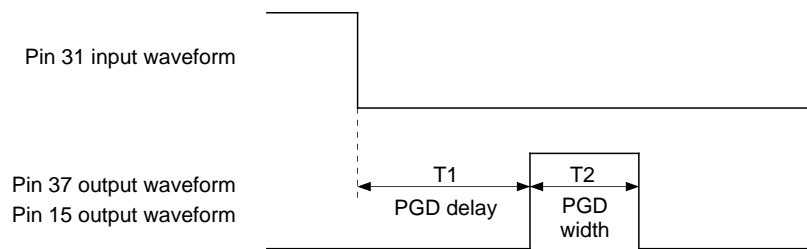


Fig. 3

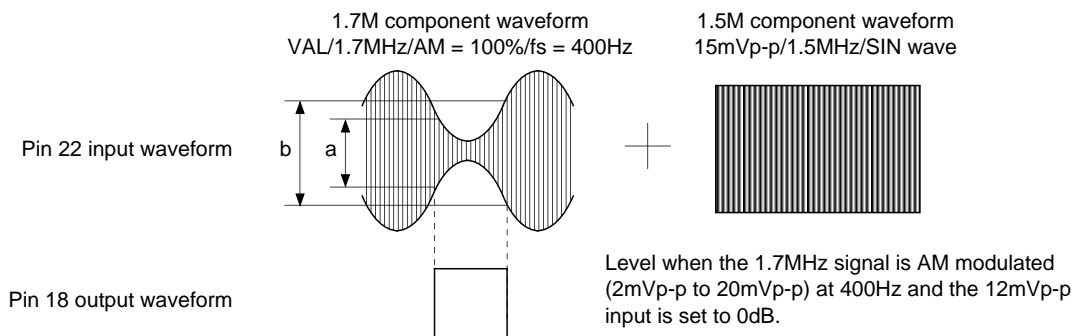


Fig. 4

## Adjustment and Measurement Methods

### DEV adjustment method

- Lch adjustment

Input the reference input ( $-38\text{dBm}/400\text{Hz}$ ) to the MIC input (Pin 62) and adjust the voltage applied to Pin 36 (V36) so that the Pin 24 output reference frequency deflection is  $1.5\text{MHz} \pm 60\text{kHz}$ .

When adjusting DEV, connect a  $10\text{k}\Omega$  load resistor between Pin 24 and GND as shown in the electrical characteristics measurement circuit.

- Rch adjustment

Input the reference input ( $-38\text{dBm}/400\text{Hz}$ ) to the MIC input (Pin 4) and adjust the voltage applied to Pin 16 (V16) so that the Pin 24 output reference frequency deflection is  $1.7\text{MHz} \pm 30\text{kHz}$ .

When adjusting DEV, connect a  $10\text{k}\Omega$  load resistor between Pin 24 and GND as shown in the electrical characteristics measurement circuit.

### Reference FM modulation distortion factor measuring method

Demodulate the Pin 24 output into the audio signal with the reference demodulator under the same conditions as for DEV adjustment above, then measure the distortion factor.

### BPF adjustment method

Input  $15\text{mVp-p}$ ,  $1.625\text{MHz}$  signal to Pin 22 and adjust the voltage applied to Pin 26 (V26) so that the output level when the SW of Pin 23 is switched to "a" ( $1.7\text{M}$  BPF output) and the output level when the SW of Pin 23 is switched to "b" ( $1.5\text{M}$  BPF output) are equal.

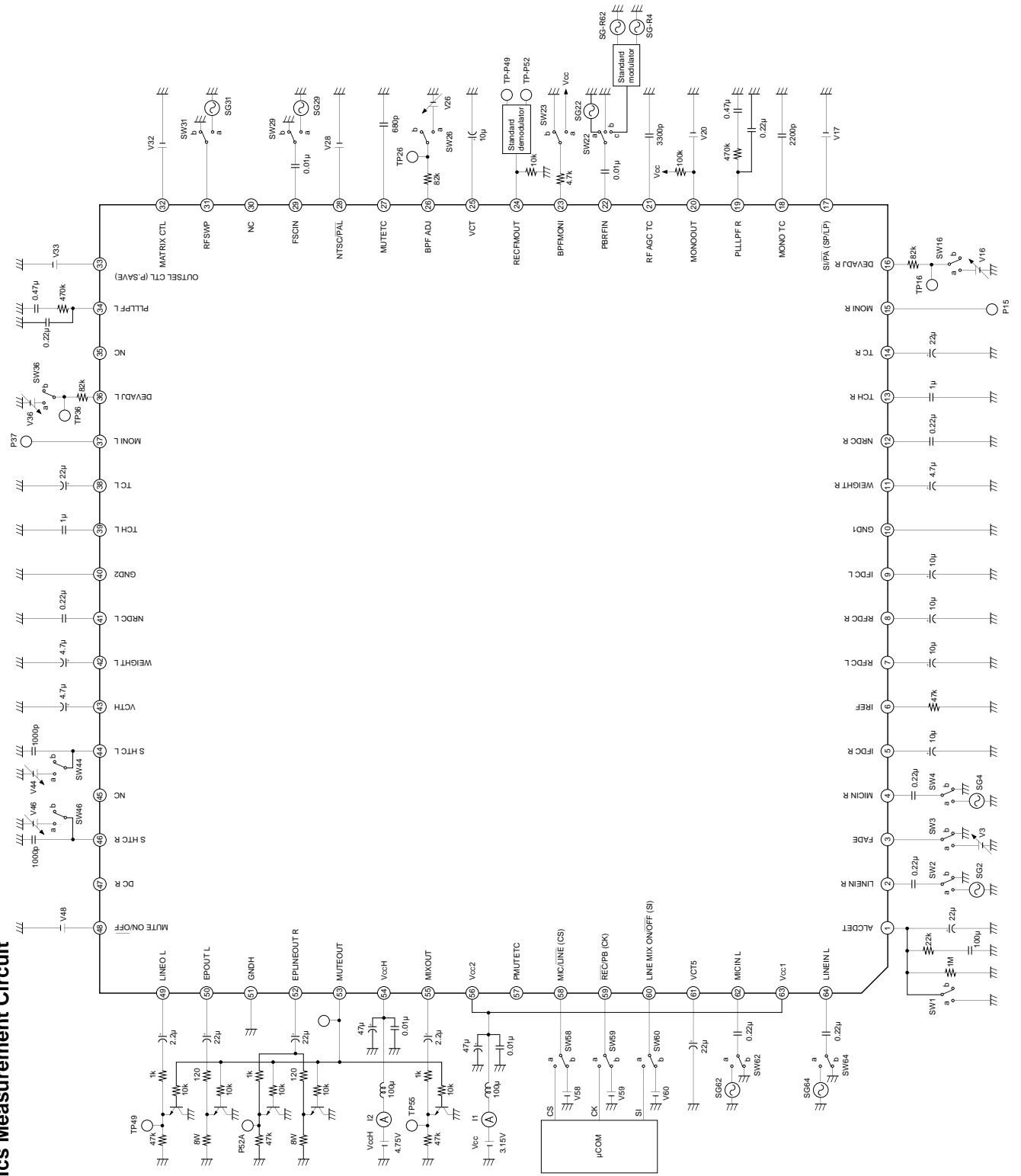
When adjusting BPF, connect a  $4.7\text{k}\Omega$  load resistor between Pin 23 and GND as shown in the electrical characteristics measurement circuit.

### Fader adjustment method

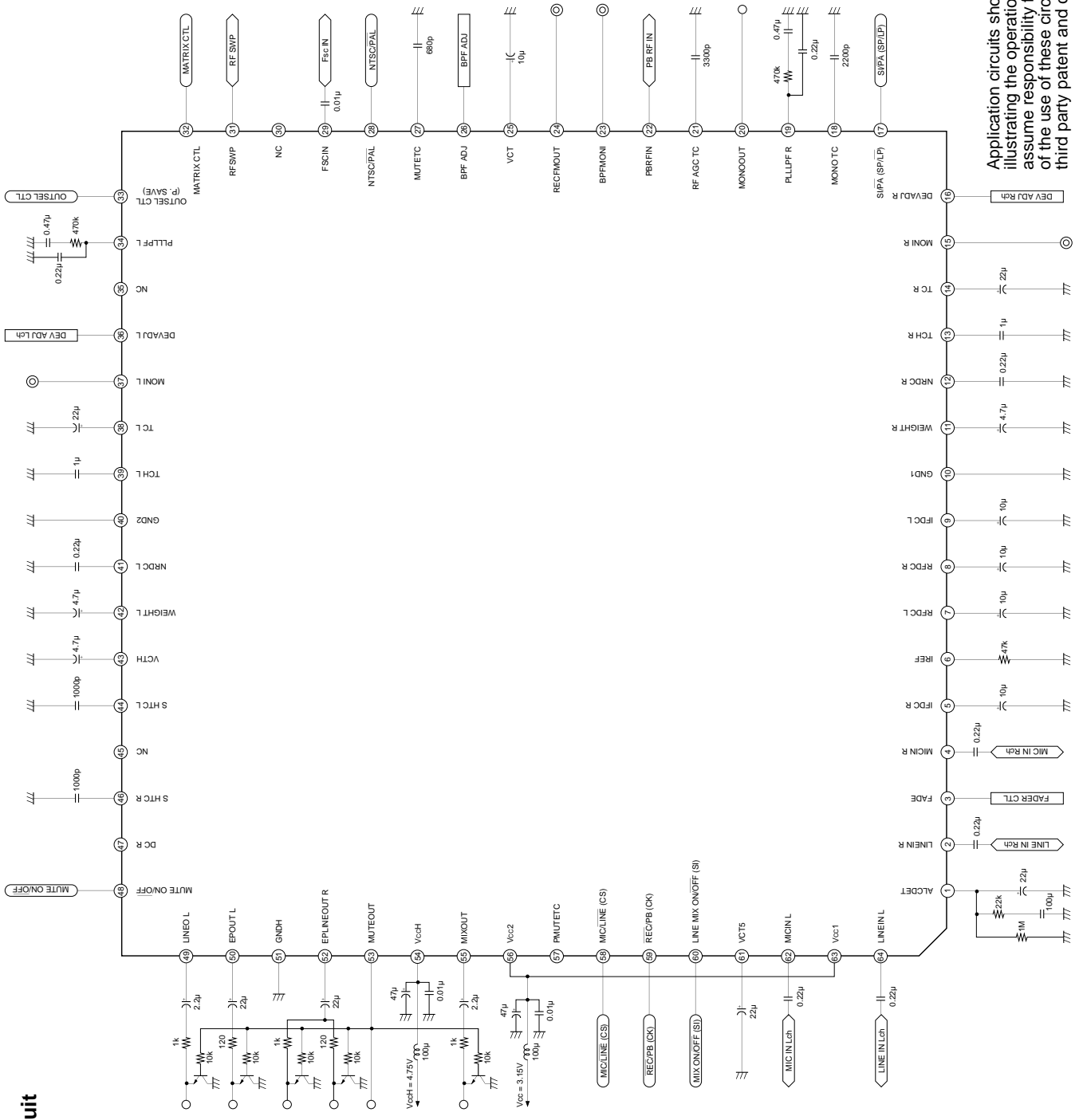
Input the reference input ( $-38\text{dBm}/400\text{Hz}$ ) to the MIC input (Pins 62 and 4) and adjust the output level of Pins 49 and 52 with the voltage applied to Pin 3 (V3).



Electrical Characteristics Measurement Circuit

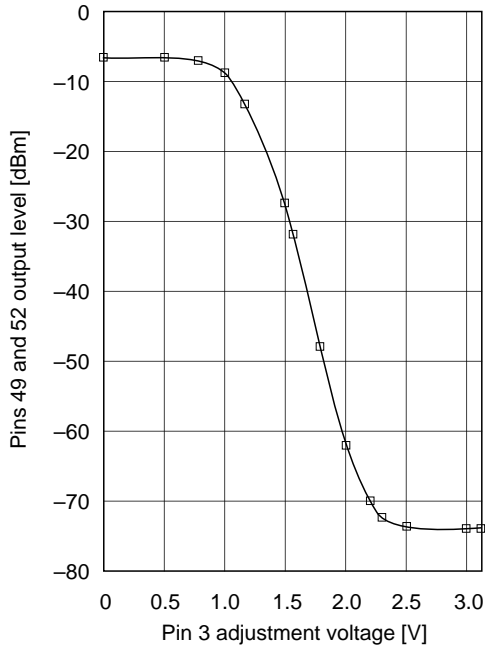


Application Circuit

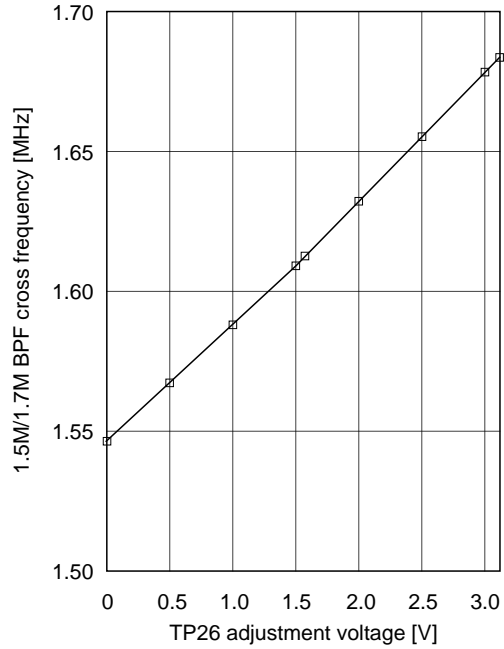


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

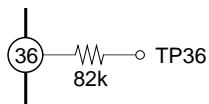
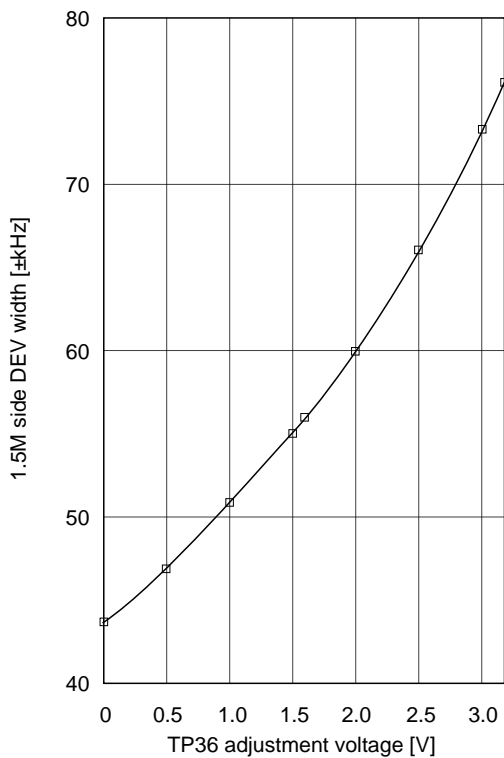
Graph 1. FADER control characteristics



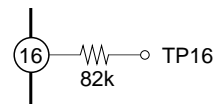
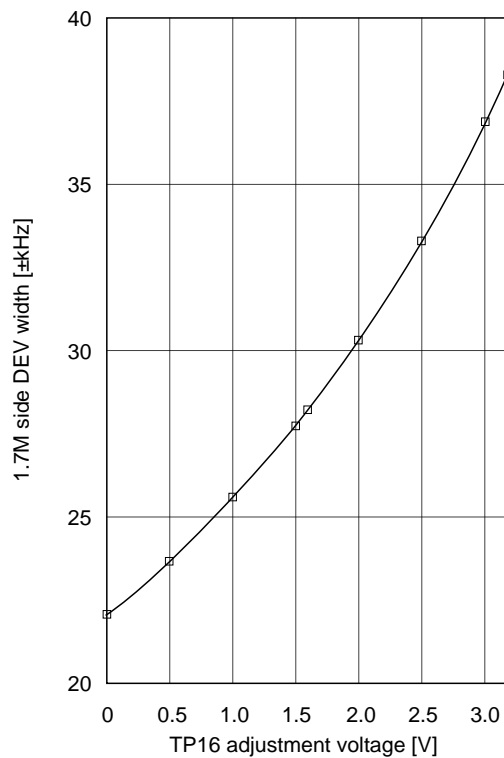
Graph 2. BPF ADJ control characteristics



Graph 3. DEV ADJ control characteristics Lch

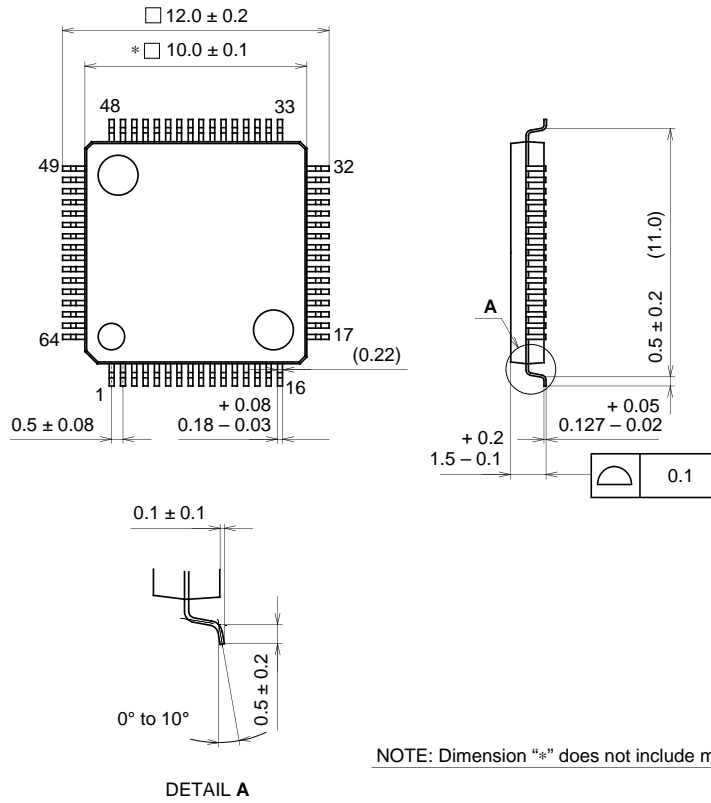


Graph 4. DEV ADJ control characteristics Rch



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g