查询CXA1792供应商 捷多邦，专业PCB打样工厂，24小时加急出货

SONY

CXA1792S

2-Channel, 5-Element Graphic Equalizer IC

Description

The CXA1792S is a bipolar IC designed for graphic equalizer. All functions are DC-controlled so that a 2-channel graphic equalizer can be easily constructed with a set of volumes externally added.

Features

- Microcomputer controllable
- Electric volume
- Balance function
- Supports 2-channel and 5-band
- 2-channel FIX OUT and LINE OUT pins provided

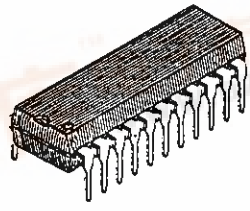
Absolute Maximum Ratings (Ta=25℃)

• Supply voltage	Vcc	12	V
• Storage temperature	Tstg	–65 to +150	℃
• Allowable power dissipation	PD	1200	mW

Operating Conditions

• Supply voltage	Vcc	4.0 to 10.0	V
	DVcc	3.5 to Vcc	V
• Ambient temperature	Topr	–20 to +75	℃

22 pin SDIP (Plastic)



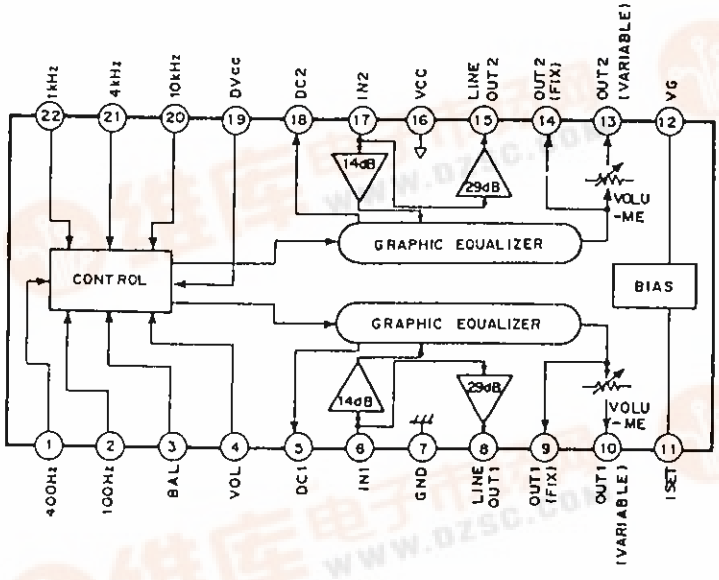
Structure

Bipolar silicon monolithic IC

Applications

Graphic equalizer used for applications such as cassette tape recorder with radio, car stereo and portable stereo.

Block Diagram and Pin Configuration

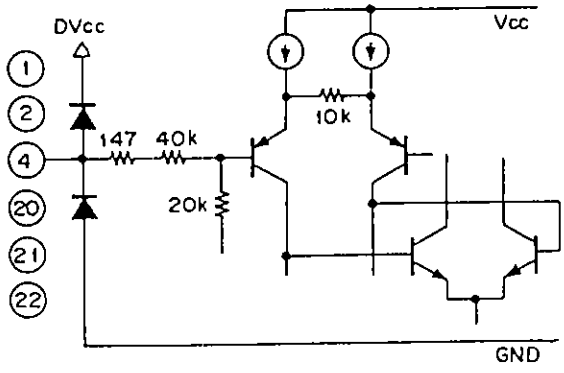
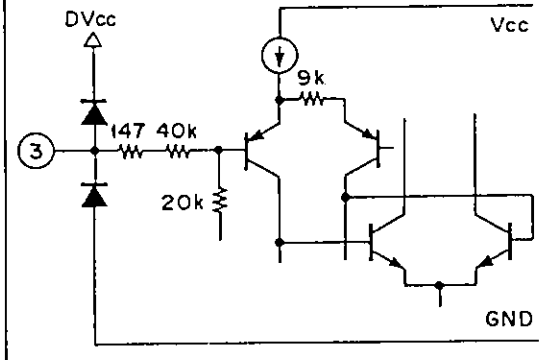
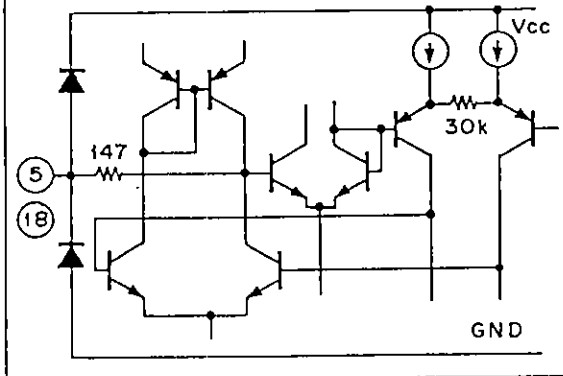
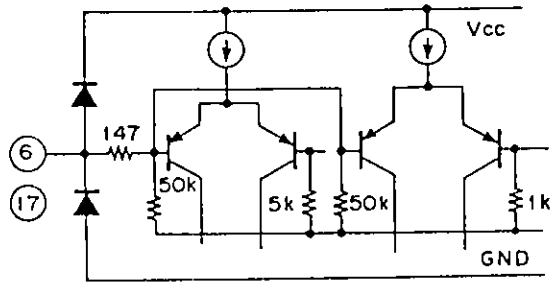
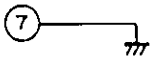


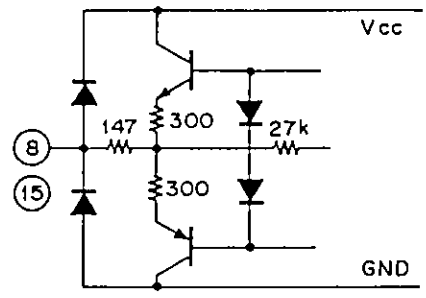
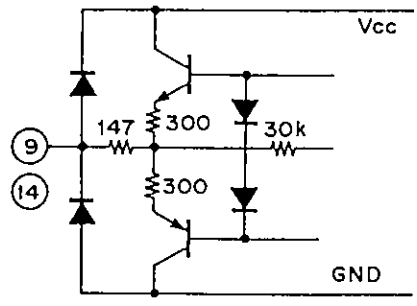
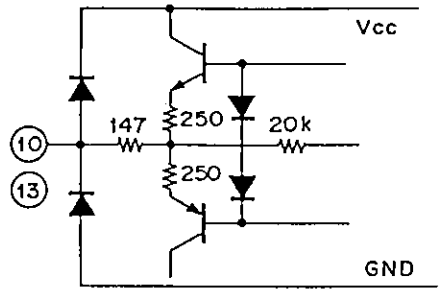
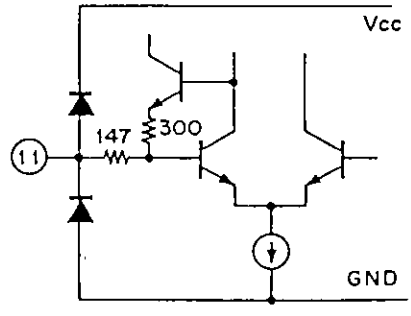
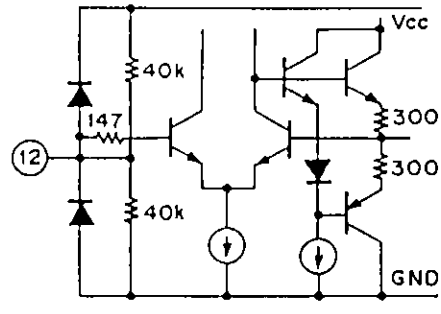
Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

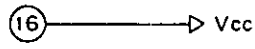
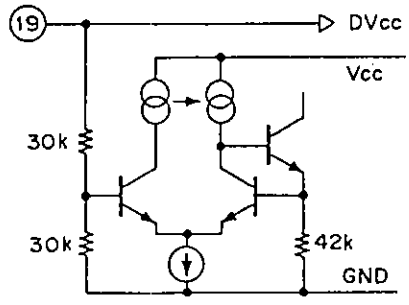
E93305 – ST

找PDF 维库一下 pdf.dzsc.com

Pin Description

Pin No.	Symbol	Pin voltage	I/O resistance	Equivalent circuit	Description
1 2 20 21 22	400Hz 100Hz 10kHz 4kHz 1kHz	$\frac{DVcc}{2}$	60kΩ		Graphic equalizer control. DC input.
4	VOL				Volume control. DC input.
3	BAL	$\frac{DVcc}{2}$	60kΩ		Balance control. DC input.
5 18	DC1 DC2	$\frac{Vcc}{2}$	—		Connects the DC feedback capacitor of LPF used for the 100Hz graphic equalizer.
6 17	IN1 IN2	$\frac{Vcc}{2}$	25kΩ		Signal input.
7	GND	GND			GND

Pin No.	Symbol	Pin voltage	I/O resistance	Equivalent circuit	Description
8 15	L OUT1 L OUT2	$\frac{Vcc}{2}$	0		Line output.
9 14	F OUT1 F OUT2	$\frac{Vcc}{2}$	0		FIX output.
10 13	OUT1 OUT2	$\frac{Vcc}{2}$	0		Electric volume output.
11	ISET	1.3V	0		Reference current setting. (for graphic equalizer) Normally connect a 160kΩ resistor.
12	VG	$\frac{Vcc}{2}$	20kΩ		Signal reference voltage. Connect a capacitor for ripple elimination.

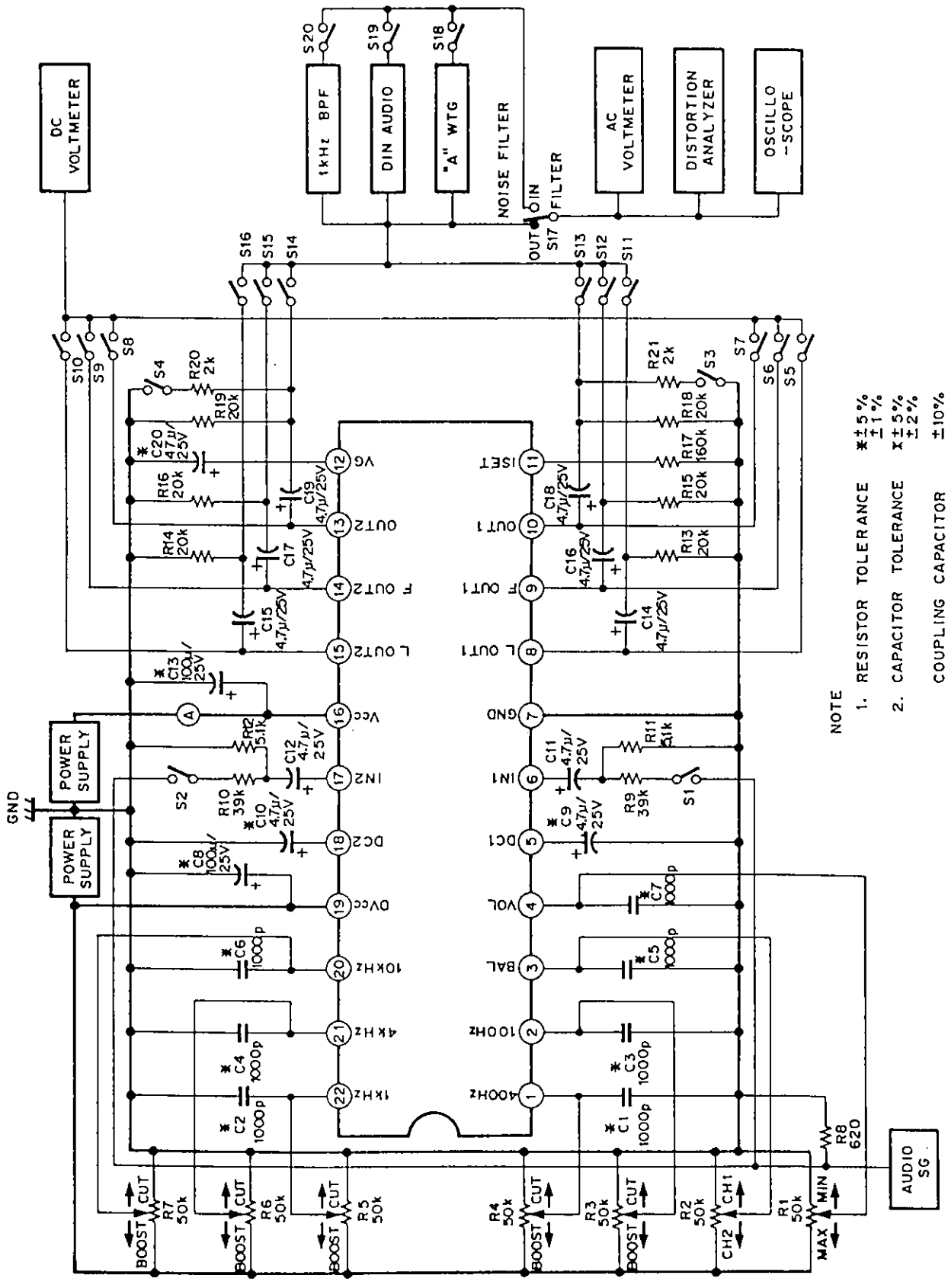
Pin No.	Symbol	Pin voltage	I/O resistance	Equivalent circuit	Description
16	Vcc	Vcc			Operating supply voltage.
19	DVcc	DVcc	60kΩ		Control supply voltage.

Electrical Characteristics

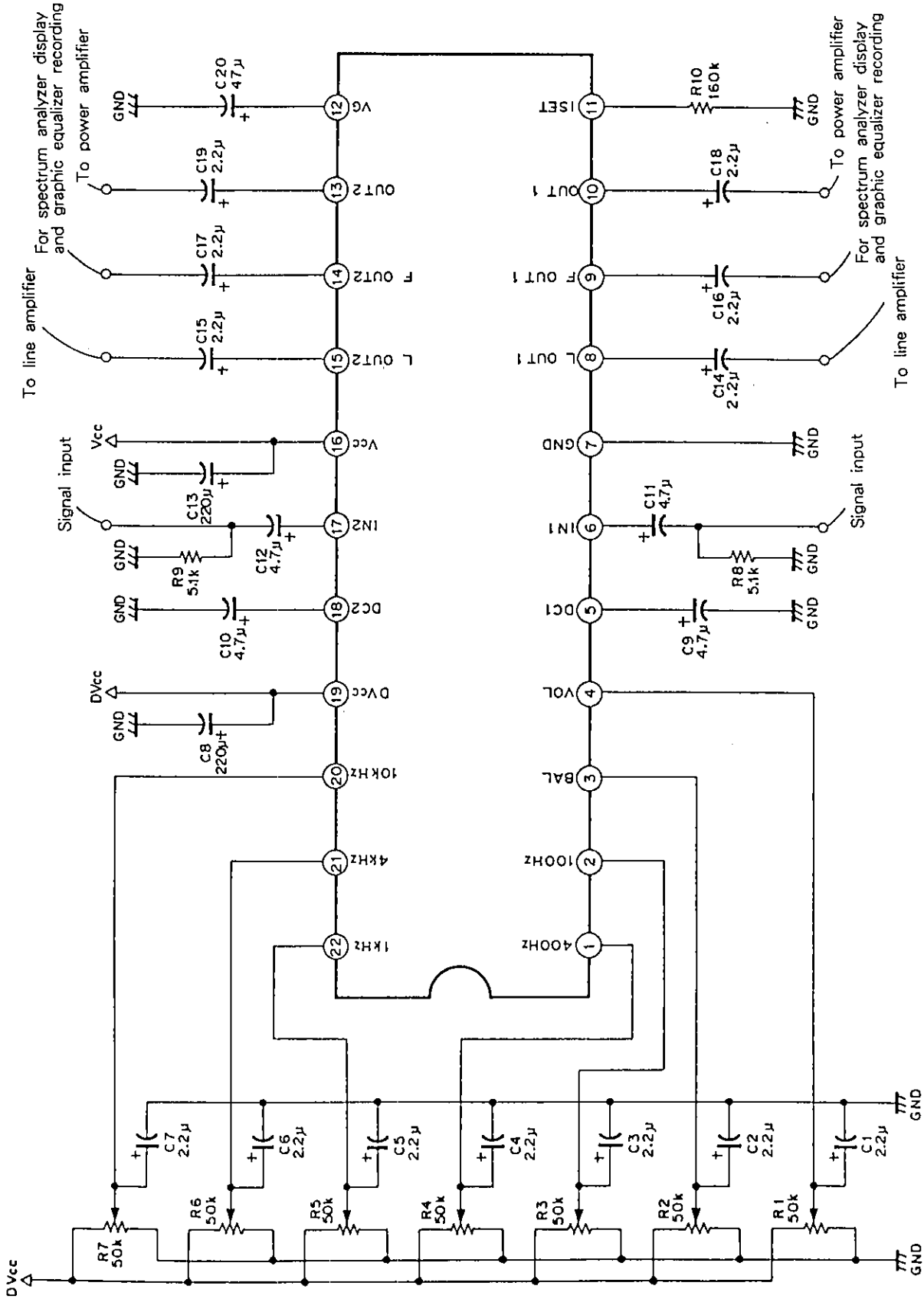
(Ta=25℃, Vcc=8V, DVcc=5V)

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
1	Operating supply voltage	Vcc		4.0	—	10.0	V
2	Control supply voltage	DVcc		3.5	—	Vcc	V
3	Current consumption	Icc	All flat graphic equalizer, medium volume	8.0	12.0	16.0	mA
4	Reference input level	V_{IN}		—	–34.0	—	dBm
5	Reference output level	V_{OUT}	All flat graphic equalizer, maximum volume, f=1kHz	–23.0	–20.0	–17.0	dBm
6	Reference LINE output level	V_{LINE}	f=1kHz	–6.5	–4.5	–2.5	dBm
7	Reference FIX output level	V_{FIX}	All flat graphic equalizer, f=1kHz	–23.0	–20.0	–17.0	dBm
8	Graphic equalizer setting frequency (1)	GEQ1	LPF cut-off frequency (–3dB)	—	200	—	Hz
9	Graphic equalizer setting frequency (2)	GEQ2	BPF (1) center frequency	—	400	—	Hz
10	Graphic equalizer setting frequency (3)	GEQ3	BPF (2) center frequency	—	1.0	—	kHz
11	Graphic equalizer setting frequency (4)	GEQ4	BPF (3) center frequency	—	4.0	—	kHz
12	Graphic equalizer setting frequency (5)	GEQ5	HPF cut-off frequency (–3dB)	—	8.0	—	kHz
13	Graphic equalizer frequency deviation	ΔEQ	Deviation of cut-off and center frequencies	–20	0	20	%
14	Maximum boost level (1)	GEQB1	f=400Hz, 1kHz and 4kHz maximum boost level	9.0	11.2	14.0	dB
15	Maximum boost level (2)	GEQB2	f=100Hz and 10kHz maximum boost level	8.0	10.7	14.0	dB
16	Maximum cut level (1)	GEQC1	f=400Hz, 1kHz and 4kHz maximum cut level	–13.0	–10.7	–8.5	dB
17	Maximum cut level (2)	GEQC2	f=100Hz, 10kHz maximum cut level	–12.0	–9.5	–7.0	dB
18	Total harmonic distortion	THD	R_L=2kΩ, all flat graphic equalizer, maximum volume, f=1kHz, reference 10dB input	—	0.25	1.0	%
19	Volume attenuation (1)	VOL1	All flat graphic equalizer, maximum volume, f=1kHz	–1.5	0	1.5	dB
20	Volume attenuation (2)	VOL2	All flat graphic equalizer, minimum volume, f=1kHz	—	–94.4	–80.0	dB
21	Noise level	V_{NOIS}	Rg=5kΩ, all flat graphic equalizer, maximum volume, "A" WTG filter	—	–93.1	–88.0	dBm
22	Output offset voltage	V_{OFF}	All flat graphic equalizer, maximum volume	3.5	4.0	4.5	V

Electrical Characteristics Test Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Graphic Equalizer

- Conventional method

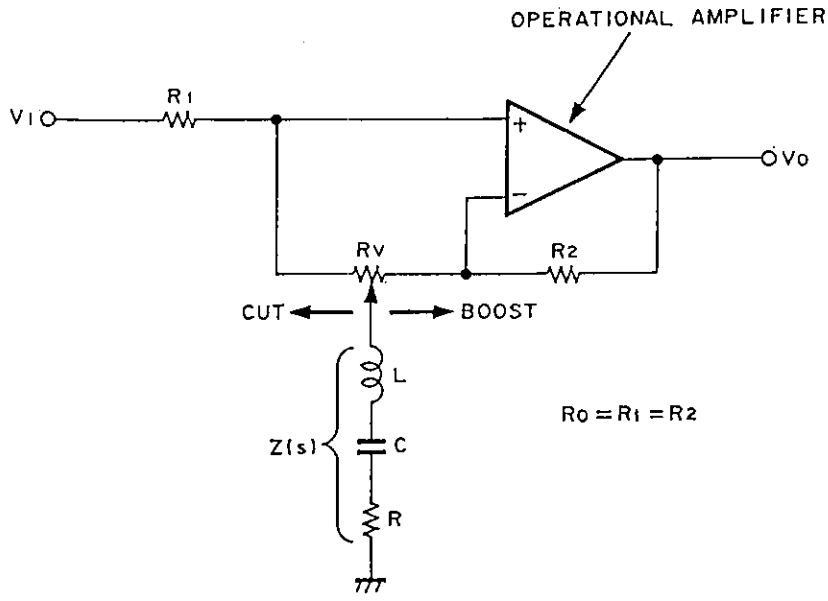


Fig. 1

Fig. 1 shows the structure of the conventional graphic equalizer. This circuit boosts or cuts frequencies around resonance frequency fo which is produced from the LCR circuit and potentiometer Rv. This operation is as follows. Frequencies around fo is cut most when the LCR circuit is moved to the most left end of Rv. When the transmittance is set to T (s),

$$T(s)=\frac{Z(s)}{Z(s)+Ro}$$

Using $Z(s)=sL+R+\frac{1}{sC}$

$$T(s)=(S)=\frac{LCs^2+RCs+1}{LCs^2+(R+Ro)Cs+1}$$

If $fo=\frac{\omega o}{2\pi}$, $\omega o=\frac{1}{LC}$ and $Q=\frac{\omega oL}{R}$, the frequency characteristics for cut can be obtained.

While frequencies around fo is boosted most when the LCR circuit is moved to the most right end.
The transmittance in this condition is

$$T(s)=\frac{Z(s)+Ro}{Z(s)}=\frac{LCs^2+(R+Ro)Cs+1}{LCs^2+RCs+1}$$

If fo, ωo and Q are defined as for cut, the frequency characteristics for boost can be obtained.

Fig. 2 shows frequency characteristics for both boost and cut conditions.

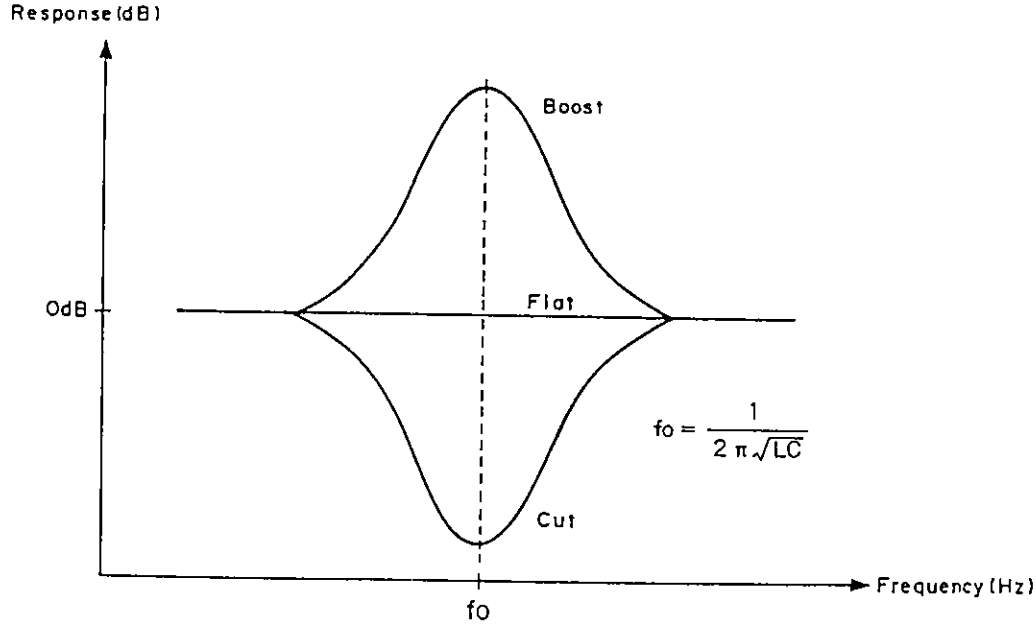


Fig. 2

- The CXA1792S method

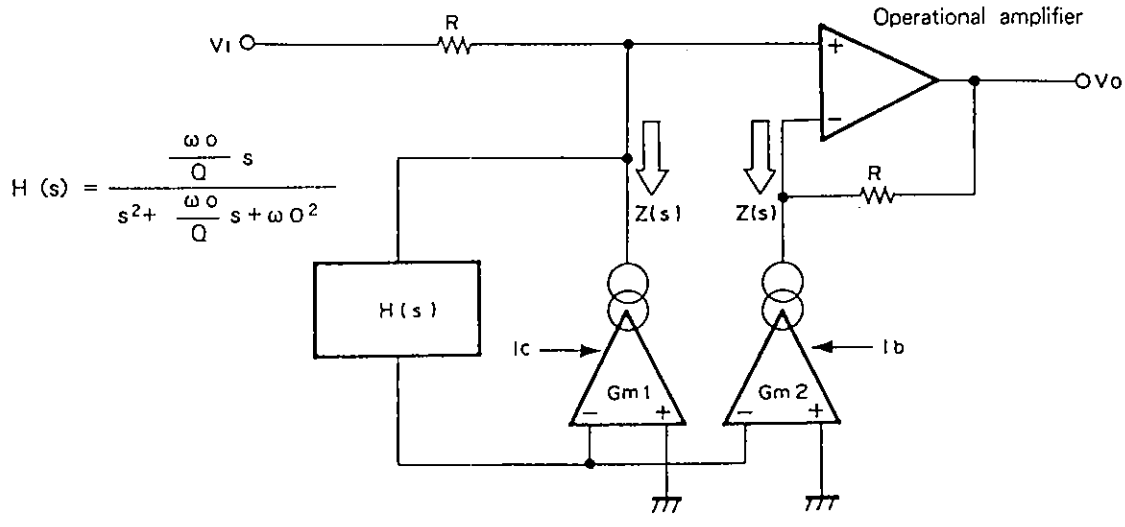


Fig. 3

Fig. 3 shows the structure of the graphic equalizer circuit used in the CXA1792S. The circuit boosts or cuts frequencies around center frequency ωo, using ωo of band-pass filter (BPF) and two transconductance amplifiers whose conversion factor can be changed by the control currents Ib and Ic. Output impedance Z (s) of Gm1 and Gm2 are

$$Z(s) = \frac{1}{H(s) \cdot Gm1}$$

Using ωo and Q, transmittance H (s) of the BPF is described as follows:

$$H(s)=\frac{\frac{\omega o}{Q}s}{s^2+\frac{\omega o}{Q}s+\omega^2}$$

Then, the following equation is obtained:

$$Z(s)=\frac{Q}{\omega o \cdot Gm1}s+\frac{1}{Gm1}+\frac{\omega o \cdot Q}{Gm1 \cdot s}$$

This equation shows that the Z (s) has impedance characteristics equivalent to that of the LCR circuit.
Assuming the maximum values of Gm1 and Gm2 equal Gm, the operation of this circuit is described below.
When Gm1=Gm and Gm2=0, frequencies around ωo is cut most and its transmittance T (s) is

$$T(s)=\frac{Z(s)}{Z(s)+R}=\frac{s^2+\frac{\omega o}{Q}\cdot s+\omega o^2}{s^2+\frac{(1+R\cdot Gm)\cdot \omega o^2}{Q}\cdot s+\omega o^2}$$

The frequency characteristics for cut is equivalent to that of the conventional graphic equalizer.
When Gm1=0 and Gm2=Gm, frequencies around ωo is boosted most and its transmittance is

$$T(s)=\frac{Z(s)+R}{Z(s)}=\frac{s^2+\frac{(1+R\cdot Gm)\cdot \omega o^2}{Q}\cdot s+\omega o^2}{s^2+\frac{\omega o}{Q}\cdot s+\omega o^2}$$

The frequency characteristics for boost is equivalent to that of the conventional graphic equalizer.
From this, the two methods are different, but the operation of the graphic equalizer contained in the CXA1792S is equivalent to that of the conventional one. This IC has an advantage of realizing a graphic equalizer without external parts by monolithic filter technology.
The actual structure of graphic equalizer including BPF is shown in Fig. 4

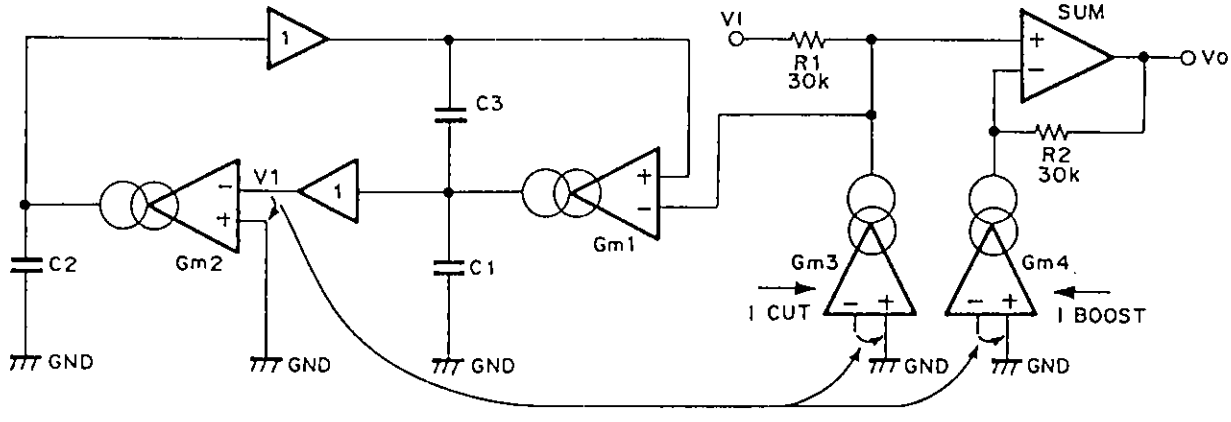


Fig. 4

2. Microcomputer Controllable

All controls for volume, balance, and boosting and cutting at 100Hz, 400Hz, 1kHz, 4kHz and 10kHz frequencies are executed though DC voltage.
DC voltage range is from 0V to DVcc, determined by the control power supply DVcc independently of Vcc. Then, the control range can be freely varied by changing the DVcc voltage. If DVcc=5V, this IC is controllable with microcomputer.
If DVcc=Vcc, this IC can be used with a single power supply.

Notes on Operation

1. Power supply

DVcc can be used independent of Vcc, but must satisfy the following relationship.

Vcc ≧ DVcc

2. Output pins

This IC provides two channels each for OUT, LINE OUT and FIX OUT pins. These output pins are used as follows:

- OUT pin
  Used for the normal graphic equalizer output.
- LINE OUT pin
  A source signal is amplified and immediately out from this pin without going through the graphic equalizer.
- FIX OUT pin
  Suitable for recording a signal processed by the graphic equalizer or spectrum analyzer display.

Fig. 5 shows the relationship between the input and each output.

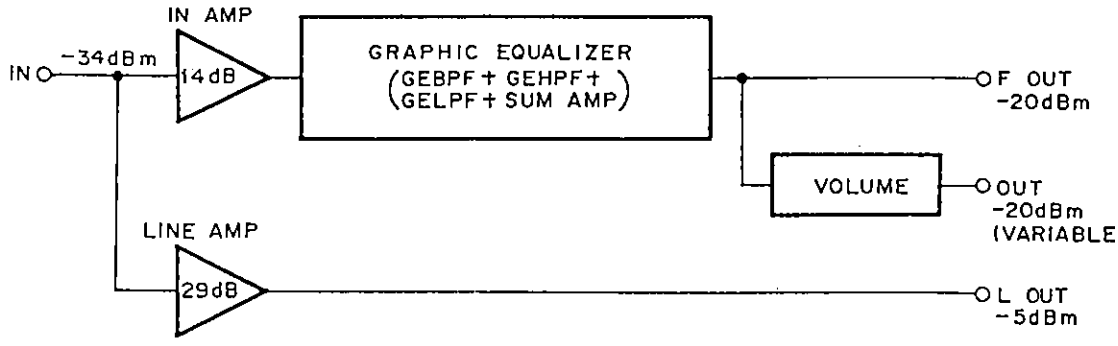


Fig. 5

3. Reference resistor

In order to minimize the deviation of the center frequency in the graphic equalizer, the CXA1792S uses an external resistor in place of an internal resistor to determine control current which determines time constant of the filter.

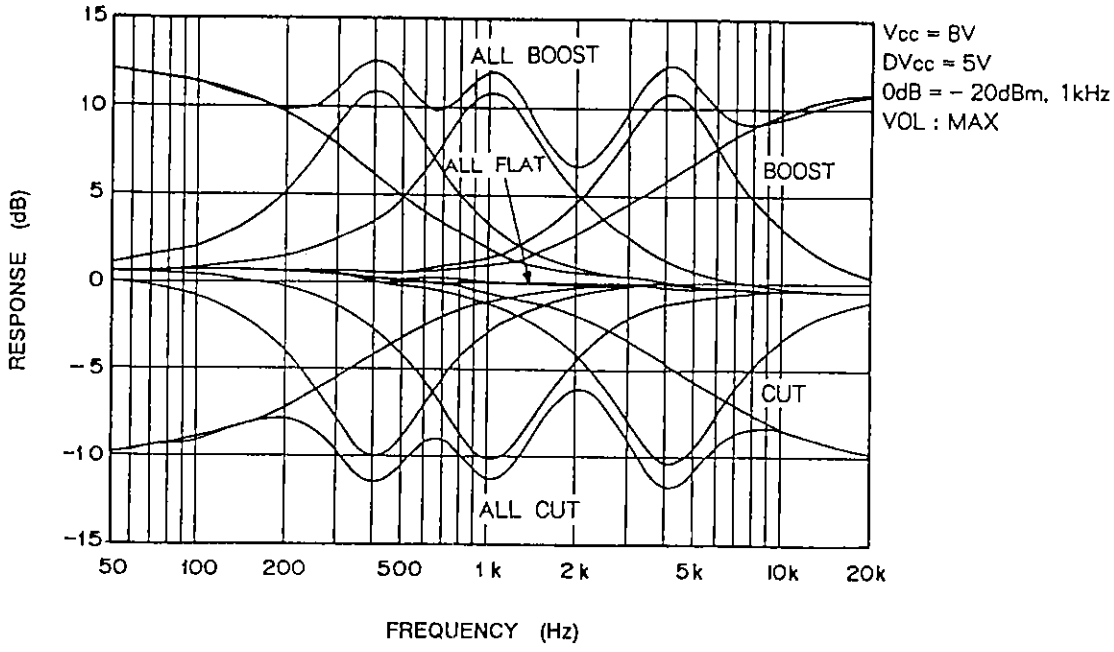
This is a 160kΩ resistor connected to ISET pin (Pin 11). Therefore, this resistor, having smaller tolerance and better temperature characteristics, is recommended.

Using the external resistor of different resistance can shift the frequency characteristics of the graphic equalizer. Using that of smaller resistance shifts the characteristics toward the higher frequency side, and using that of larger resistance shifts it toward the lower frequency side.

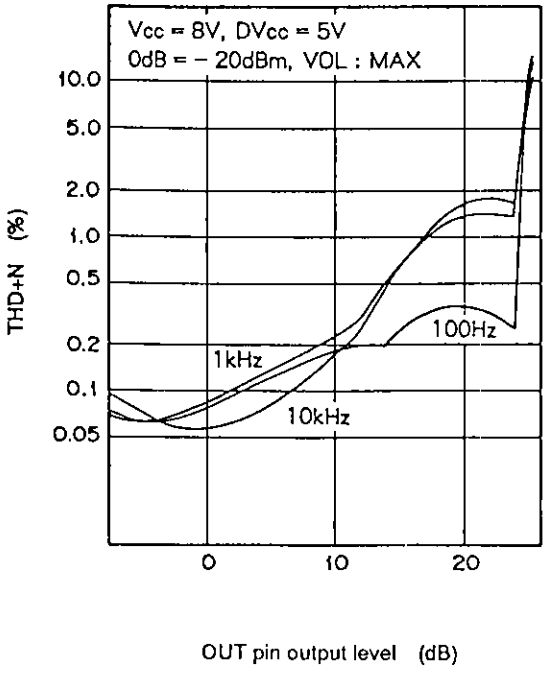
In this operation, the 5 elements can not be shifted independently.

Example of Representative Characteristics

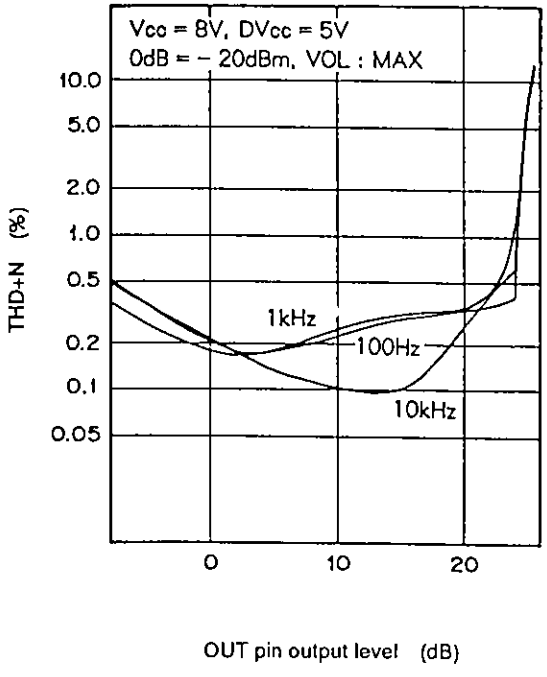
Frequency characteristics



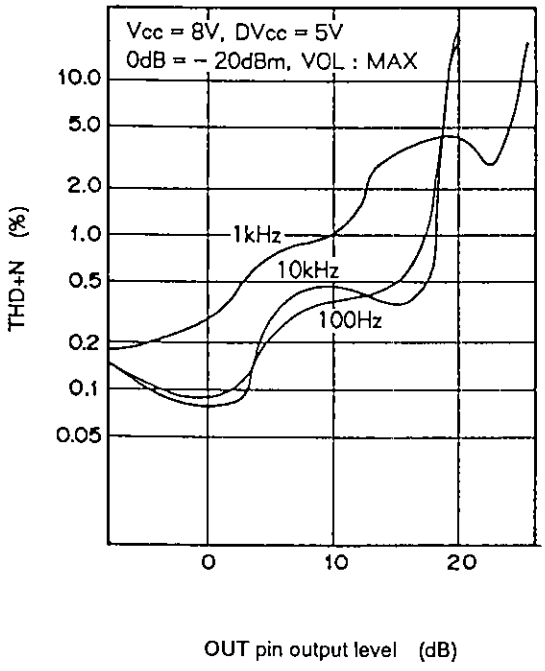
THD vs. OUT characteristics (ALL FLAT)



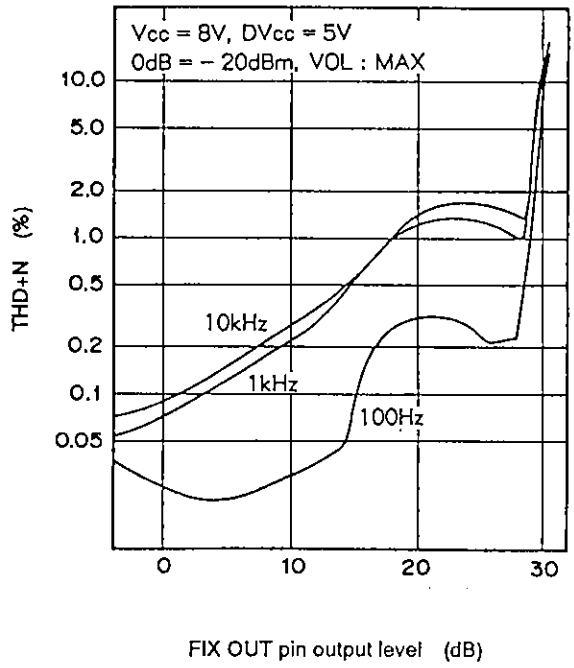
THD vs. OUT characteristics (ALL BOOST)



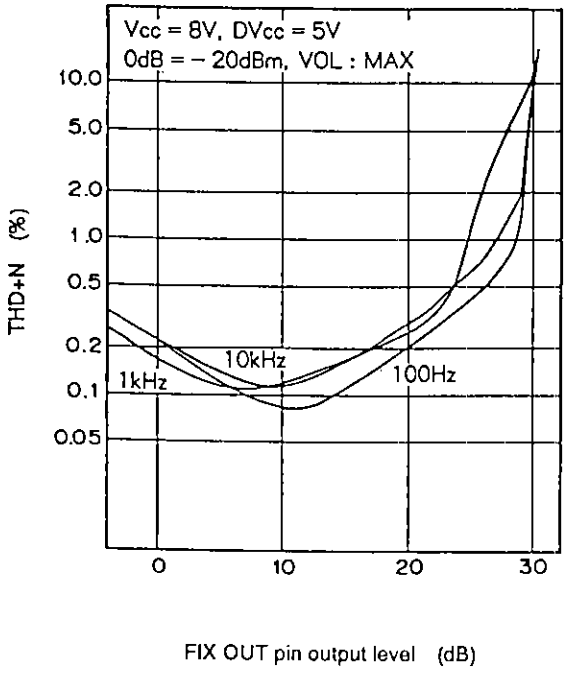
THD vs. OUT characteristics (ALL CUT)



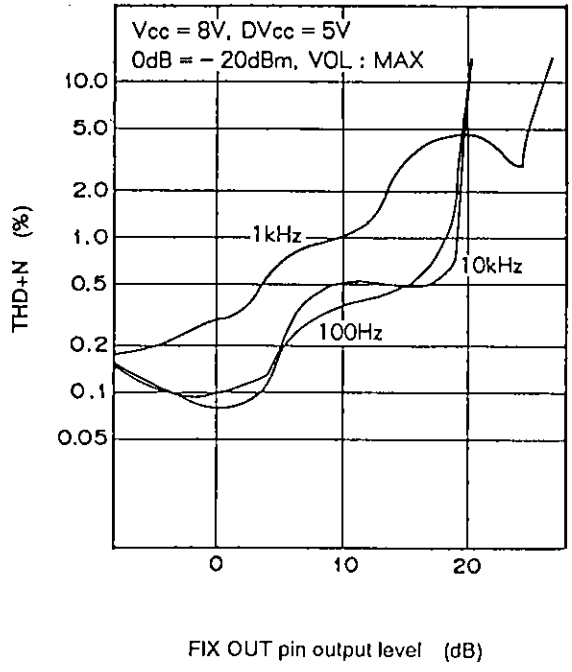
THD vs. F OUT characteristics (ALL FLAT)



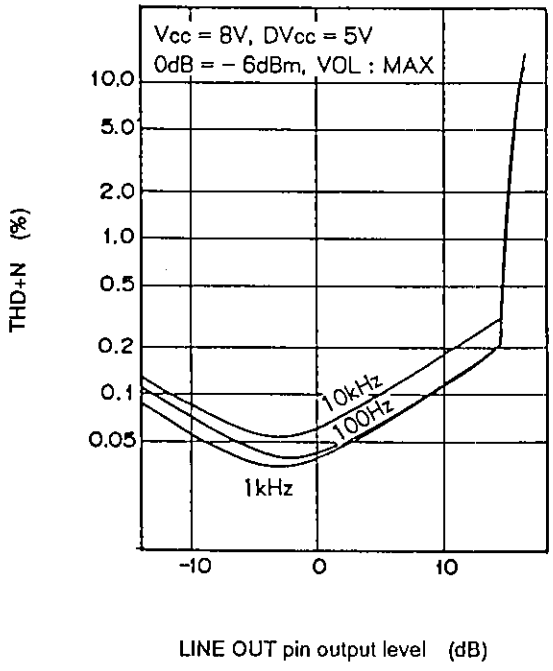
THD vs. F OUT characteristics (ALL BOOST)



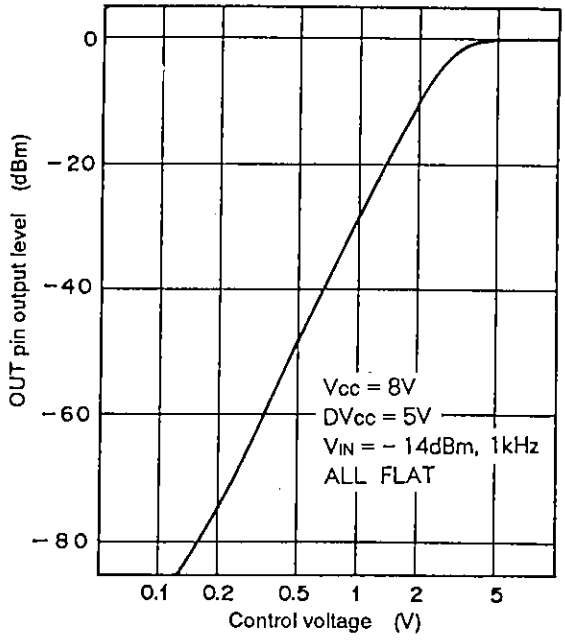
THD vs. F OUT characteristics (ALL CUT)



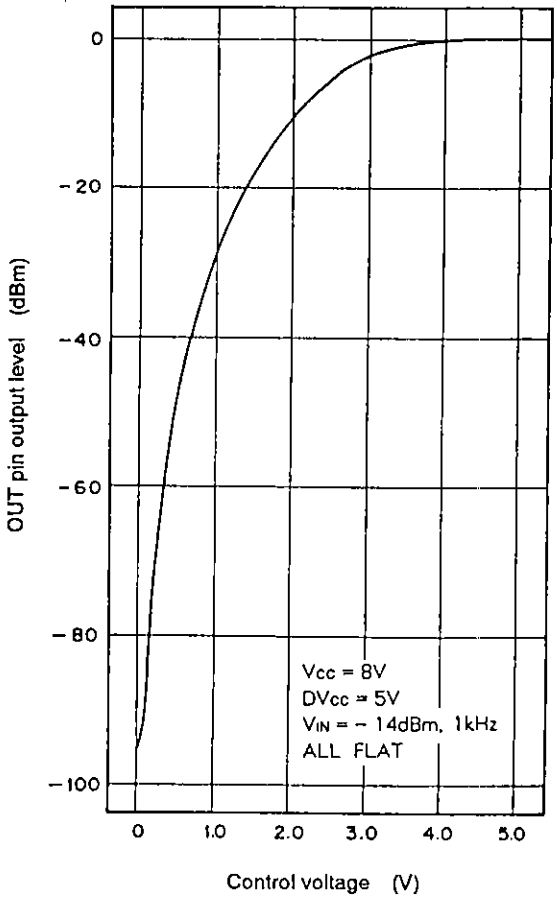
THD vs. L OUT characteristics



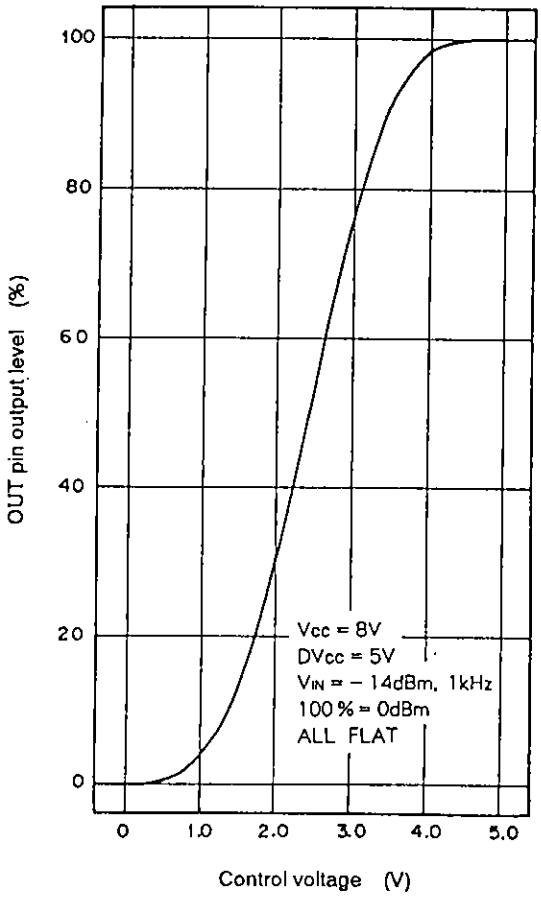
Output voltage vs. Control voltage (VOL)



Output voltage vs. Control voltage (VOL)



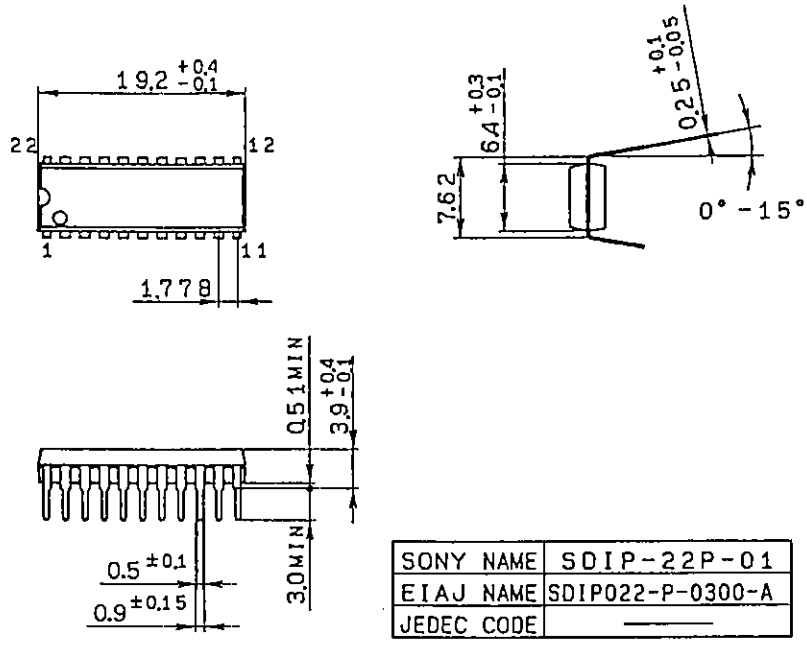
Output voltage vs. Control voltage (VOL)



Package Outline

Unit : mm

22pin SDIP (Plastic) 300mil



SONY NAME	SDIP-22P-01
EIAJ NAME	SDIP022-P-0300-A
JEDEC CODE	———