

SONY**CXA1875AP/AM****8-bit D/A Converter Compatible with I²C Bus****Description**

The CXA1875AP/AM is developed as a 8-bit 5 ch D/A converter compatible with I²C bus.

Features

- Serial control through I²C bus
- 4 built-in general purpose I/O ports (Digital I/O)
- I/O can be specified to respective ports independently
- Selection of 8 slave addresses possible through address select pins (3 pins)

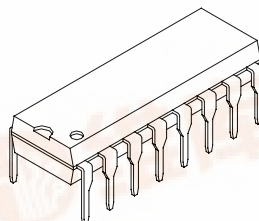
Applications

I²C bus can control ICs that do not correspond to I²C bus by connecting the DC control pins of them.

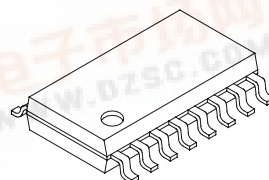
Structure

Bipolar silicon monolithic IC

16 pin DIP (Plastic)



16 pin SOP (Plastic)

**Absolute Maximum Ratings** (Ta=25°C)

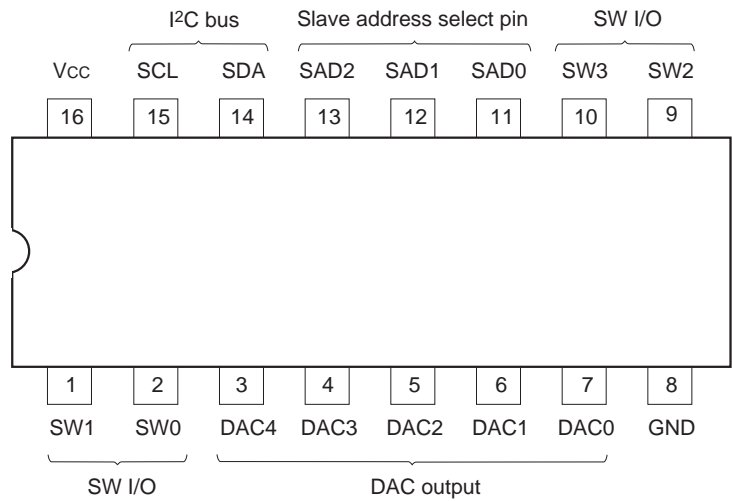
• Supply voltage	V _{cc}	7	V
• Operating temperature	T _{opr}	-20 to +75	°C
• Storage temperature	T _{stg}	-65 to +150	°C
• Allowable power dissipation	P _d	960	mW

Operating Conditions

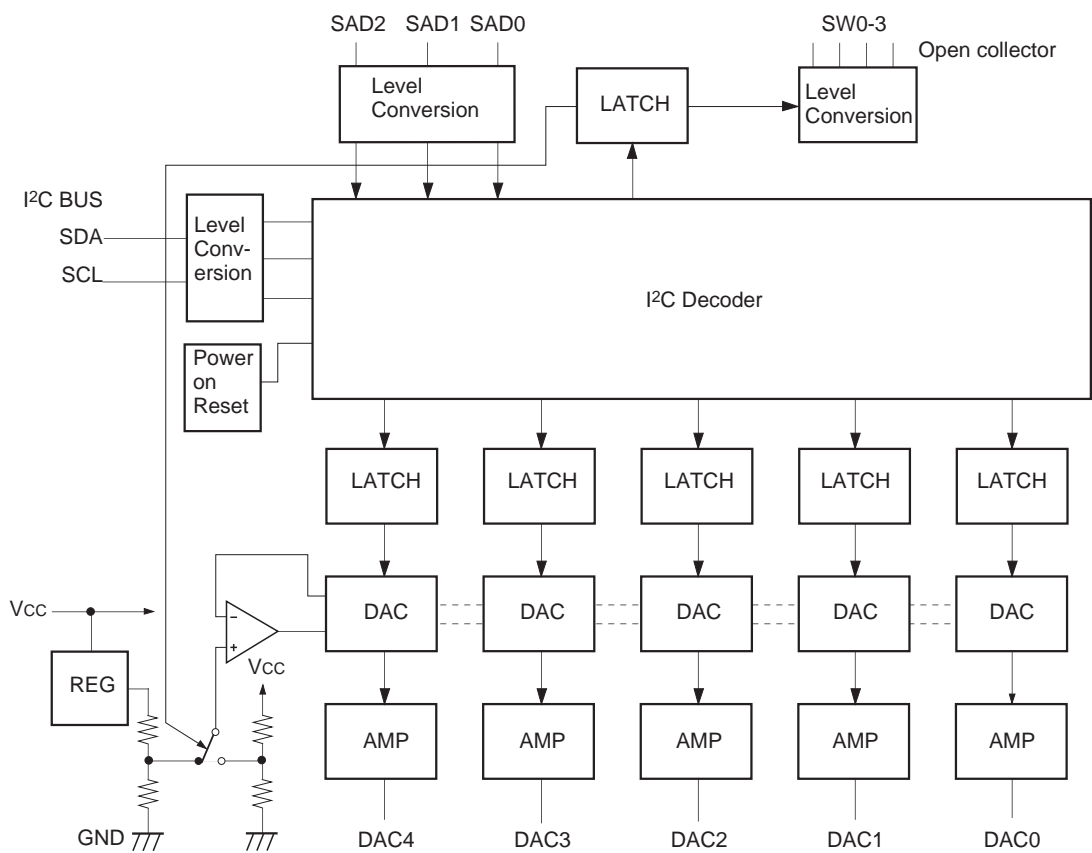
• Supply voltage	V _{cc}	5±0.5	V
• Operating temperature	T _{opr}	-20 to +75	°C

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Pin Configuration (Top View)



Block Diagram



Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 9 10	SW1 SW0 SW2 SW3		I/O pin for general purpose I/O port V_{ILmax} : 1.5 V V_{IHmin} : 3 V V_{OLmax} : 0.4 V
14 15	SDA SCL		SDA I/O pin for I ² C bus
3 4 5 6 7	DAC4 DAC3 DAC2 DAC1 DAC0		D/A converter output pin
8	GND		GND pin
11 12 13	SAD0 SAD1 SAD2		Slave address input pin Input at positive logic V_{ILmax} : 1.5 V V_{IHmin} : 3 V
16	Vcc		Power supply pin

Electrical Characteristics (Ta=25 °C, Vcc=5 V)

D/A Converter Block

No.	Item	Symbol	Test circuit	Test contents	Min.	Typ.	Max.	Unit
1	Circuit current	I _{cc}	1	DAC 0 to 4=127	6	9	12	mA

2	Differential linearity	DLE	1	$\frac{V(DAC0 \text{ to } 4=n+1) - V(DAC0 \text{ to } 4=N)}{V(DAC0 \text{ to } 4=191) - V(DAC0 \text{ to } 4=63)} \times 128 - 1$ n=0 to 127	-1	0	+1	LSB
3	Minimum output voltage	V _{min}	1	DAC 0 to 4=0	0.1	0.4	0.7	V
4	Maximum output voltage	V _{max}	1	DAC 0 to 4=255	4.3	4.6	4.9	V
5	Output current	I _{out}	2	Current that can be flowed from Pins 3 to 7	-1		+1	mA
6	Output impedance	Z ₀	2	DAC 0 to 4=127, $\frac{V(-1 \text{ mA}) - V(1 \text{ mA})}{2 \text{ mA}}$	0	3	6	Ω

SW, SAD Pins

No.	Item	Symbol	Text circuit	Test contents	Min.	Typ.	Max.	Unit
7	Low level input voltage	V _{IL}	3	ST 0 to 3 an input voltage that turns to '0'	—	—	1.5	V
8	High level input voltage	V _{IH}	3	ST 0 to 3 an input voltage that turns to '1'	3.0	—	—	V
9	Low level input current	I _{IL}	3	Input current when 0.4 V is applied	−10	0	+10	μA
10	High level input current	I _{IH}	3	Input current when 4.5 V is applied	−10	0	+10	μA
11	Low level input voltage	V _{OL}	4	SW 0 to 3=1, Output voltage when 1 mA flows in	0	0.2	0.4	V

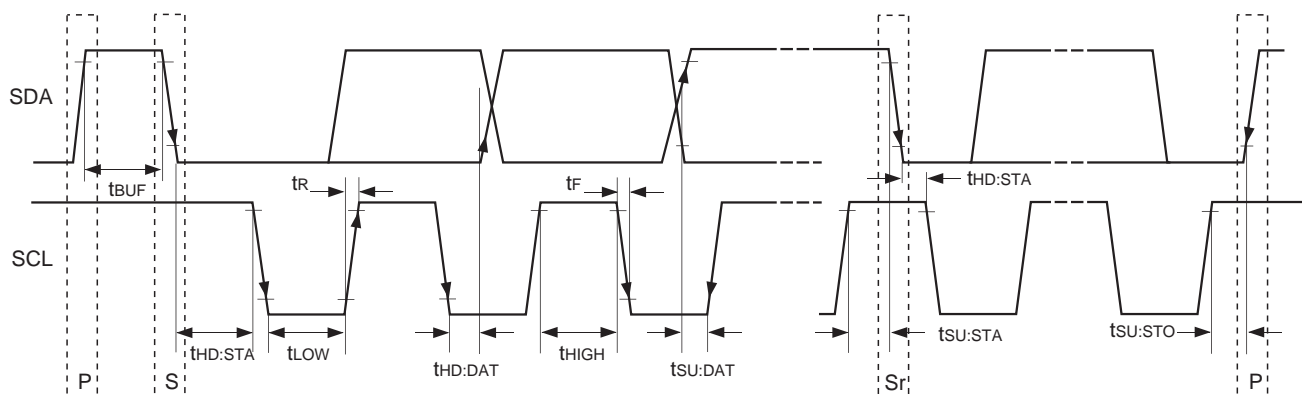
I²C Bus Block Items (SDA, SCL)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
12	High level input voltage	V _{IH}	3.0	—	5.0	V
13	Low level input voltage	V _{IL}	0	—	1.5	V
14	High level input current	I _{IH}	—	—	10	μA
15	Low level input current	I _{IL}	—	—	10	μA
16	Low level output voltage At 3 mA flow to SDA (Pin 14)	V _{OL}	0	—	0.4	V
17	Maximum flowing current	I _{OL}	3	—	—	mA
18	Input capacitance	C _i	—	—	10	pF
19	Maximum clock frequency	f _{SCL}	0	—	100	kHz
20	Data change minimum waiting time	t _{BUF}	4.7	—	—	μs
21	Data transfer start minimum waiting time	t _{HD:STA}	4.0	—	—	μs
22	Low level clock pulse width	t _{LOW}	4.7	—	—	μs
23	High level clock pulse width	t _{HIGH}	4.0	—	—	μs
24	Minimum start preparation waiting time	t _{SU:STA}	4.7	—	—	μs
25	Minimum data hold time	t _{HD:DAT}	5	—	—	μs
26	Minimum data preparation time	t _{SU:DAT}	250	—	—	ns
27	Rise time	t _R	—	—	1	μs
28	Fall time	t _F	—	—	300	ns
29	Minimum stop preparation waiting time	t _{SU:STO}	4.7	—	—	μs

I²C bus load conditions: Pull up resistance 4 kΩ (Connected to +5 V)

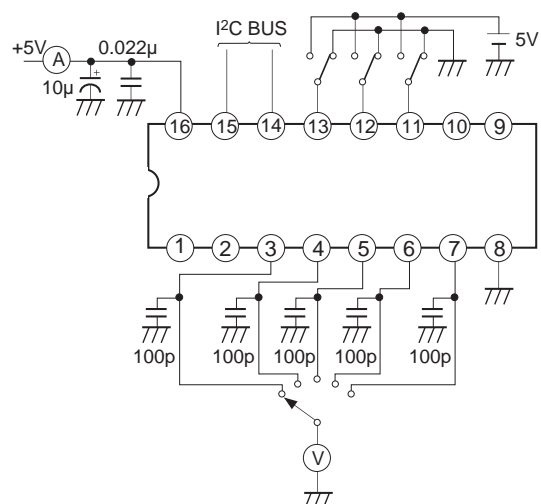
Load capacitance 200 pF (Connected to GND)

I²C Bus Control Signal

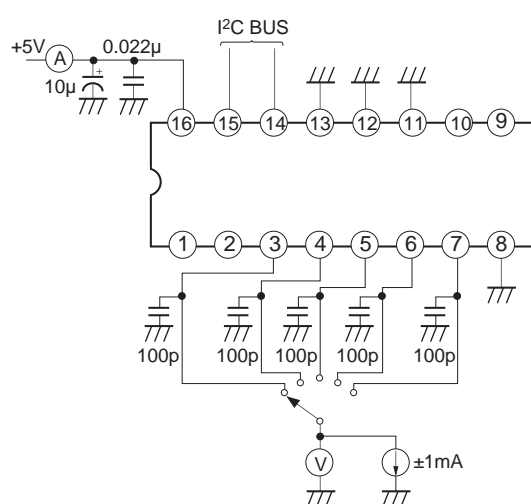


Electrical Characteristics Test Circuit

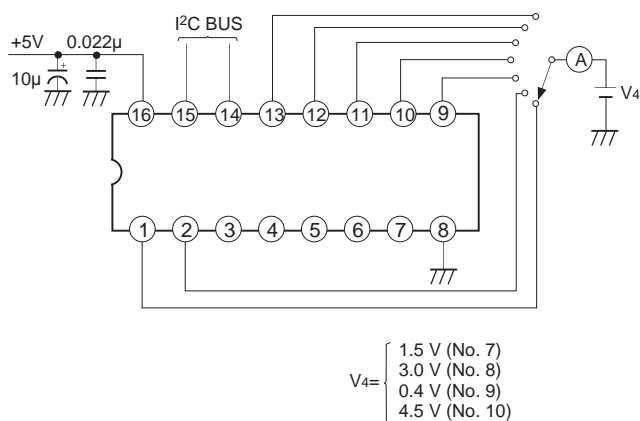
Test circuit 1



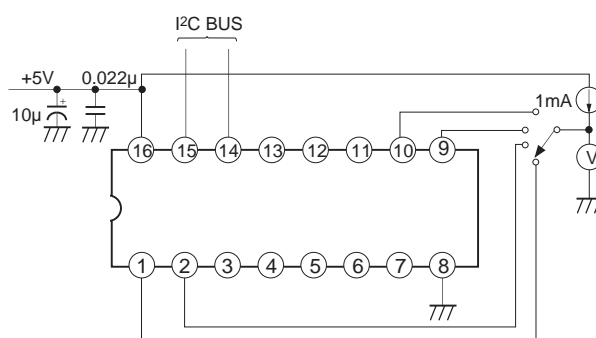
Test circuit 2



Test circuit 3

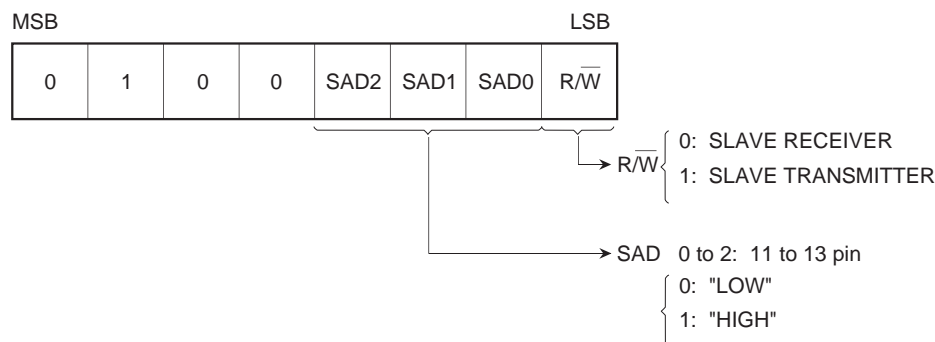


Test circuit 4



Definition of I²C Register

<Slave address>



<Register table>

- With the IC reset all registers are reset to 0
- *: Not defined
- ×: Don't care
- Sub address is auto incremented
- It can be used as a 6-bit D/A converter by setting the lower two bits of DAC 0-4 registers to 0, but take care that the max. voltage of DA output will lower about 100 mV compared with the use of 8 bits.

Control Register

Sub address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
××××× 000	REF	*	*	*	SW3	SW2	SW1	SW0
××××× 001	DAC0 (8)							
××××× 010	DAC1 (8)							
××××× 011	DAC2 (8)							
××××× 100	DAC3 (8)							
××××× 101	DAC4 (8)							

Status Register

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PONRES	0	0	0	ST3	ST2	ST1	ST0

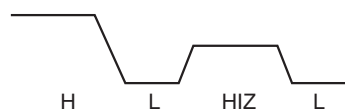
<Registers> In brackets () number of bits

- REF (1): Switches D/A converter reference voltage
 0:Standardizes the inner regulator
 1:Standardizes voltage resistance divided from Vcc
- SW0 to 3 (1): Selects ON/OFF of Pins 1, 2, 9 and 10
 (Each pin is the open collector output of NPN transistor)
 0:OFF
 1:ON
- DAC0 to 4 (8): Digital data input register of D/A converter
 0:Output voltage turns to minimum
 255:Output voltage turns to maximum
- PONRES (1): Detects POWER ON RESET
 0:Master passes from the bus and is reset to 0 after having read this status
 1:Set to 1 when power supply is turned on or when there has been a power dip
- ST0 to 3 (1): Detects and registers the voltage condition of Pins 1, 2, 9 and 10
 0:1.5 V and below
 1:3.0 V and above
 Note) SW0 to 3 effective during 0

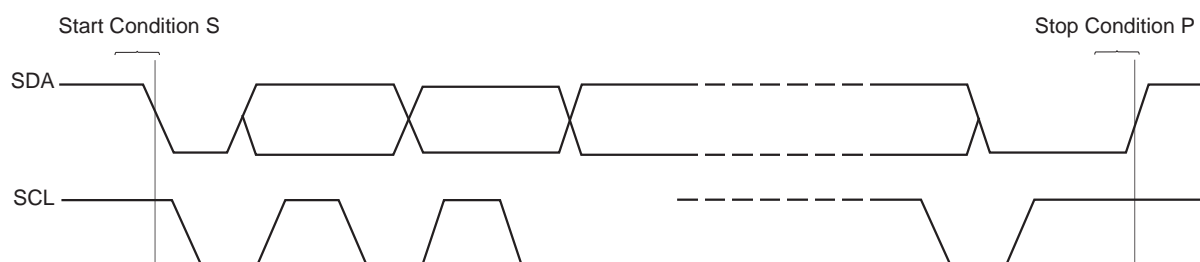
I²C Bus Signal

There are 2 signals in I²C bus. SDA (Serial DAta) and SCL (Serial Clock).
 SDA is double-way.

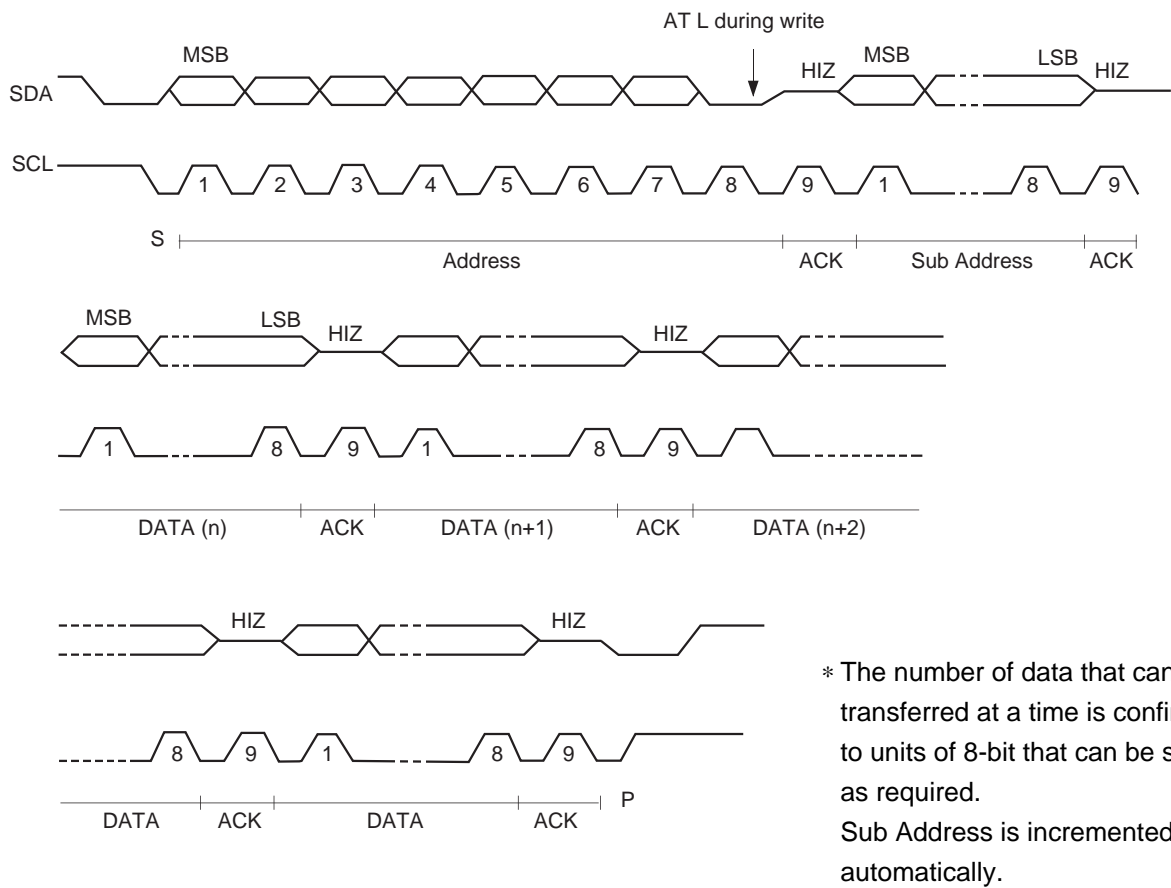
- As SDA is double-way it has 3 state outputs, H, L and HIZ.



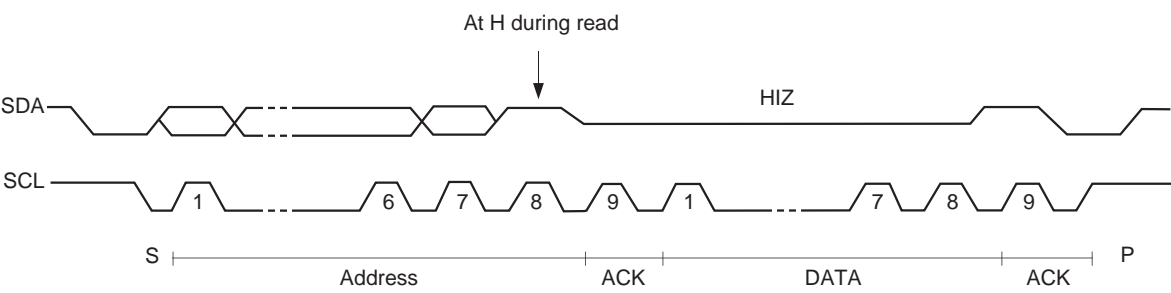
- I²C transfer begins with Start Condition and ends with Stop Condition.



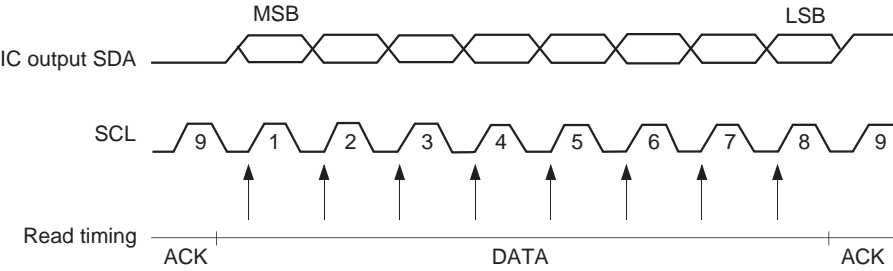
• I²C data write (Write from I²C controller to IC)



• I²C data read (Read from IC to I²C controller)

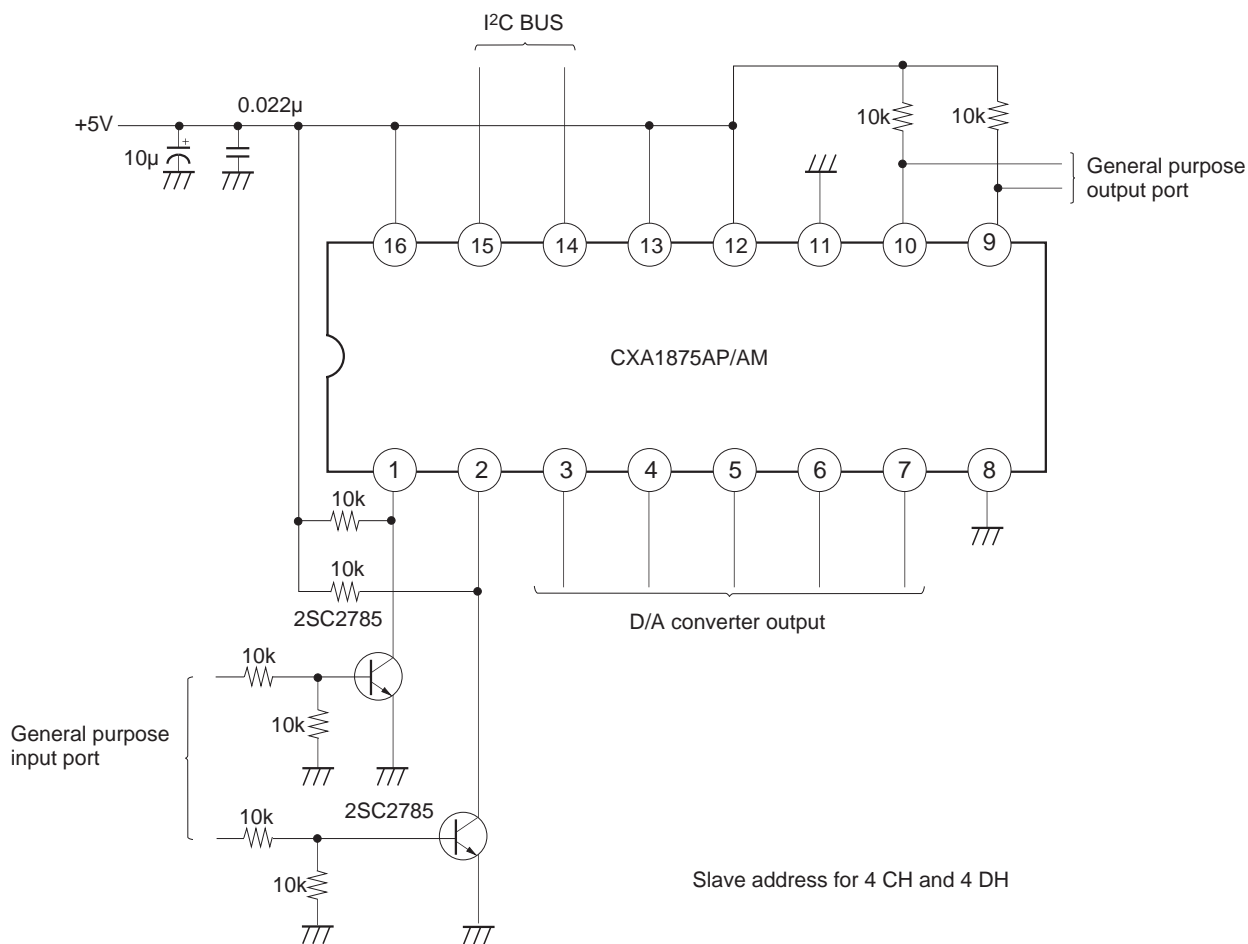


• Read timing



* Data read is performed with SCL rise.

Application Circuit

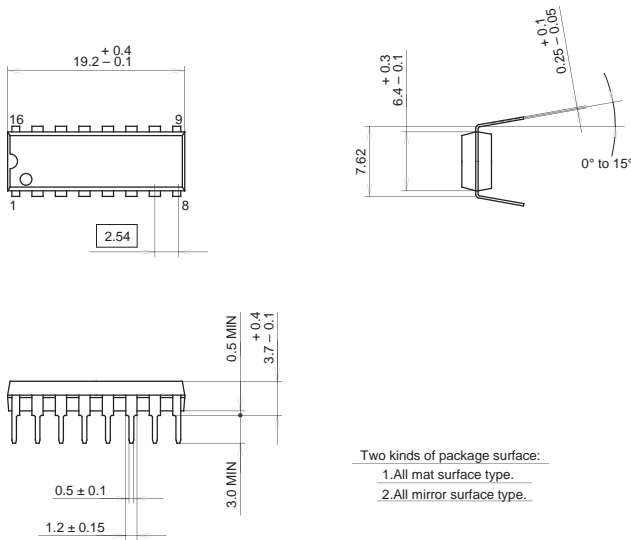


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Package Outline Unit : mm

CXA1875AP

16PIN DIP (PLASTIC)



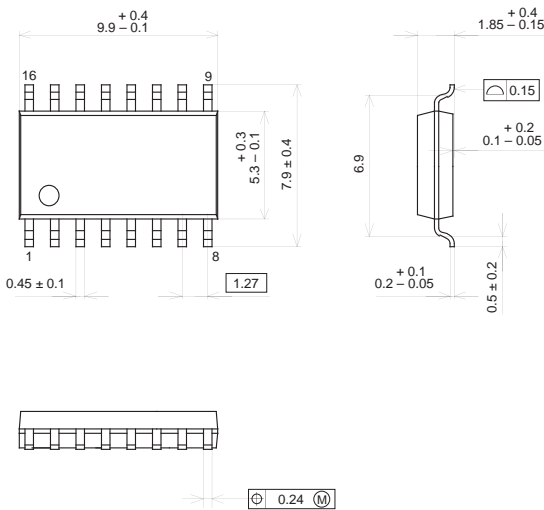
PACKAGE STRUCTURE

SONY CODE	DIP-16P-01
EIAJ CODE	DIP016-P-0300
JEDEC CODE	Similar to MO-001-AE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.0 g

CXA1875AM

16PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

Purchase of Sony's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.