SONY

CXA1951AQ

GPS Down Converter

Description

The CXA1951AQ is an IC developed as a GPS down converter, featuring low current consumption and small package. This IC is suitable for the mobile GPS (Global Positioning System).

Features

- Includes all functions required for the GPS converter
- Total gain: 100 dB or more
- Operating supply voltage range: 2.7 to 5.5 V
- Low current consumption:
  I_{CC} = 30 mA (Typ. at V_{CC} = 3 V)
- Excellent temperature characteristics

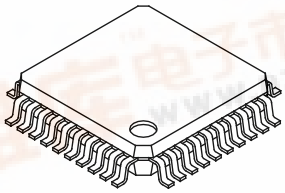
Applications

GPS (Global Positioning System)

Structure

Bipolar silicon monolithic IC

40 pin QFP (Plastic)



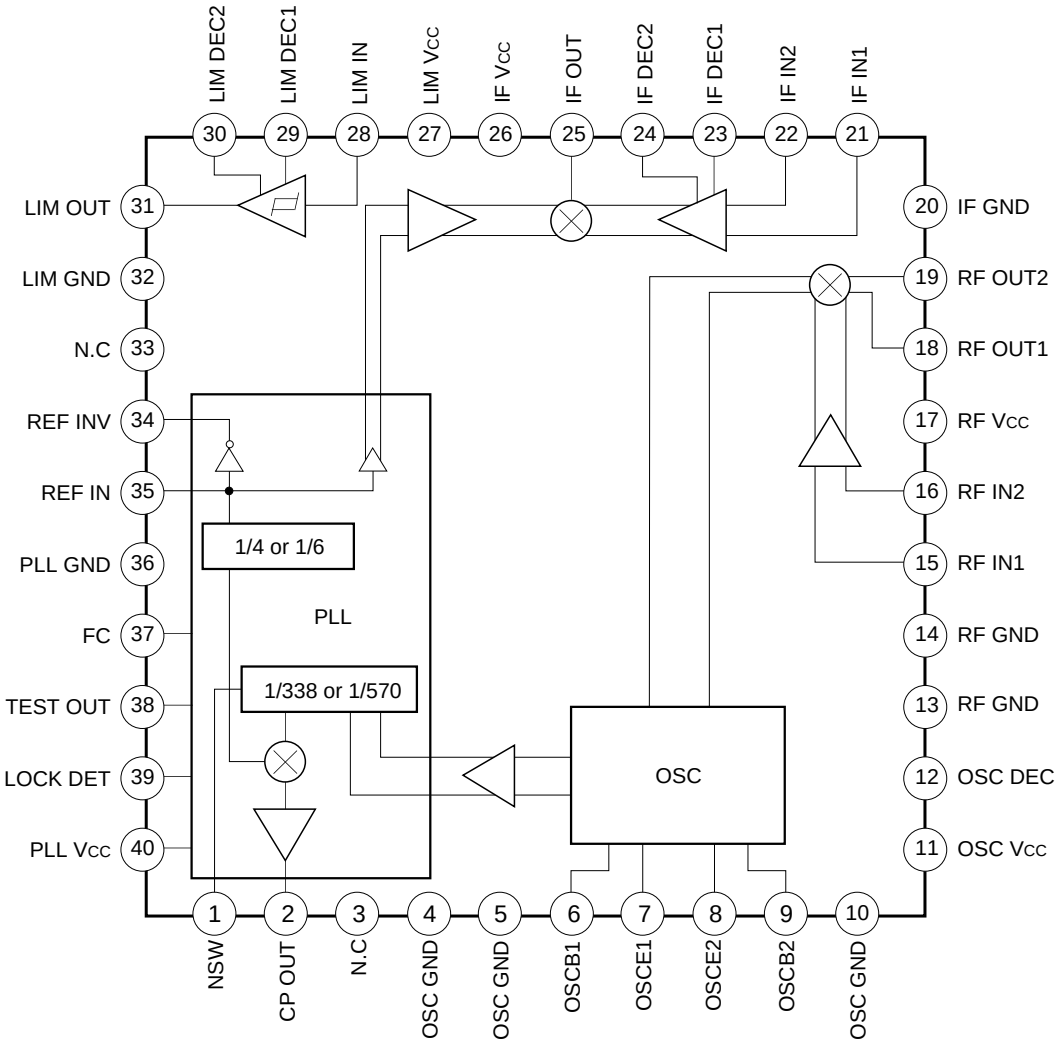
Absolute Maximum Ratings (Ta = 25 °C)

• Supply voltage	V_{CC}	7.0	V
• Operating temperature	Topr	–40 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	200	mW

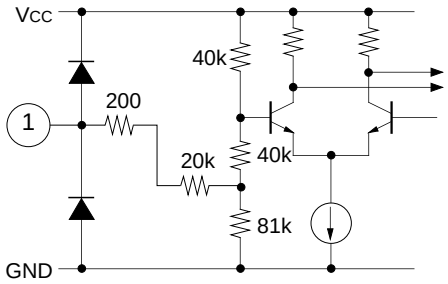
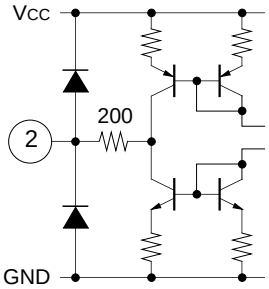
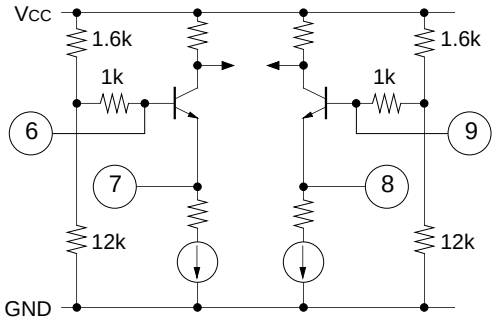
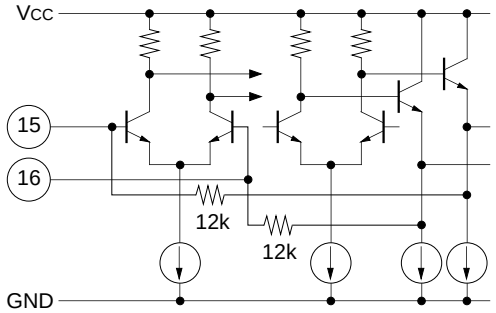
Operating Conditions

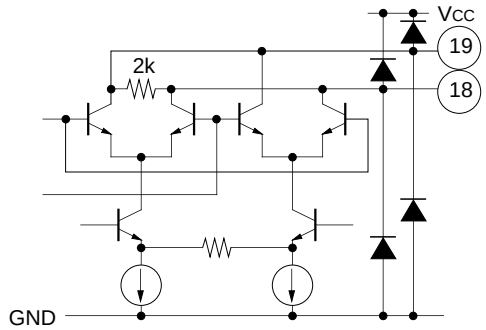
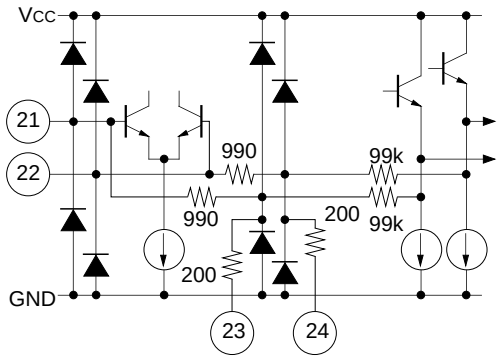
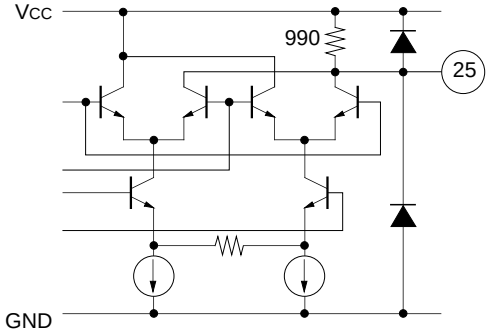
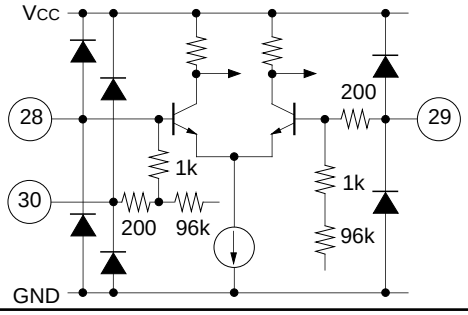
Supply voltage	V_{CC}	2.7 to 5.5	V

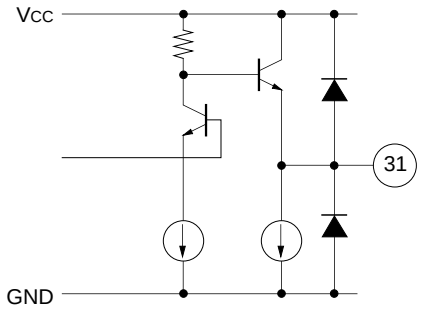
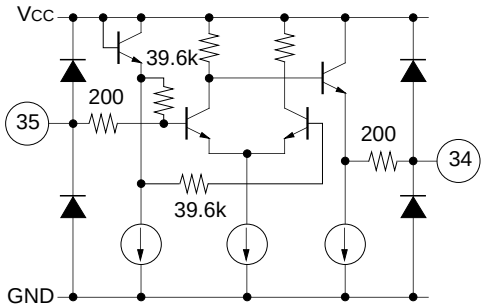
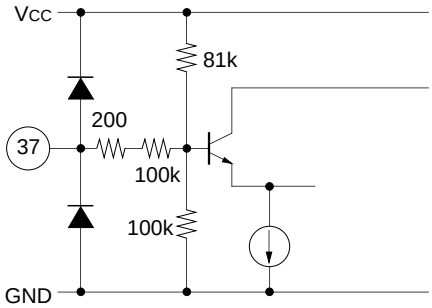
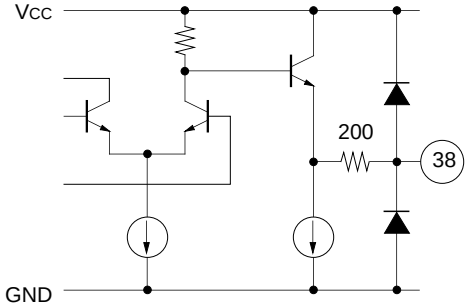
Block Diagram and Pin Configuration

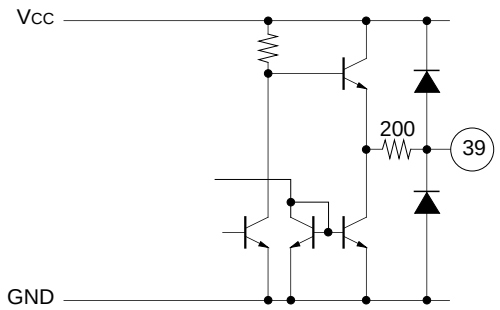


Pin Description

Pin No.	Symbol	Pinvoltage	Equivalent circuit	Description
1	NSW	—		Internal PLL frequency division value switching
2	CPOUT	—		Charge pump output
3, 33	NC	—		Not connected
4, 5, 10	OSC GND	0 V		Ground for the internal oscillator
6 9 7 8	OSCB1 OSCB2 OSCE1 OSCE2	2.5 V 1.7 V 1.7 V 2.5 V		Connects the internal oscillator resonator. Connects to main counter input via the internal buffer.
11	OSC Vcc	3 V		Internal oscillator power supply
12	OSC DEC	1.7 V		Connects decoupling capacitor for the internal oscillator bias power supply
13, 14	RF GND	0 V		RF amplifier ground
15, 16	RF IN1 RF IN2	1.6 V 1.6 V		RF amplifier input. When using as a single input, ground Pin 16 via the capacitor.

Pin No.	Symbol	Pinvoltage	Equivalent circuit	Description
17	RF Vcc	3 V		RF amplifier power supply
18, 19	RF OUT1 RF OUT2	— —		RF amplifier mixer output
20	IF GND	0 V		IF amplifier ground
21, 22	IF IN1 IF IN2	1.9 V 1.9 V		IF amplifier input
23, 24	IF DEC1 IF DEC2	1.9 V 1.9 V		IF amplifier decoupling
25	IF OUT	2.7 V		IF amplifier mixer output
26	IF Vcc	3 V		IF amplifier power supply
27	LIM Vcc	3 V		Limiter buffer power supply
28	LIM IN	2.1 V		Limiter input
29, 30	LIM DEC1 LIM DEC2	2.1 V 2.1 V		Limiter decoupling

Pin No.	Symbol	Pinvoltage	Equivalent circuit	Description
31	LIM OUT			Limiter buffer output
32	LIM GND	0 V		Limiter buffer ground
34	REF INV	High: 2.2 V Low: 2.0 V		Reference frequency signal output. The reference frequency signal can also be made by connecting this pin and Pin 35 with a crystal oscillator to configure an oscillator.
35	REF IN	2.1 V		Reference frequency input and reference counter input
36	PLL GND	0 V		PLL ground
37	FC	—		Switching for the charge pump output status and for the signal output to Pin 38
38	TEST OUT	High: 2.2 V Low: 2.0 V		Output of the frequency division signal by the counter

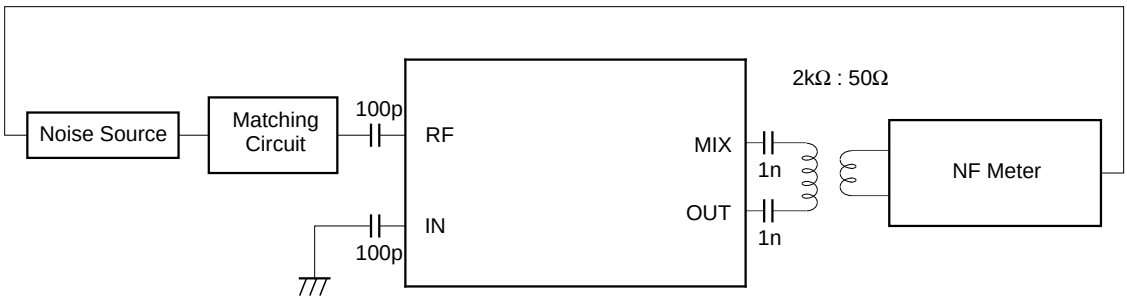
Pin No.	Symbol	Pinvoltage	Equivalent circuit	Description
39	LOCK DET	High: 2.2 V Low: 0.1 V		Lock detection signal output
40	PLL Vcc	3 V		PLL power supply

Electrical Characteristics (V_{CC} = 3 V, Ta = 25 °C)

Item			Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption			I_{CC}			30	40	mA
Front-end conversion gain			CGmix1	fin = 1575.42 MHz, –60 dBm fout = 20.46 MHz fosc = 1554.96 MHz, –10 dBm	14	16		dB
2nd mixer conversion gain			CGmix2	fin = 20 MHz, –60 dBm fref = 16 MHz, –10 dBm	24.5	26.5		dB
Limiter gain			PGlim	fin = 4 MHz, –80 dBm	59	63		dB
Limiter output level			Volim	fin = 4 MHz, –30 dBm	0.7	0.75	0.8	Vp-p
FC	Input High current		I_{IH}	Pin = V_{CC}		9.5	14	µA
	Input Low current		I_{IL}	PIN = GND	–16.5	–11.5		µA
NSW	Input High current		IFCin	Pin = V_{CC}		25	36	µA
	Input Low current		IFCin	PIN = GND	–36	–25		µA
Charge pump output current		H	I_{OH}	Vcpout = V_{CC}/2	–3	–2		mA
		L	I_{OL}	Vcpout = V_{CC}/2		2	3	mA
LOCK DET output voltage		H	V_{OH}	Load current = 0.1 mA	2			V
		L	V_{OL}	Load current = 0.1 mA			500	mV
1st IF output resistance			Romix1	Balanced output	1.4	2	2.6	kΩ
1st IF input resistance			Rimix2	Single input	0.84	1.2	1.56	kΩ
2nd IF output resistance			Romix2	Single output	0.69	1	1.3	kΩ
Limiter input resistance			Rilim	Single input	0.84	1.2	1.56	kΩ

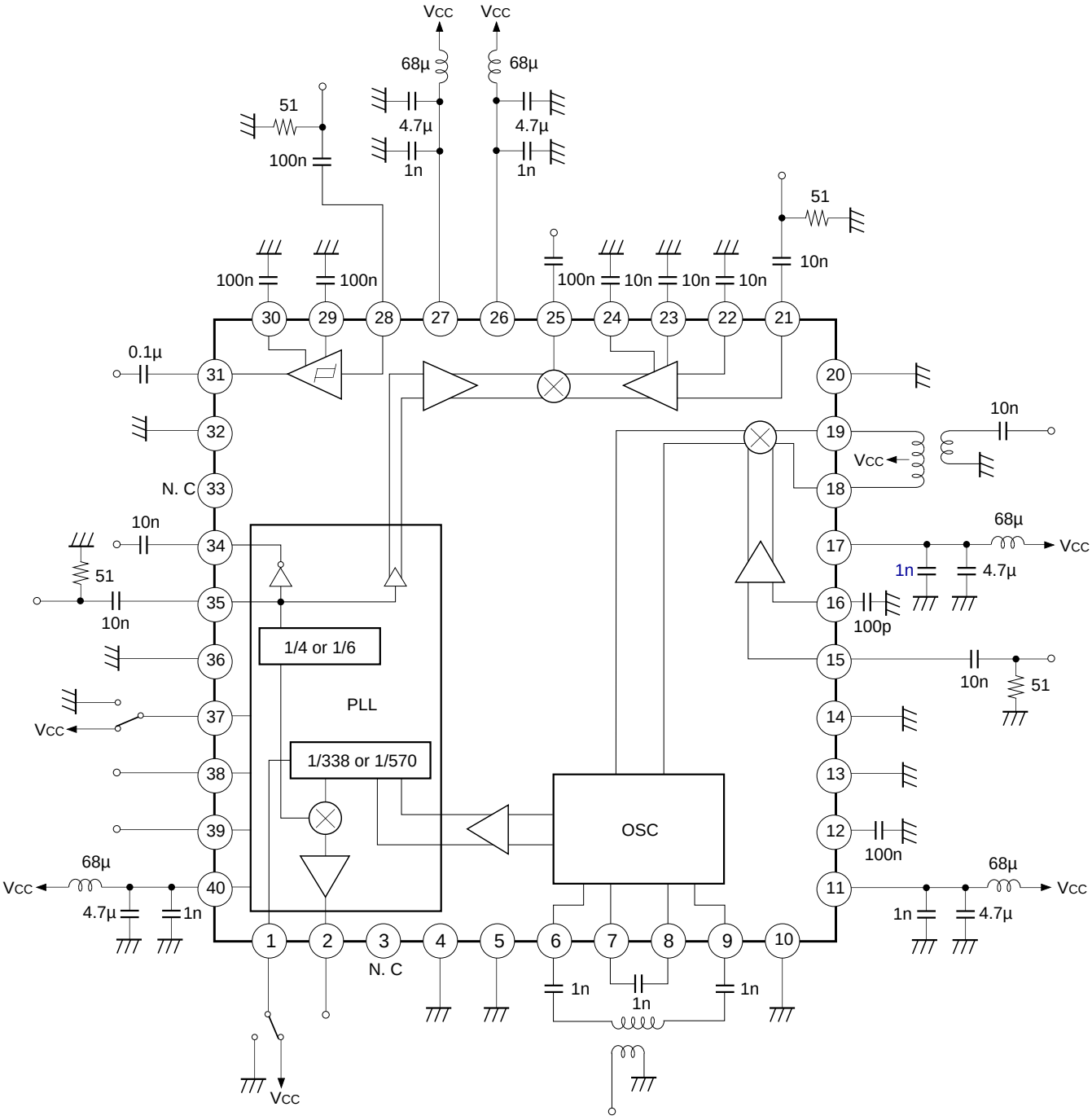
Design Reference Values (Vcc = 3 V, Ta = 25 °C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Noise figure	NF	f = 1.58 GHz DBS measurement		7		dB
1st IF output capacitance		Balanced output		2		pF
1st IF input capacitance		Single input		2		pF
2nd IF output capacitance		Single output		2		pF
Limiter input capacitance		Single input		2		pF
IF amplifier band width	BWif	Input Level = –60 dBm		41		MHz

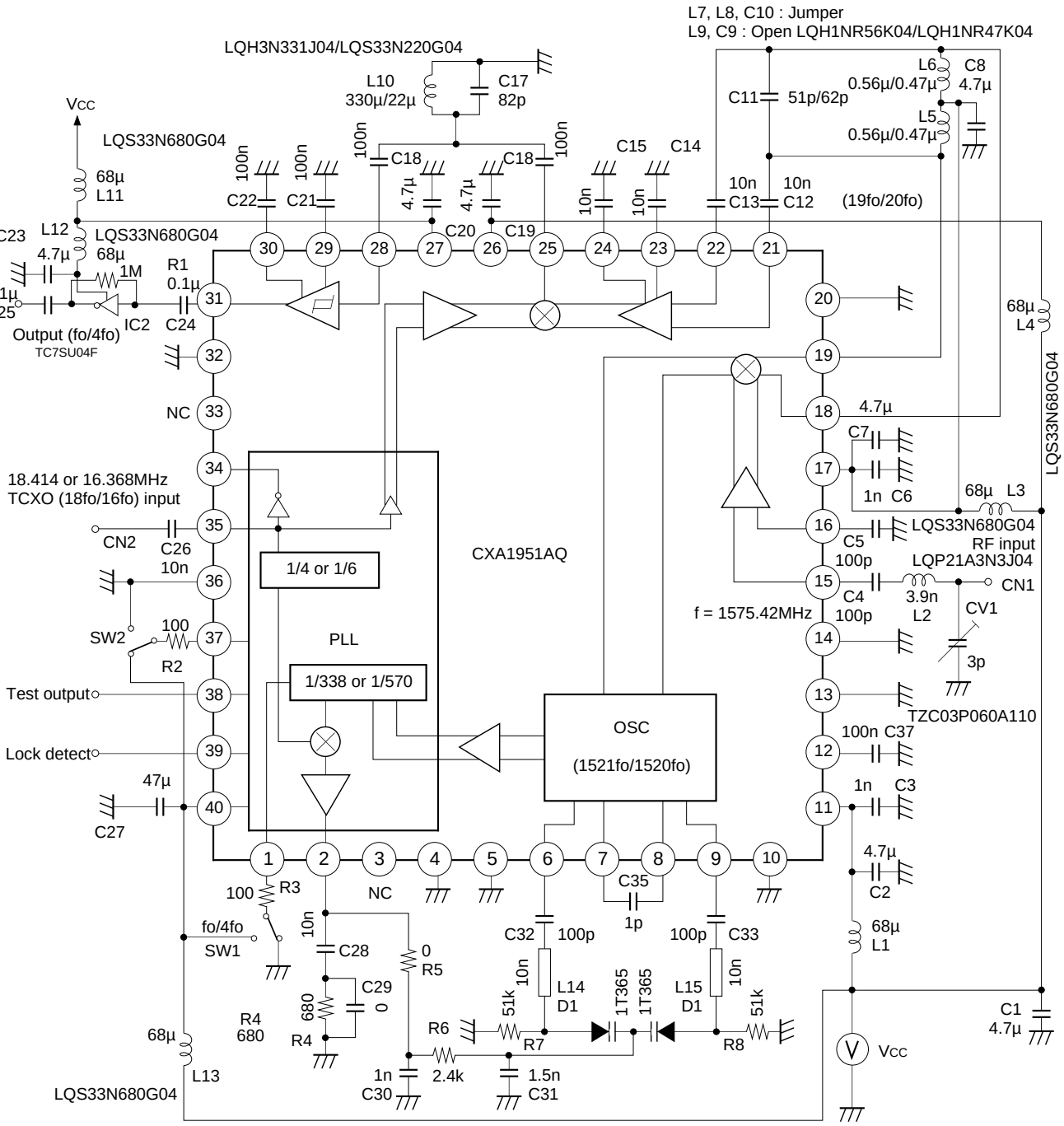


NF Measurement

Electrical Characteristics Measurement Circuit



Application Circuit



Notice: Two component values are indicated, the order is depending on the output frequency.
The first value is as for 'fo output' and the second value is as for '4fo output'.

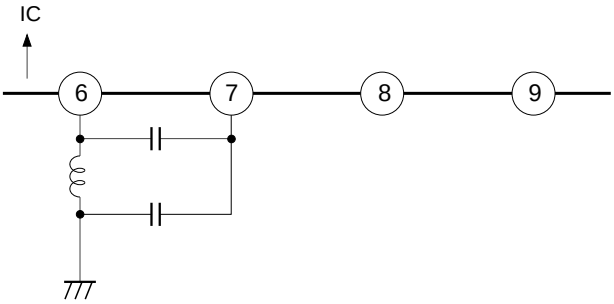
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

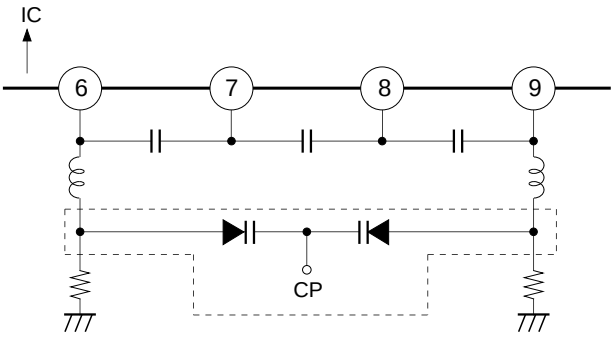
This IC down-converts the GPS (Global Positioning System) frequency of 1.57542 GHz to fo (fo: 1.023 MHz) or 4fo.
The internal configuration is divided into the analog block, consisting of the amplifier and mixer, and the digital block (including limiter), which forms the PLL.
The two-stage analog block has an external filter; it converts the frequency and amplifies the signal. The PLL frequency division ratio can be switched in the digital block in order to down-convert the output signal to fo or 4fo.

1. Oscillator

Transistor and bias circuits are incorporated in this IC. A Colpitts or Hartley oscillator can be configured by adding an external resonator. Also, the oscillator is a paired circuit so as to enable balanced output.



Example of Colpitts Oscillator Configuration (one side)



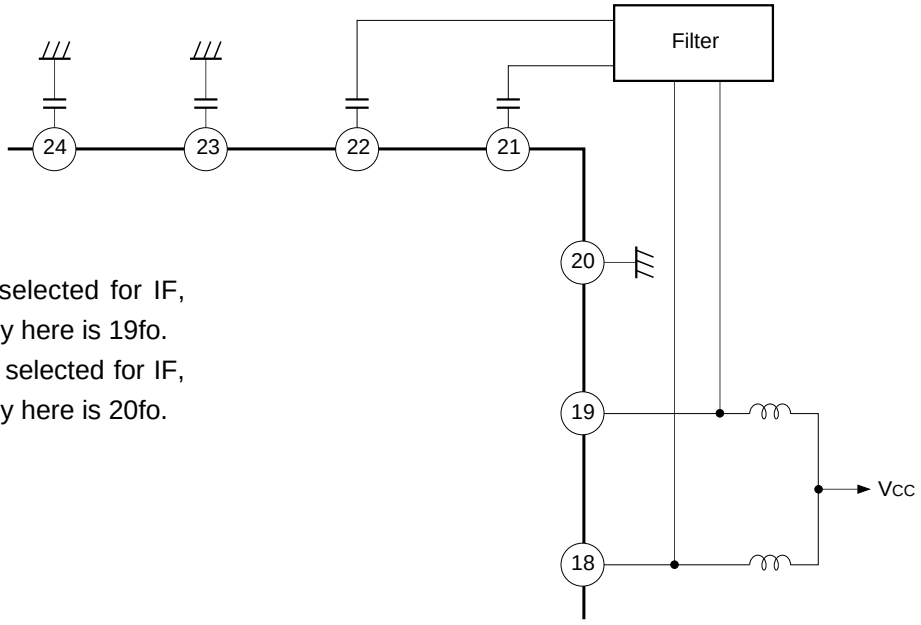
Example of Balanced Configuration

A varactor (variable capacitance) diode, as shown by the dotted line, is added to this IC to configure a VCO, and the resonant frequency is varied depending on the control voltage of Pin 2 (charge pump output) to CP.

2. 1st IF Output

Pins 18 and 19 are open collector outputs.

The bias signal is supplied by the coils, and the output is connected to the 2nd mixer input Pins 21 and 22 via the filter. Use a capacitor to cut direct current. Decoupling for Pins 23 and 24 should be done as close to the IC as possible.



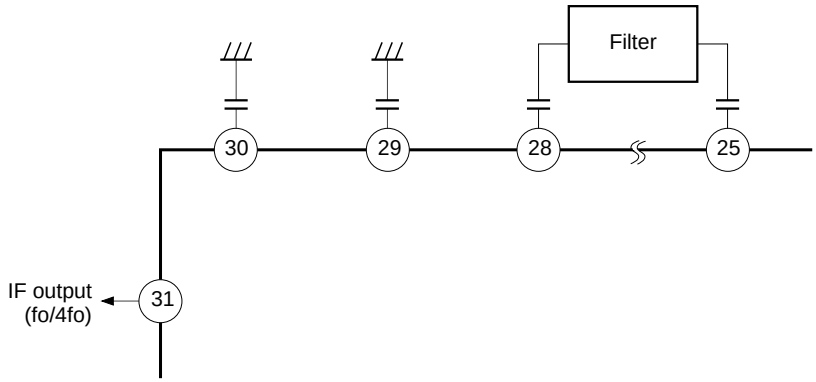
When fo is selected for IF, the frequency here is 19fo. When 4fo is selected for IF, the frequency here is 20fo.

3. 2nd IF Output

Pin 25 is emitter follower output.

After passing via the filter, the direct current is cut, and input is to the limiter input Pin 28. fo or 4fo is output from the limiter output Pin 31. (Pin 31 is emitter follower output.)

Decoupling for Pins 29 and 30 must be done as close to the IC as possible.



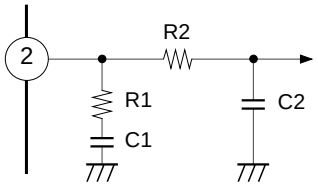
4. NSW (Pin 1)

The internal counter frequency division value is determined by connecting this pin to V_{CC} or GND when selecting fo or 4 fo for IF, as shown in the table below.

IF	fo	4fo
NSW	V_{CC}	GND
VCO counter	338 frequency division	570 frequency division
Reference frequency counter	4 frequency division	6 frequency division

5. CPOUT (Pin 2)

A current output charge pump configures an external loop filter for VCO control voltage.



6. FC (Pin 37)

This pin performs two functions when connected to V_{CC} or GND; CPOUT (Pin 2) output status switching and TEST OUT (Pin 38) selector switch. (See Table 1)

7. TEST OUT (Pin 38)

This is the monitor pin for the internal counter frequency division output.

The frequency division signals for VCO counter and reference frequency counter can be switched depending on FC status. (See Table 1)

	FC to V_{CC}		FC to GND	
	CPOUT	TESTOUT	CPOUT	TESTOUT
fr > fm	L	fr	H	fm
fr = fm	Z	fr	Z	fm
fr < fm	H	fr	L	fm

Table 1

Z: High-impedance
H: High
L: Low

fr: Reference frequency counter output frequency
fm: VCO counter output frequency

8. LOCK DET (Pin 39)

This pin detects PLL lock status. When PLL is not locked, the pin voltage is not set; when locked, it is 2V DC.

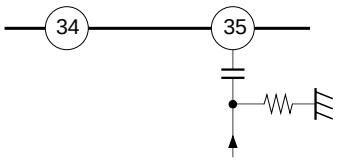
Note) • The voltages mentioned are for supply voltage of 3 V, load current of 100 µA.
• A thin pulse will be observed on monitoring this pin with an oscilloscope, but this is normal.

9. REF IN (Pin 35) and REF INV (Pin 34)

The signal input from the external oscillator to REF IN can be used as the reference signal. Further, a reference signal can be generated by connecting a crystal oscillator between Pin 35 and Pin 34.

(1) Example of reference signal generated by the external oscillator

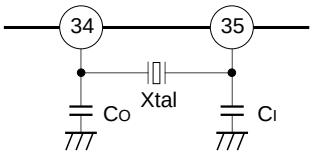
As shown in the figure below, input to RFIN via the capacitor to use the external oscillator signal as the reference signal.



(2) Example of reference signal generated by the crystal oscillator

As shown below, connect the crystal oscillator between Pin 34 and Pin 35, making sure that the oscillation stability, etc. is satisfactory.

Further, the capacitance ratio of C_I and C_O should be 1 to 2 : 1 (C_I : C_O). Select the capacitance values so that the serial capacitance of C_I and C_O may be the load capacitance specified by the crystal oscillator.

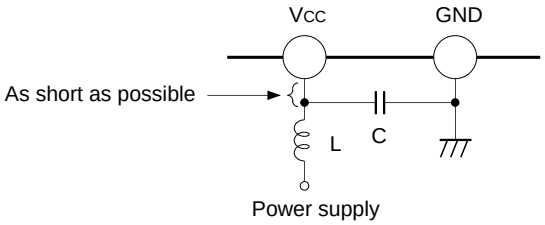


10. Power supply pin and OSC DEC (Pin 12) decoupling

This IC has five power supply and ground systems, due to the following reasons:

1) It handles high frequency signals.
2) The total gain is high. (100 dB or more)
3) It combines analog and digital blocks.

Therefore, it is absolutely necessary to decouple these power supply lines as close to the IC as possible. When necessary, insert the inductor (about 6.8 µ) in series in the power supply line.

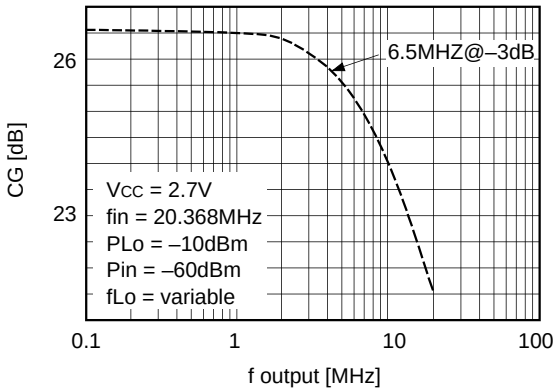


OSC DEC is the internal reference voltage decoupling pin, and must be grounded with a capacitor (about 100 nF).

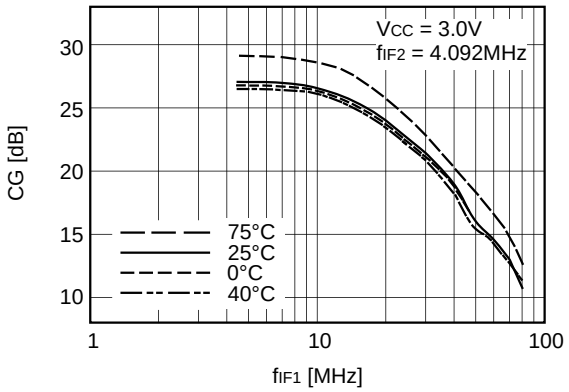
Notes on Operation

Make sure to take measures for static electric damage because the high frequency signals are handled so that protection elements are omitted from this IC.

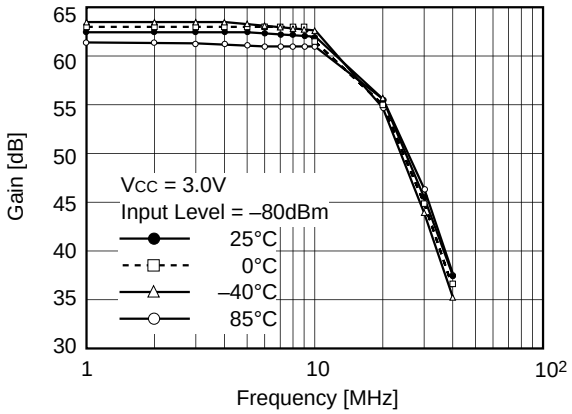
2nd Mixer BW (O/P)



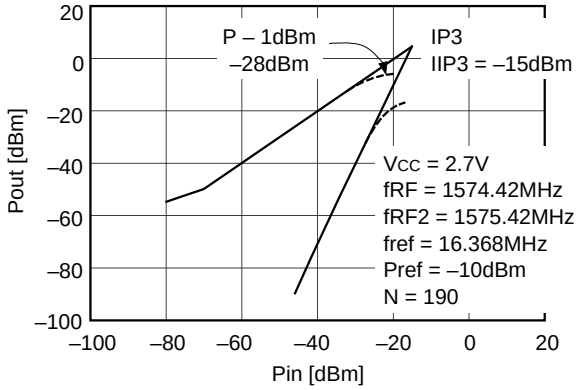
2nd Mixer Conversion Gain



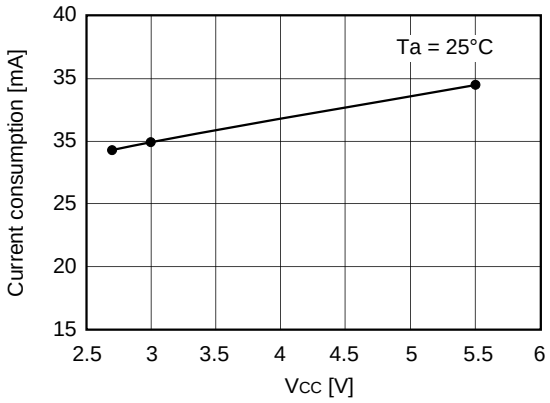
Lim Amp Gain



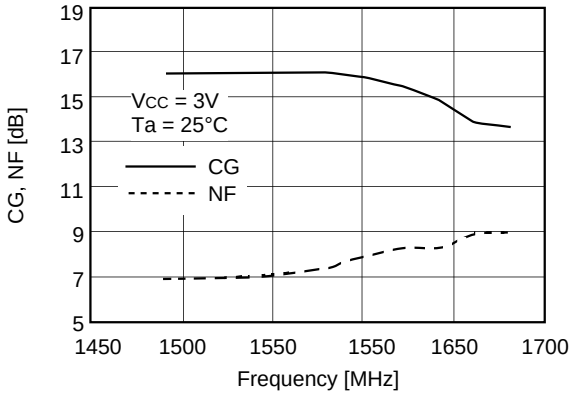
F/E 2-signal characteristics



VCC vs. Current consumption

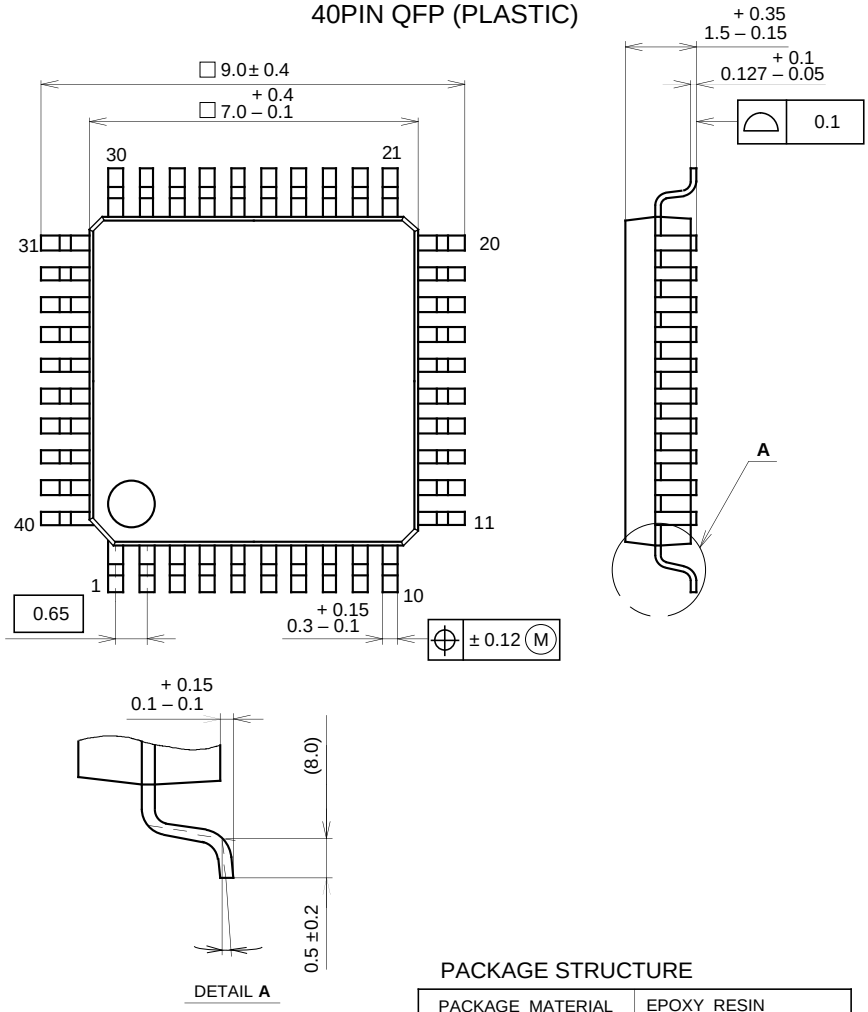


Front End conversion GAIN, NF



Package Outline Unit : mm

40PIN QFP (PLASTIC)



SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g