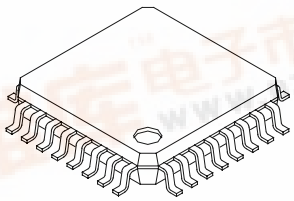
SONY

CXA2006Q

Digital CCD Camera Head Amplifier

32 pin QFP (Plastic)



Description

The CXA2006Q is a bipolar IC developed as a head amplifier for digital CCD cameras. This IC provides the following functions: correlated double sampling, AGC for the CCD signal, GCA for the low-band chroma signal, AMP for high-band chroma and line signals, A/D sample and hold, blanking, A/D reference voltage, and an output driver.

Features

- High sensitivity made possible by a high-gain AGC amplifier
- Blanking function provided for the purpose of calibrating the CCD output signal black level
- Regulator output pin provided for A/D converter reference voltage
- Built-in GCA and AMP for amplifying video signals (chroma and line signals) from external sources
- Built-in sample-and-hold circuits (for camera signals and for video signals) required by external A/D converters

Absolute Maximum Ratings

• Supply voltage	V_{CC}	14	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	640	mW

Operating Conditions

Supply voltage	V_{CC}1, 2, 3	4.5 to 5	V

Applications

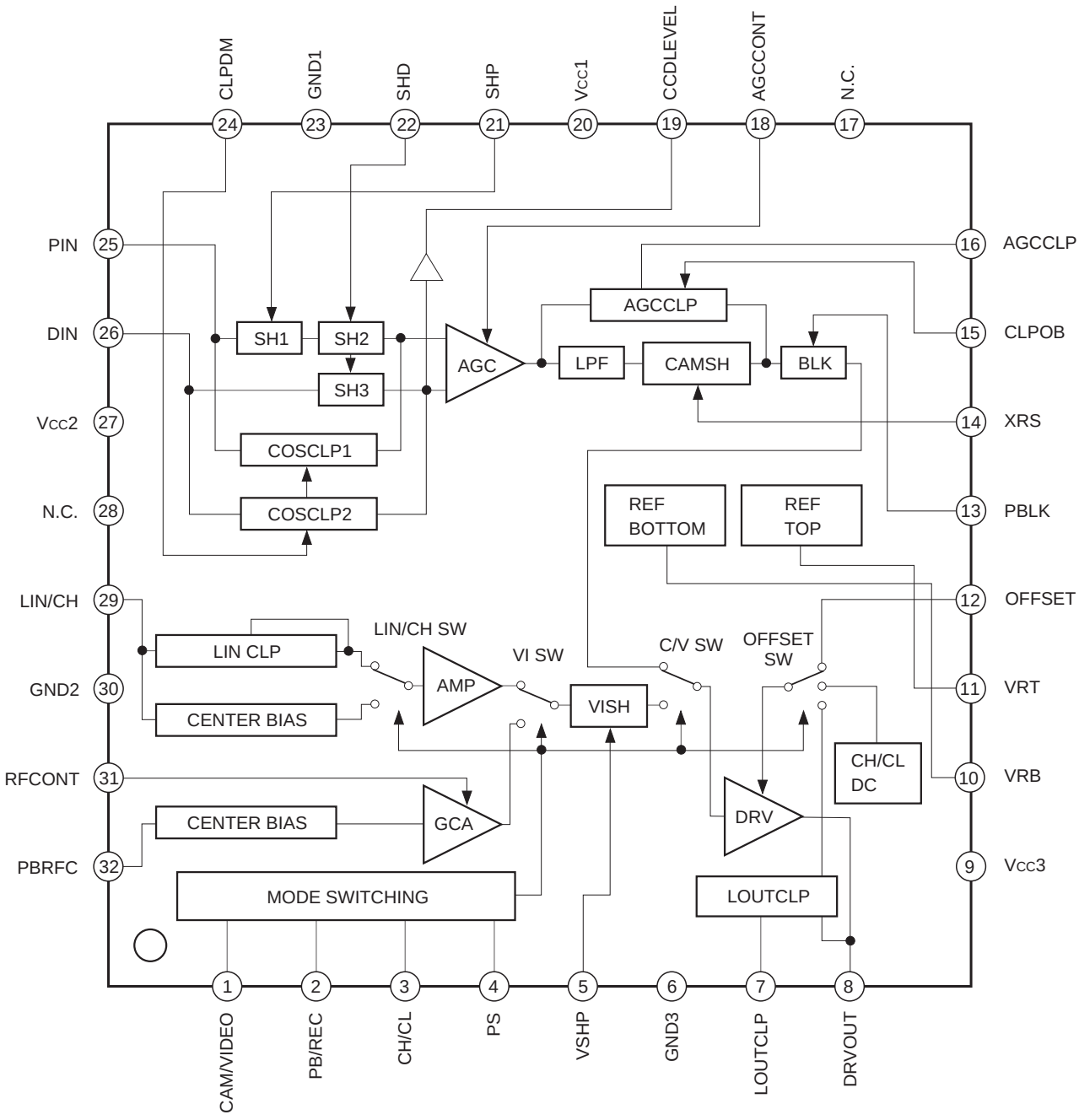
Digital CCD cameras

Structure

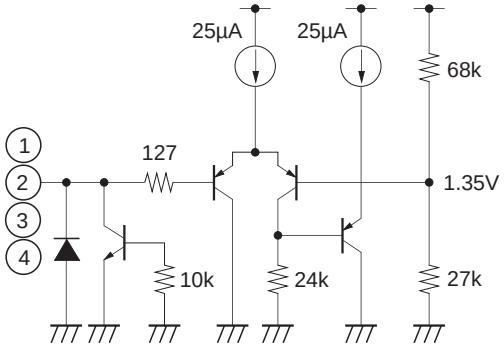
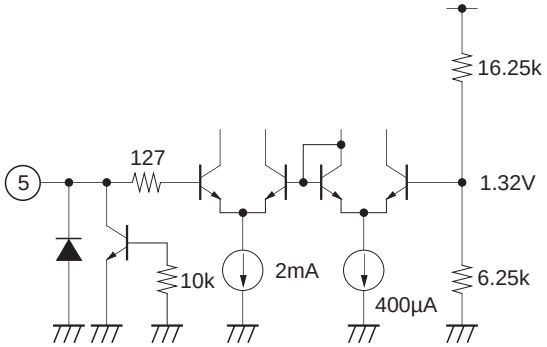
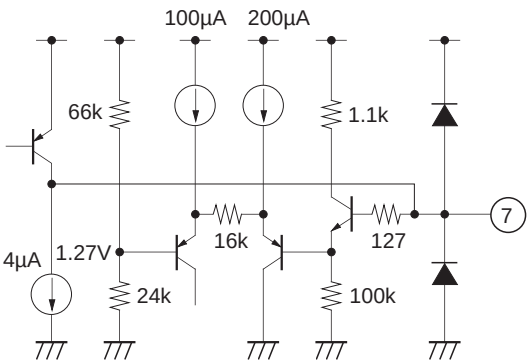
Bipolar silicon monolithic IC

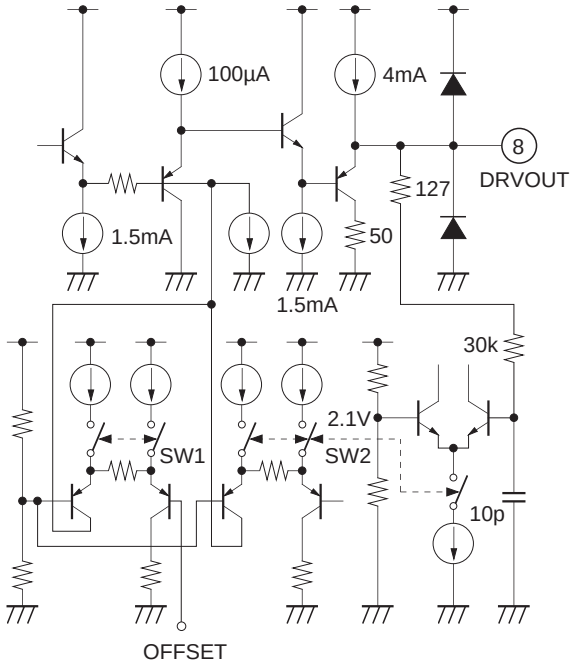
E94X41B8X-PS

Block Diagram and Pin Configuration

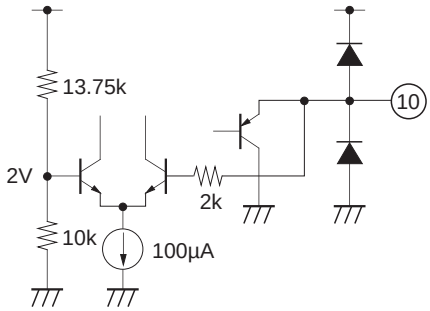


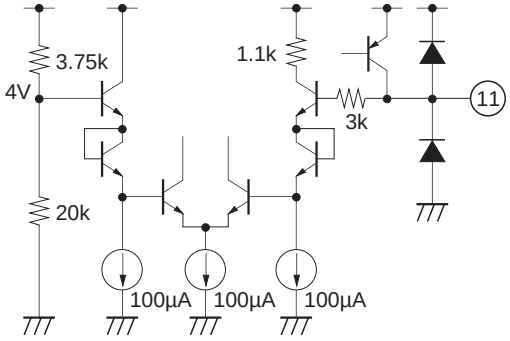
Pin Description (V_{CC}1, 2, 3 = 4.75V)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	CAM /VIDEO	VTH = 1.35V		Camera and video signal selector.
2	PB/REC			Chroma signal and composite video signal selector.
3	CH/CL			High-band chroma signal and low-band chroma signal selector.
4	PS			Power save mode.
5	VSHP	Sampling VTH = 1.32V 		Sample-and-hold pulse input for video.
6 23 30	GND3 GND23 GND2	GND		Ground.
7	LOUTCLP	Approx. 2V		Capacitor connection for LOUTCLP which clamps the output minimum level in modes which pass the composite video signal. (Recommended value: 0.1µF)

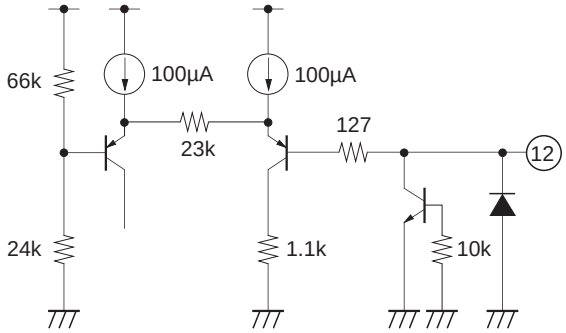
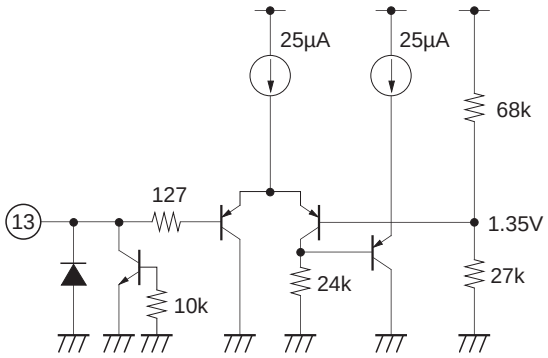
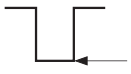
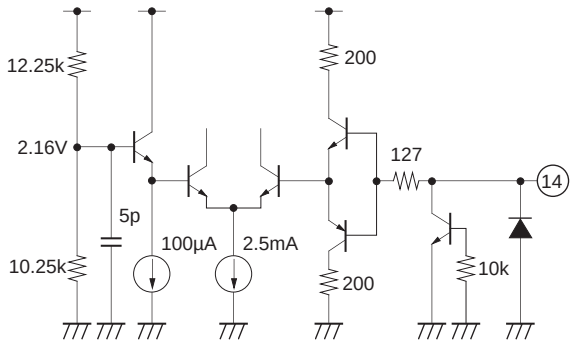
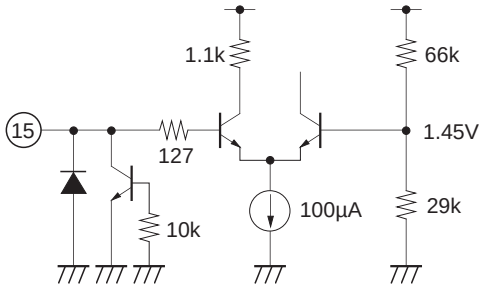
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin voltage</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr>
<td>8</td>
<td>DRVOUT</td>
<td>• Camera mode (CAM)
VRB – 200mV
< black level
< VRB + 300mV
• Composite video mode (LIN)
VRB + 100mV
• Chroma mode (CH, CL)
Center voltage =
(VRT – VRB)/2</td>
<td> 
</td>
<td>Driver output for A/D converter capable of DC coupling.

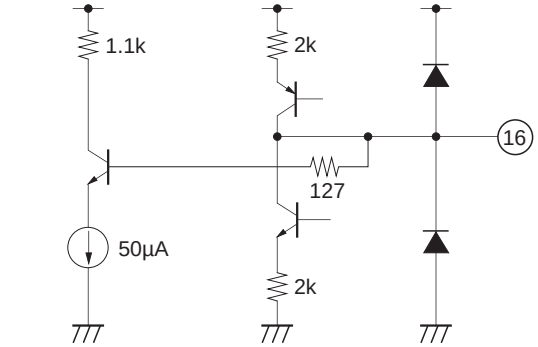
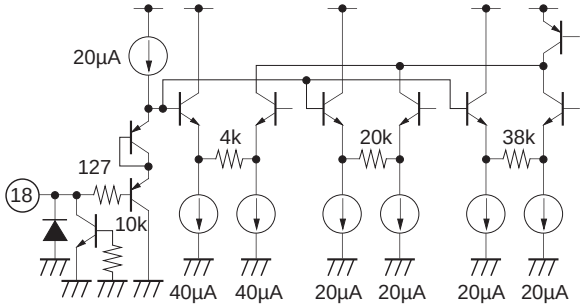
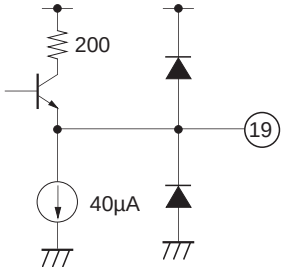
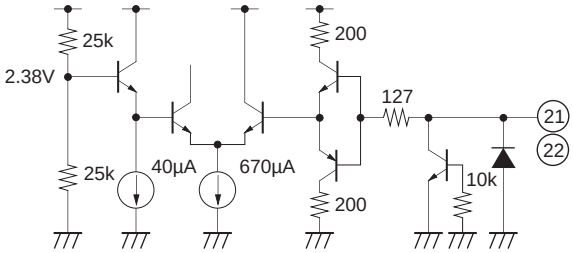
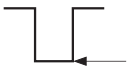
Dynamic range
= 2Vp-p

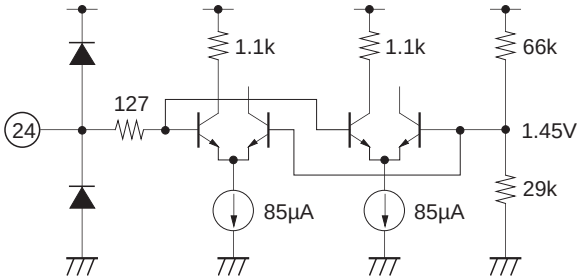
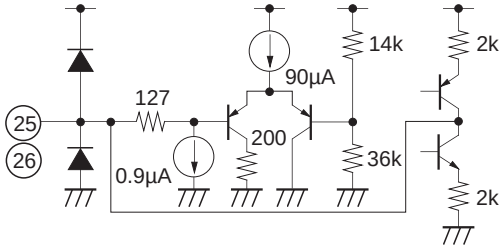
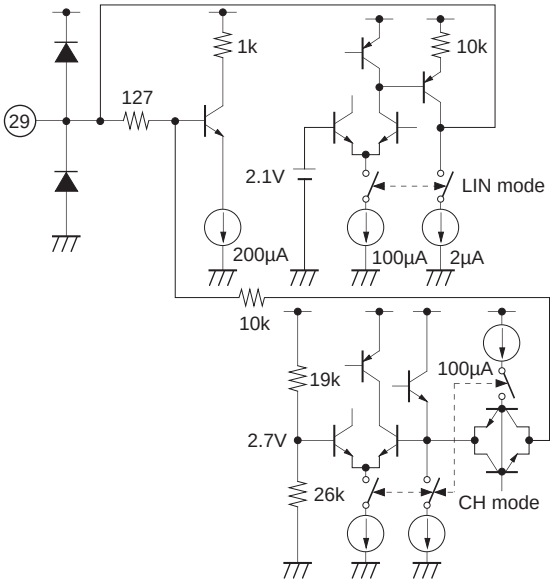
<table>
<tr><th>SW1</th><th>SW2</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>CH, CL</td></tr>
<tr><td>0</td><td>1</td><td>CAM</td></tr>
<tr><td>1</td><td>0</td><td>LIN</td></tr>
<tr><td>1</td><td>1</td><td>—</td></tr>
</table>
0: Closed
1: Open</td>
</tr>
<tr>
<td>9
20
27</td>
<td>Vcc3
Vcc1
Vcc2</td>
<td>Vcc</td>
<td></td>
<td>Power supply.</td>
</tr>
<tr>
<td>10</td>
<td>VRB</td>
<td>2.0V</td>
<td> 
</td>
<td>2V regulator output.

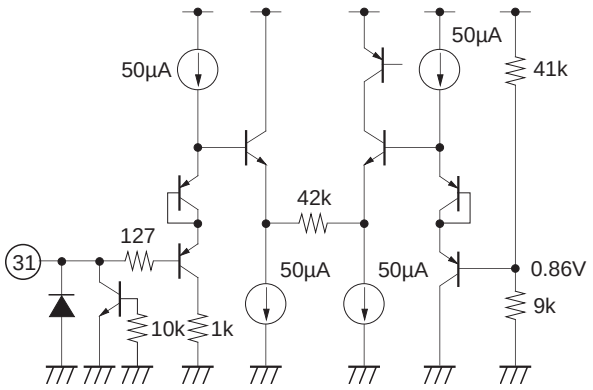
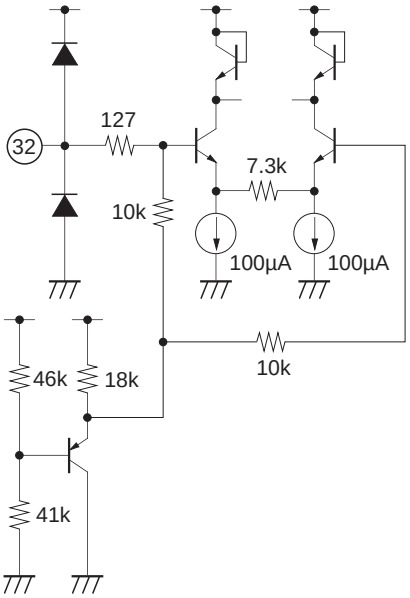
Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used.
(Recommended capacitor value: 4.7µF)</td>
</tr>
<tr>
<td>11</td>
<td>VRT</td>
<td>4.0V</td>
<td> 
</td>
<td>4V regulator output.

Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used.
(Recommended capacitor value: 4.7µF)</td>
</tr>
</table>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	OFFSET	0 to 3V		Controls the output offset during camera mode. When 0V: less than (VRB – 200mV) When 3.0V: greater than (VRB + 300mV)
13	PBLK	VTH = 1.35V  Active: Low		Camera signal pre-blanking pulse input. Active when Low only during camera mode. Calibrates the black level of the AGC output waveform. When PBLK is Low, the DRVOUT potential is forced to 2V.
14	XRS	VTH = 2.16V  Sampling		Camera signal sample-and-hold pulse input.
15	CLPOB	VTH = 1.45V  Active: Low		Clamp pulse used to clamp the optical black portion of the camera signal after it passes through the AGC amplifier.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	AGCCLP	Approx. 3V		AGC clamp capacitor. (Recommended value: 0.1µF)
18	AGCCONT	0 to 3.0V		AGC gain control. When 0V: 8dB (Minimum gain) When 3.0V: 38dB (Maximum gain)
19	CCDLEVEL	DIN input CCD signal black level: approx. 2.7V		Enables monitoring of the SHD output camera signal.
21	SHP	VTH = 2.38V		Preset level sample-and-hold pulse input.
22	SHD			Data level sample-and-hold pulse input.

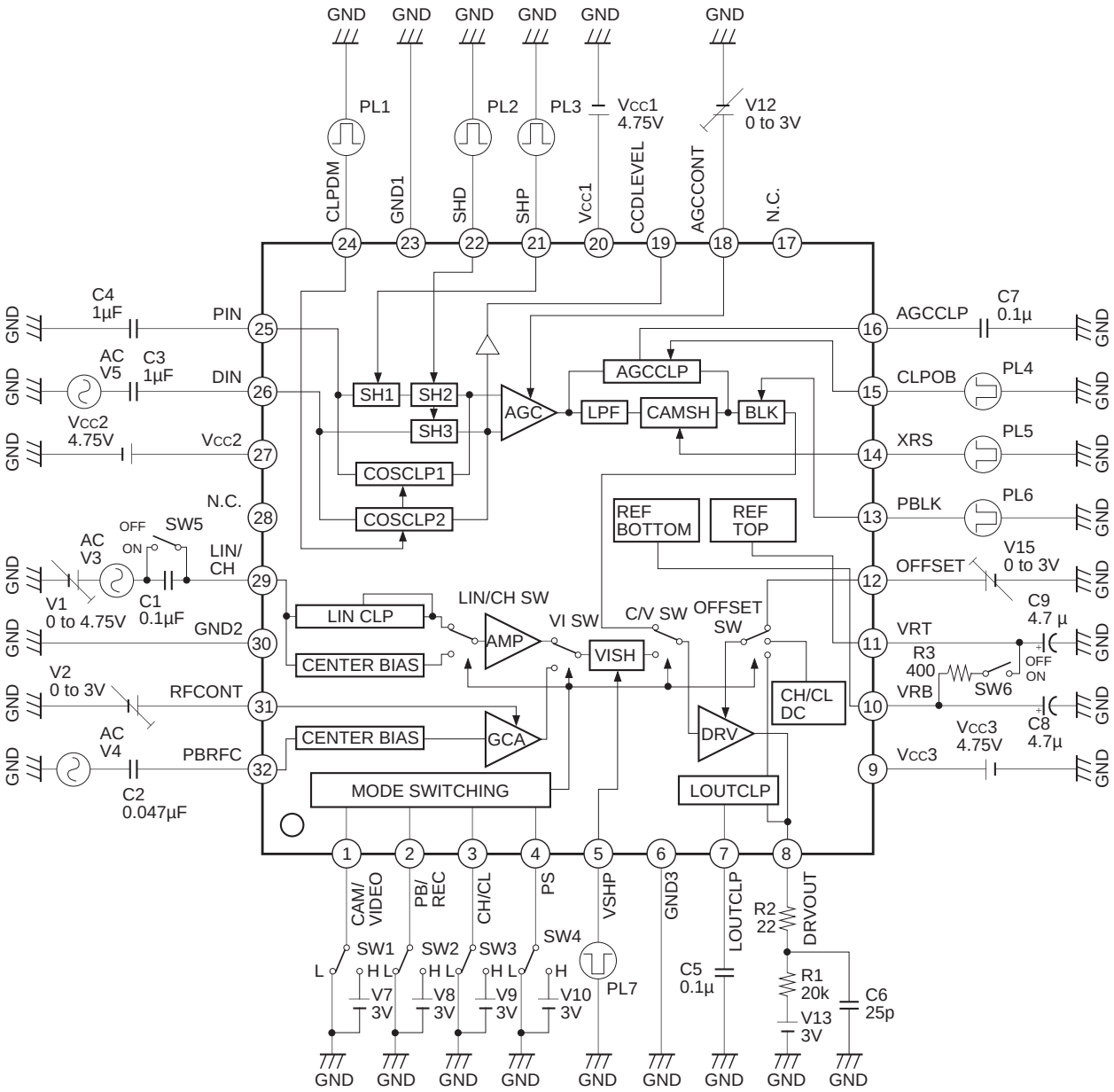
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	CLPDM	VTH = 1.45V  Active: Low		Clamp pulse used to clamp the dummy pixel portion of the input CCD signal.
25 26	PIN DIN	Black level: approx. 2.7V		CCD signal input.
29	LIN/CH	Clamp potential during LIN mode: approx. 2.4V During CH mode: approx. 2.7V		Common input for the composite video signal (LIN) and high-band chroma signal (CH).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31	RFCONT	0 to 3.0V		Gain control for the low-band chroma signal (CL). When 0V: 3.5dB (Minimum gain) When 3.0V: 15.5dB (Maximum gain)
32	PBRFC	Approx. 2.94V		Low-band chroma signal (CL) input.

Electrical Characteristics (Ta = 25°C, V_{CC}1, 2 and 3 = 4.5V, V_{CC}4 = OPEN)

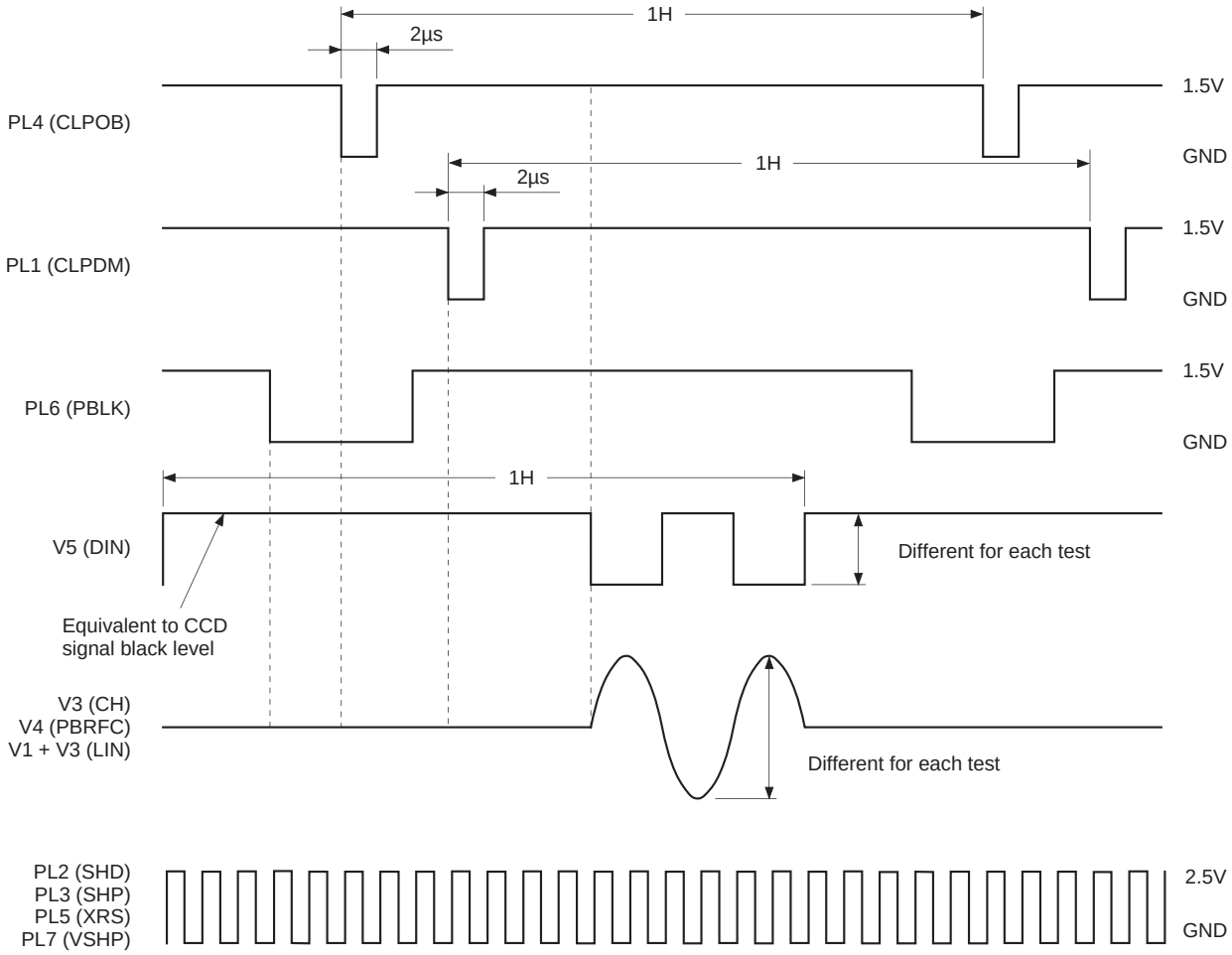
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Camera mode	I_{DC}	AGCCONT = 0V, open between V_{RT} and V_{RB} CAM/VIDEO = 3V, PB/REC = 0V, CH/CL = 0V, PS = 3V	31	46	60	mA
	LINE mode	I_{DL}	Open between V_{RT} and V_{RB} CAM/VIDEO = 0V, PB/REC = 0V, CH/CL = 0V, PS = 3V	19	27	36	
	CH mode	I_{DCH}	Open between V_{RT} and V_{RB} CAM/VIDEO = 0V, PB/REC = 3V, CH/CL = 3V, PS = 3V	17	26	35	
	CL mode	I_{PCL}	RFCONT = 0V, open between V_{RT} and V_{RB} CAM/VIDEO = 0V, PB/REC = 3V, CH/CL = 0V, PS = 3V	16	24	33	
	PS mode	I_{DP}	PS = 0V	6	10	13	
AGC	Maximum gain	A CONT max.	DIN = 1µs, 10mVp-p pulse AGCCONT = 3V	36	38	40	dB
	Minimum gain	A CONT min.	DIN = 1µs, 600mVp-p pulse AGCCONT = 0V	—	8	10	
	Range of gain variance	AGC G	A CON max. – A CON min.	28	30	32	
	Dynamic range maximum	AGCmax. D	AGCCONT = 3V CLPOUT output signal at saturation level	1.9	2.1	2.5	V
	Dynamic range minimum	AGCmin. D	AGCCONT = 0V CLPOUT output signal at saturation level	1.9	2.1	2.5	
DRV	Offset high	CAOF high	V_{CC}1, 2, 3 = 4.75V, OFFSET = 3V camera mode	560	660	—	mV
	Offset low	CAOF low	V_{CC}1, 2, 3 = 4.75V, OFFSET = 0V camera mode	—	–270	–200	
REF	V_{RT} DC level	VRTO	V_{CC}1, 2, 3 = 4.75V with a 400Ω load	3.97	4	4.03	V
	V_{RB} DC level	VRBO	V_{CC}1, 2, 3 = 4.75V with a 400Ω load	1.9	2	2.1	
	$V_{RT} – V_{RB}$	ΔVR	V_{CC}1, 2, 3 = 4.75V with a 400Ω load	1.9	2	2.1	
BLK	Offset	BLKOF	BLKOF (PBLK = 3V) – BLKOF (PBLK = 0V)	–5	8.5	15	mV
AMP	LIN mode gain	LIN G	LIN/CH = 3MHz, 500mVp-p, sine wave + offset voltage	8.5	9.5	10.5	dB
	CH mode gain	CH G	LIN/CH = 3MHz, 500mVp-p, sine wave	8.1	9.1	10.1	
GCA	CL mode maximum gain	RF CONmax.	RFCONT = 3V 15kHz 80mVp-p sine wave	16	20.5	—	
	CL mode minimum gain	RF CONmin.	RFCONT = 0V 15kHz 400mVp-p sine wave	—	0.4	2	

Electrical Characteristics Measurement Circuit

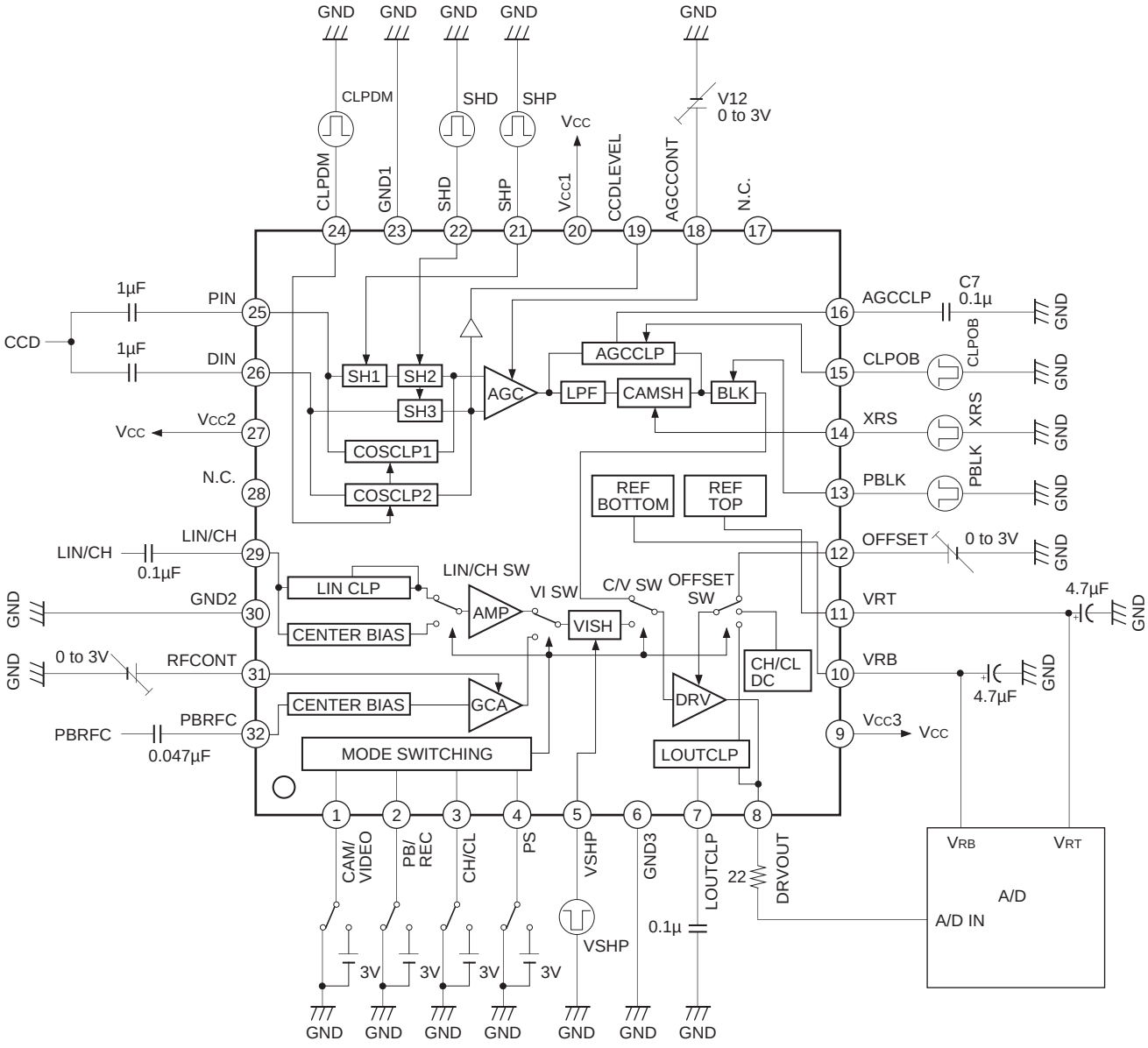


SW1	SW2	SW3	SW5	SW4	MODE
L	L	H	OFF	H	CAM
H	L	L			
H	L	H	ON		LIN
L	L	L			
H	H	L	OFF		CL
L	H	L			
L	H	H			CH
				L	POWER SAVE

Measurement Timing Chart



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Camera signal processing system

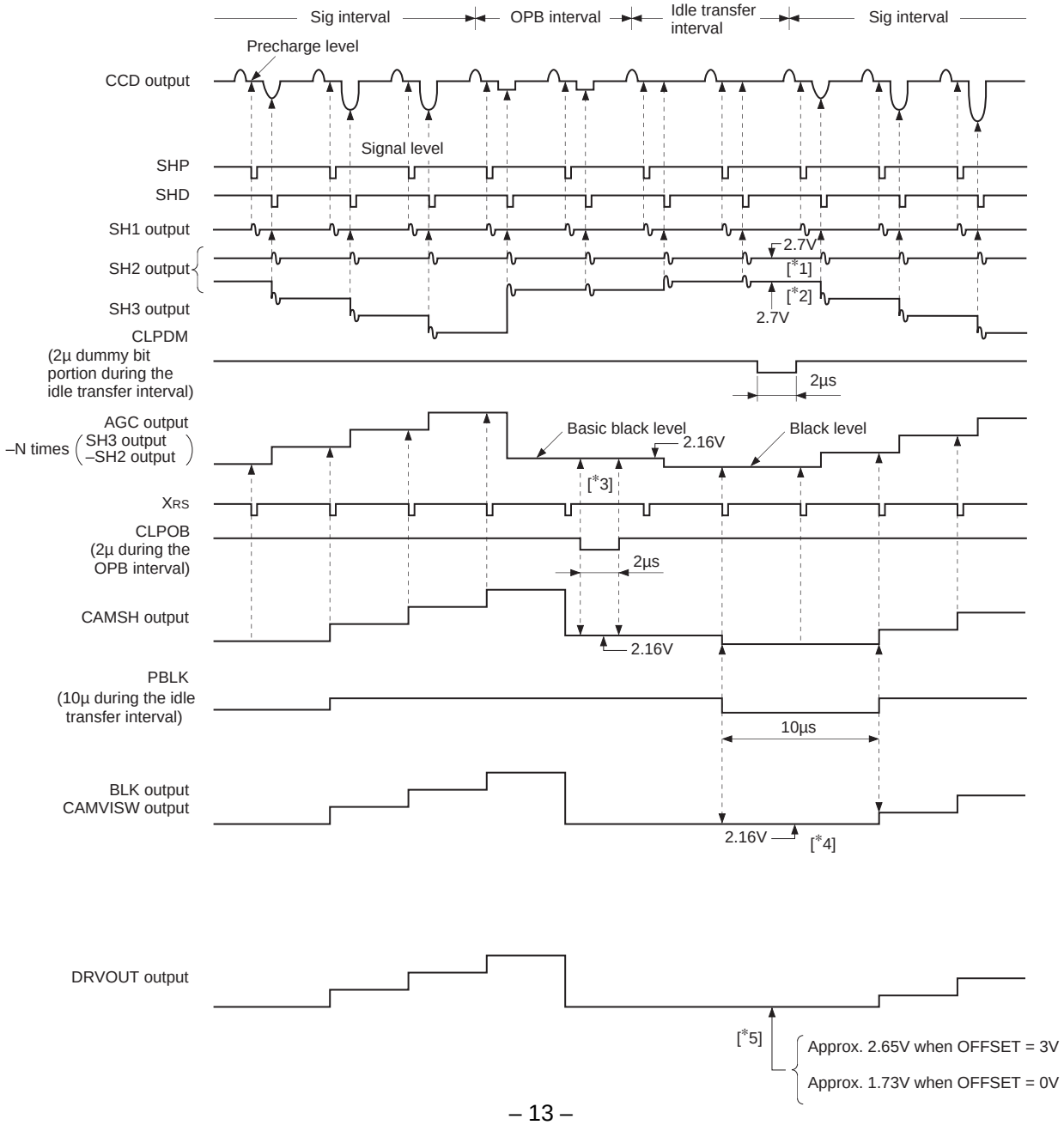
Process the video signal processing pins as follows only in camera mode.

<5> VSHP ... Connect to GND.
<7> LOUTCLP ... Connect to GND.
<29> LIN/CH ... Connect to GND.
<31> RFCONT ... Connect to GND.
<32> PBRFC ... Connect to GND via the capacitor (approx. 0.01µF).

Operating conditions

The camera signal processing system operates when PS is high, CAM/VIDEO is low, PB/REC is low and CH/CL is high, or when PS is high, CAM/VIDEO is high, PB/REC is low and CH/CL is low.

Camera signal processing system timing chart (when V_{CC} = 4.75V)



CDS:
The CCD signal from the CCD image sensor is input to PIN and DIN where correlated double sampling (CDS) is performed by SH1, SH2 and SH3. The precharge level of the CCD output signal is sampled, held and output by the SH2 output, and the signal level is sampled, held and output by the SH3 output.

CDSCLP:
The CDSCLP stabilizes the input signal DC level, clamps (CLPDM) the input signal during the idle transfer interval for the purpose of eliminating the AGC input offset, and synchronizes the DC level ([*1], [*2]) of SH2 and SH3.

AGC:
The gain can be varied from 8 to 38dB by adjusting the AGCCONT voltage control $V_{AGCCONT}$ from 0 to 3V.

LPF:
A primary low-pass filter is installed for the purpose of eliminating unused bands and white noise and improving S/N.

CAMSH:
The CAMSH is used for camera signal processing system. It is a sample-and-hold circuit which synchronizes the data read-in timing for the external A/D.

AGCCLP:
The basic black level is set ([*3]) by clamping the AGC output waveform with the CLPOB clock during the OPB interval. The AGCCLP capacitance is connected to the AGCCLP pin.

BLK:
The black level is calibrated by blanking the black level signal of the AGC output waveform so that it does not fall below the basic black level and replacing the DC potential. ([*4])
The signal is blanked when PBLK is low.

C/VSW:
When the CAM/VIDEO, PB/REC, CH/CL and PS pin voltages are set so that the camera signal processing system operates, C/VSW conducts the BLK output (camera signal) into the DRV. In addition, when these voltages are set so that the video signal processing system operates, C/VSW conducts the VISH output (video signal) into the DRV.

OFFSET SW:
The OFFSET SW selects [OFFSET], [CH/CLDC] or [LOUTCLP] as the offset adjustment input pin of the DRV block and activates these pins by selecting the CAM/VIDEO, PB/REC, CH/CL and PS pin voltages.
When the camera signal processing system is in camera mode, the OFFSET pin is conducted [OFFSET], allowing the camera signal offset to be adjusted. ([*5])
When the video signal processing system is in LIN mode, the LOUTCLP pin is conducted [LOUTCLP], clamping the video composite signal at its sync level and offsetting the signal. In addition, CH/CL mode conducts the CH/CL DC [CH/CLDC], which gives center potential to the high-band chroma and low-band chroma signals of the video signal.

DRV:
DRV drives the external A/D. Camera and video (LIN, CH, CL modes) signals are input by switching C/VSW, and offset adjusted signals are output from DRVOUT pin.

REFBOTTOM, REFTOP:
REFBOTTOM and REFTOP are reference voltage source for the external A/D. They are connected to V_{RT} and V_{RB} of the A/D, and 2V and 4V are supplied.

MODE SWITCHING:
MODE SWITCHING is a mode selection block which selects camera signal system or video signal system operation by selecting high or low potentials for the CAM/VIDEO, PB/REC, CH/CL and PS pins. PS is the power save pin, and power save functions when this pin is low.

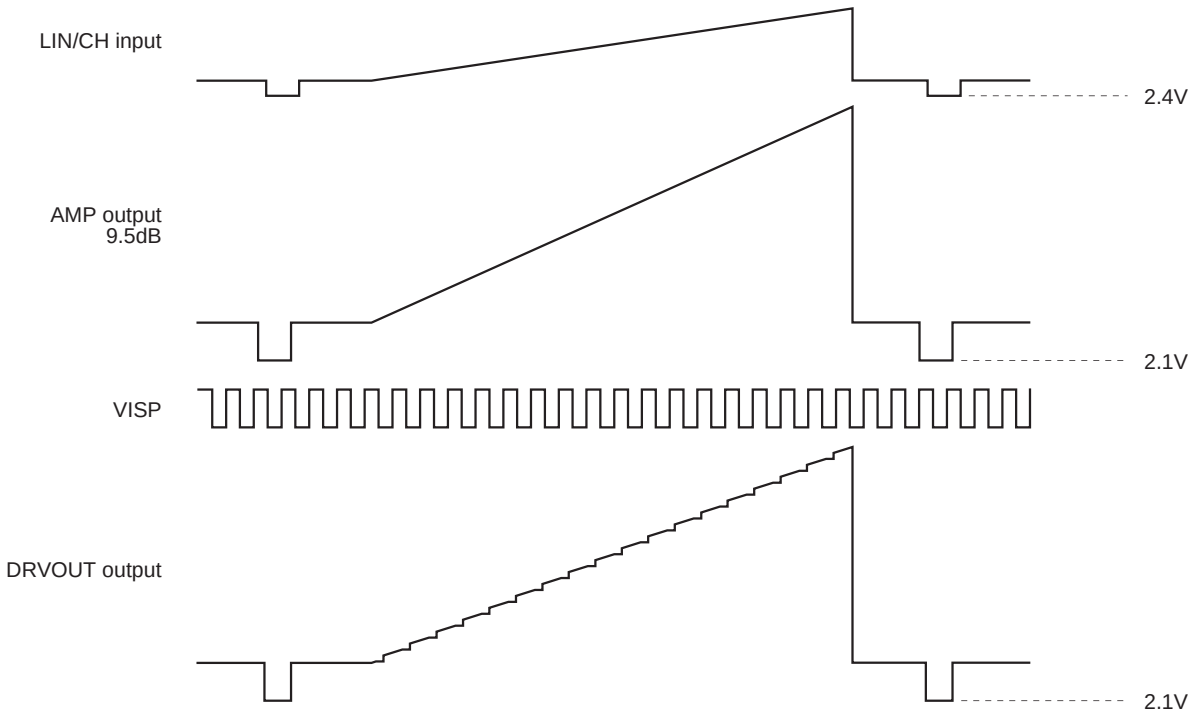
2. Video signal processing system

Operating conditions

The video signal processing system has three modes: LIN signal mode, CH signal mode and CL signal mode.
The video signal processing system operates in LIN signal mode when PS is high, CAM/VIDEO is high, PB/REC is low and CH/CL is high, or when PS is high, CAM/VIDEO is low, PB/REC is low and CH/CL is low.
The video signal processing system operates in CH signal mode when PS is high, CAM/VIDEO is low, PB/REC is high and CH/CL is high.
The video signal processing system operates in CL signal mode when PS is high, CAM/VIDEO is low, PB/REC is high and CH/CL is high, or when PS is high, CAM/VIDEO is low, PB/REC is high and CH/CL is high.

Video signal processing system timing chart

LIN mode



LIN signal mode

LINCLP:
The video composite signal is input to LIN/CH pin. LINCLP expands the input dynamic range, and sync tip clamps the input signal at 2.4V to allow full input. The input level and frequency are respectively 571mVp-p (Max.) and DC is up to 7MHz.

LINAMP:
This is a fixed gain amplifier with a gain of 9.5dB.

LIN/CHSW:
LIN/CHSW switches between the LIN signal and CH (high-band chroma) signal. The signals are switched according to the mode selection.

VISH:
The VISH is used for video signal processing system.
It is a sample-and-hold circuit which synchronizes the data read-in timing for the external A/D.

VISW:
VISW switches between the LIN, CH and CL low-band chroma signals for the video signal processing system. The signals are switched according to the mode selection.

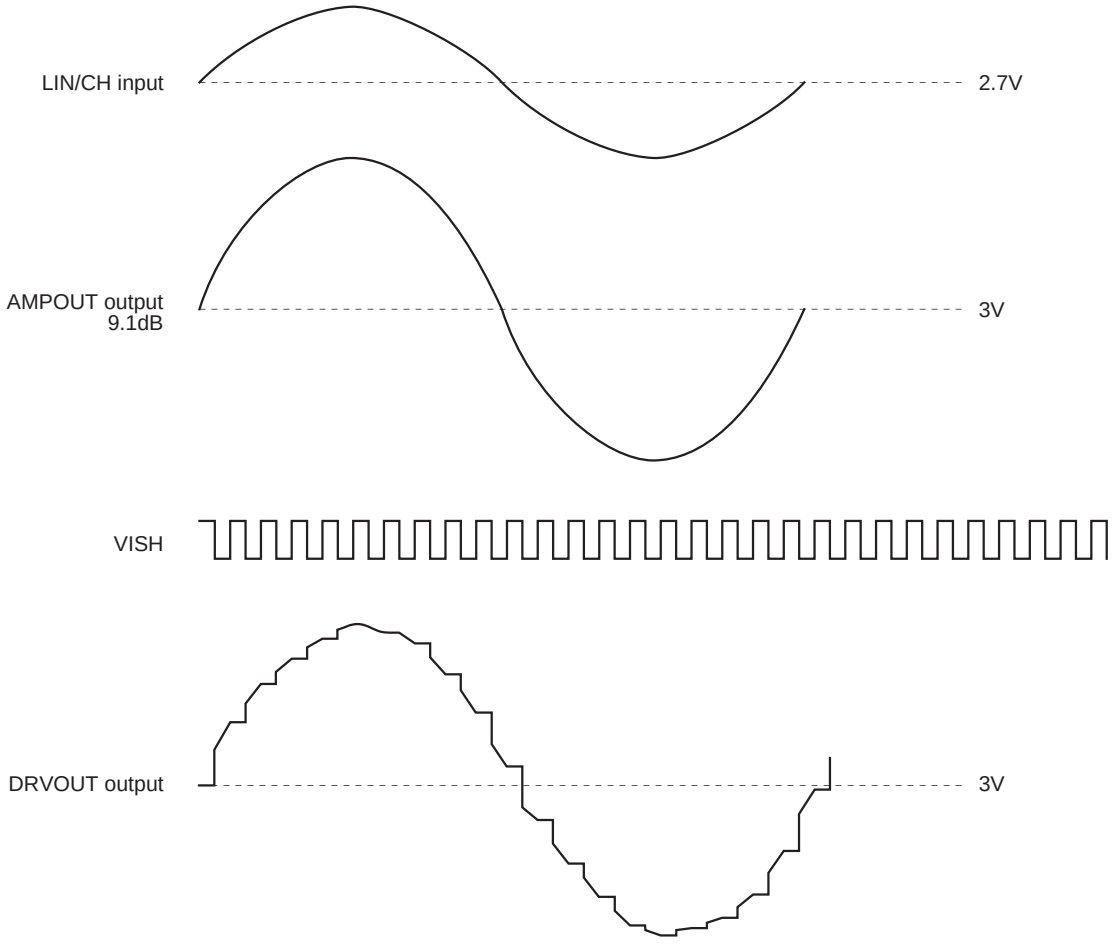
LOUTCLP:
LOUTCLP is a clamp circuit which operates when the LIN signal is output to the DRV. The clamp potential is the sync portion, and is 2.1V.

CH (high-band chroma) signal mode

CENTER BIAS:
The video high-band chroma signal is input to LIN/CH pin. CENTER BIAS expands the input dynamic range and sets a center DC bias so that the center potential of the SIN signal is 2.7V to allow full input. The input level and frequency are respectively 470mVp-p (Max.) and from 1 to 7MHz.

CH/CL DC:
CH/CL DC is a DC bias circuit which operates when the CH signal is output to the DRV. The DC bias potential is 3V.

CH mode



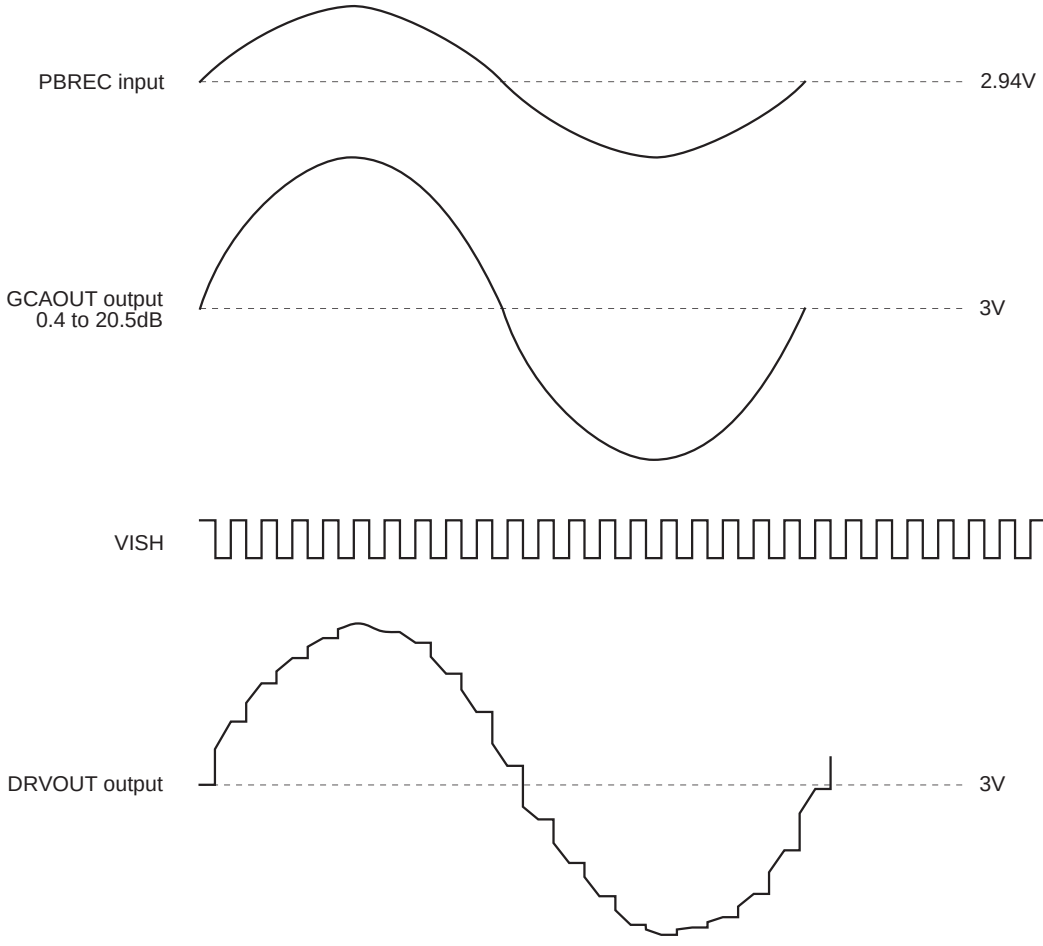
CL (low-band chroma) signal mode

CENTER BIAS:
The video low-band chroma signal is input to PBRFC pin. CENTER BIAS expands the input dynamic range and sets a center DC bias so that the center potential of the SIN signal is 2.94V to allow full input. The input level and frequency are respectively 1490mVp-p (Max.) and DC is up to 1.5MHz.

GCA:
The GCA amplifier controls the gain of the CL signal input to PBRFC. The gain can be varied from 0.4 to 20.5dB by adjusting the RFCONT voltage from 0 to 3V.

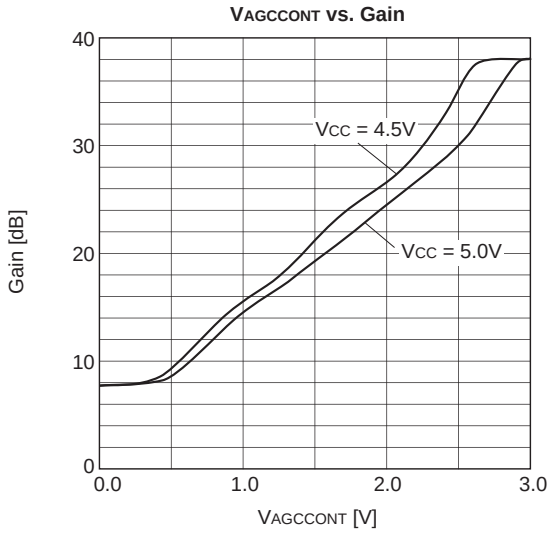
CH/CL DC:
CH/CL DC is a DC bias circuit which operates when the CL signal is output to the DRV. The DC bias potential is 3V.

CL mode

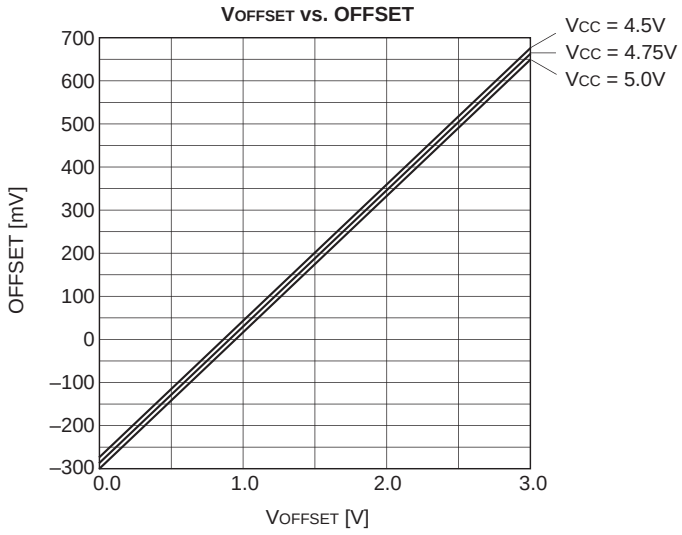


Example of Representative Characteristics

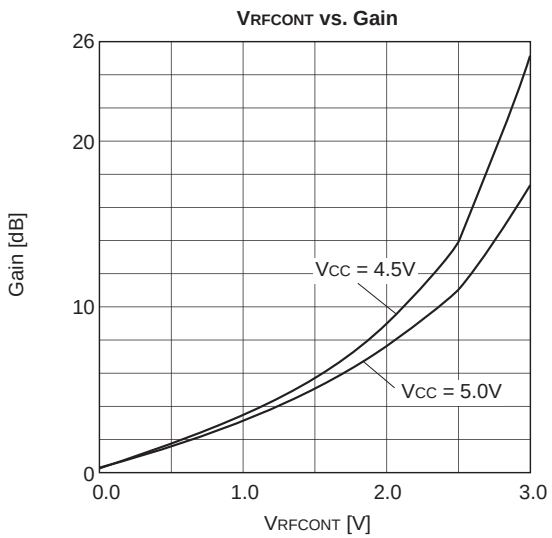
CAM mode AGCCONT control supply voltage characteristics



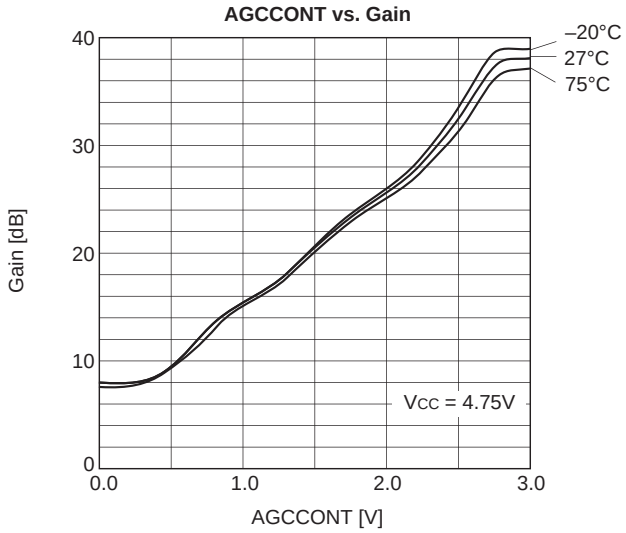
CAM mode OFFSET control supply voltage characteristics



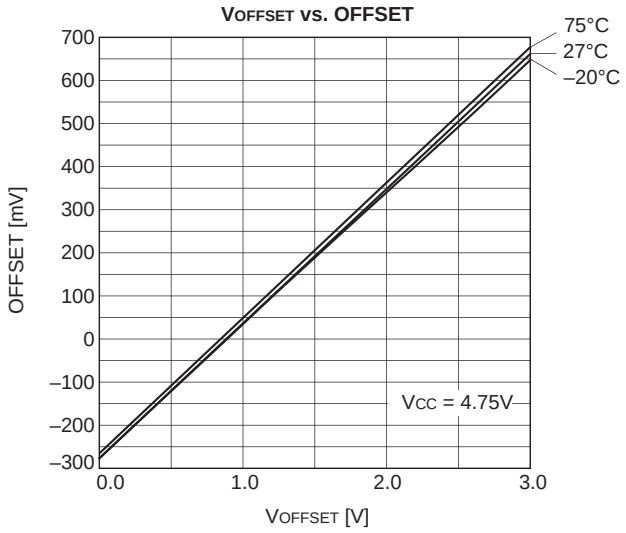
CL mode RFGCA gain control supply voltage characteristics



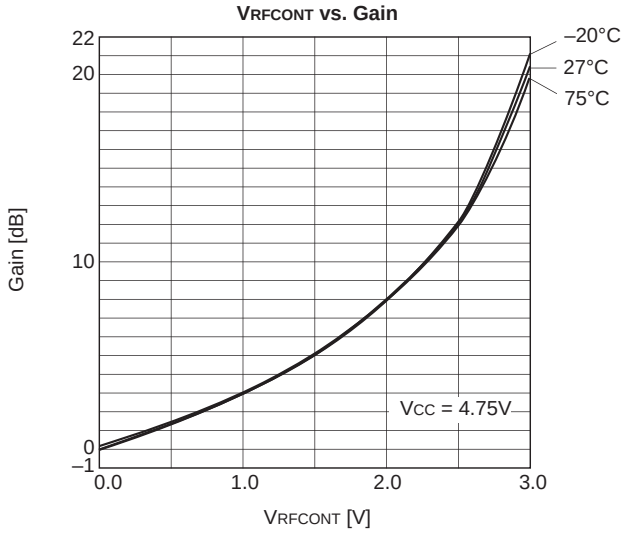
CAM mode AGCCONT control temperature characteristics (V_{CC} = 4.75V)



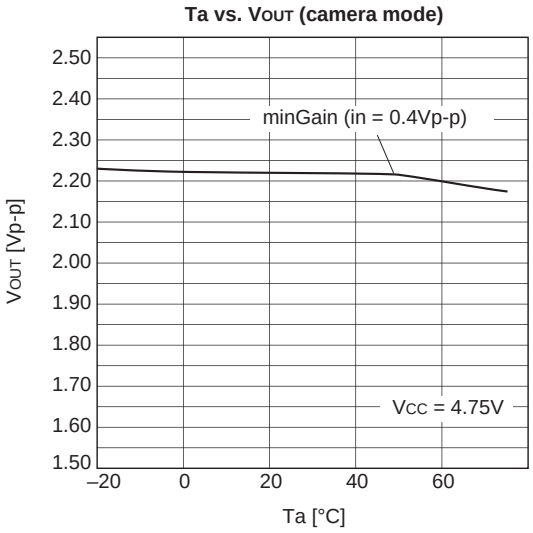
CAM mode OFFSET control temperature characteristics



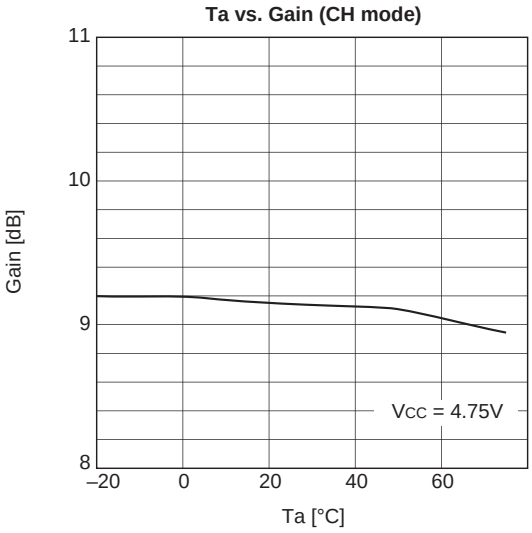
CL mode RFGCA gain control temperature characteristics



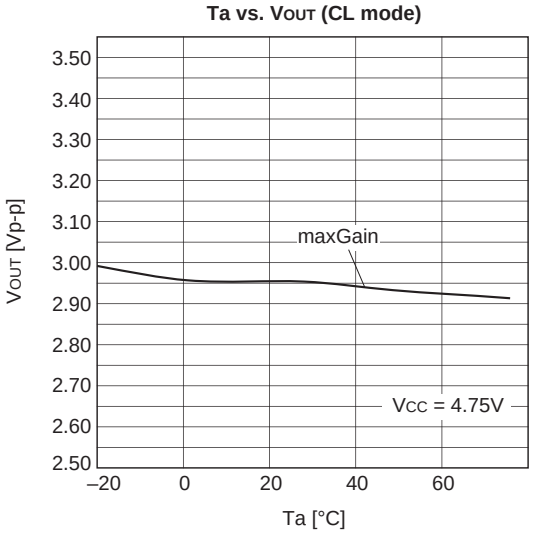
CAM mode maximum signal amplitude temperature characteristics



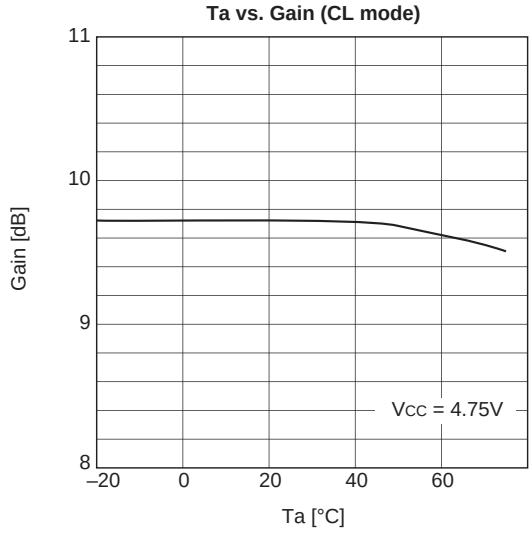
CH mode AMP gain temperature characteristics



CL mode maximum signal amplitude temperature characteristics

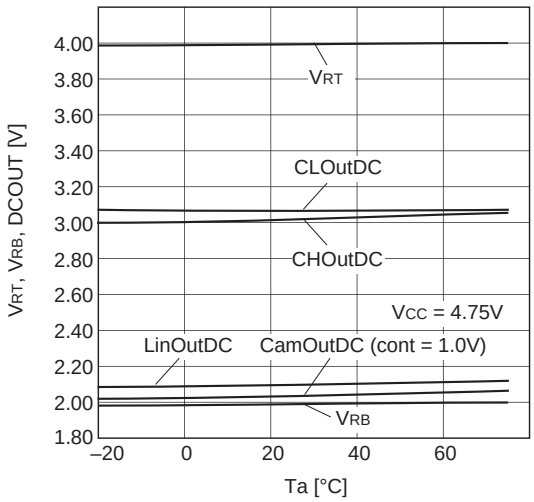


LIN mode AMP gain temperature characteristics



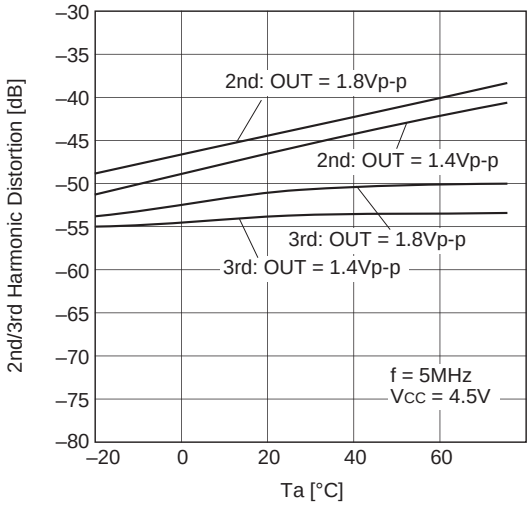
V_{RT}, V_{RB} and output DC (CAM, LIN, CH and CL modes) temperature characteristics

Ta vs. V_{RT}, V_{RB}, DCOUT



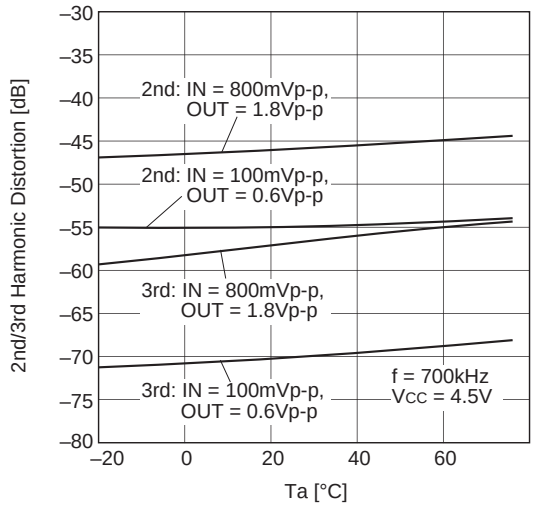
CH mode 2nd/3rd harmonic distortion temperature characteristics

Ta vs. 2nd /3rd harmonic distortion



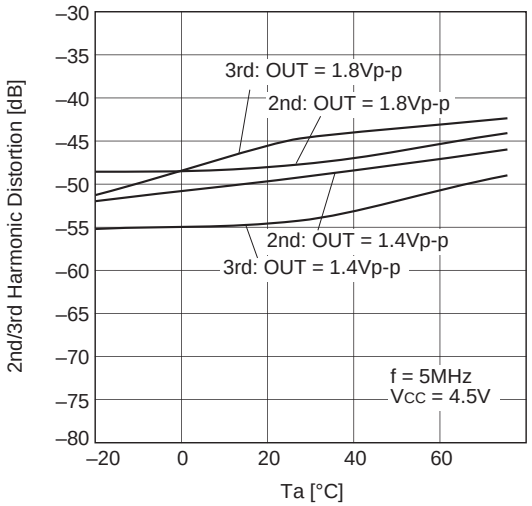
CL mode 2nd/3rd harmonic distortion temperature characteristics

Ta vs. 2nd/3rd harmonic distortion



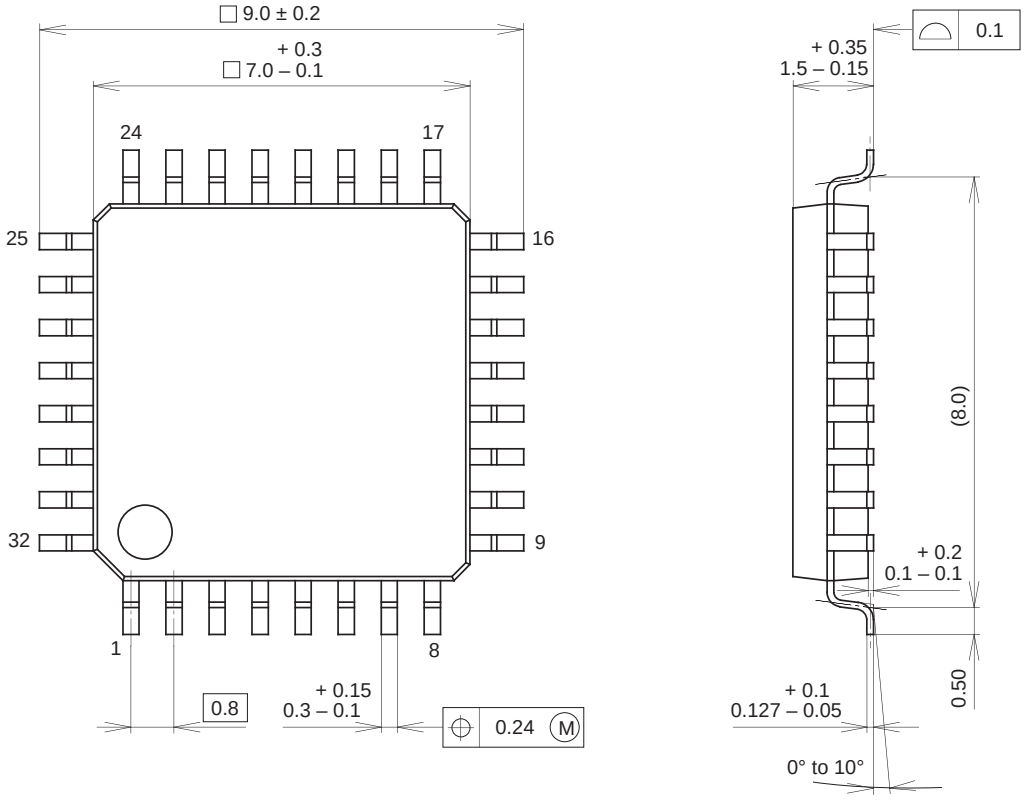
LIN mode 2nd/3rd harmonic distortion temperature characteristics

Ta vs. 2nd/3rd harmonic distortion



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g