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SONY

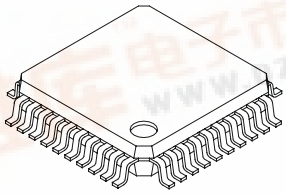
CXA2019AQ

NTSC/PAL Chroma Decoder

Description

The CXA2019AQ is a bipolar IC which integrates the luminance signal processing, chroma signal processing, and sync signal processing functions for NTSC/PAL system color TVs onto a single chip.

40 pin QFP (Plastic)



Features

- Sub picture bright and white balance can be adjusted by using the main picture Y/C/J BGP output as the timing pulse
- I^2C BUS compatible; two bus lines (SCL, SDA) allow various adjustments and user controls
- Countdown system eliminates need for H and V oscillator frequency adjustment
- Non-adjusting Y system filters (chroma trap, delay line)
- Automatic identification of color system (forced control possible)
- Automatic identification of 50/60Hz vertical frequency (forced control possible)
- Built-in delay line aperture correction
- Built-in dynamic picture (black expansion) function
- Combination with a non-adjusting SECAM chroma decoder allows configuration of multiple systems

Applications

Color TVs

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

(Ta = 25°C, SGND, JGND = 0V)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.67	W

Operating Conditions

Supply voltage	V_{CC}	9 ± 0.5	V

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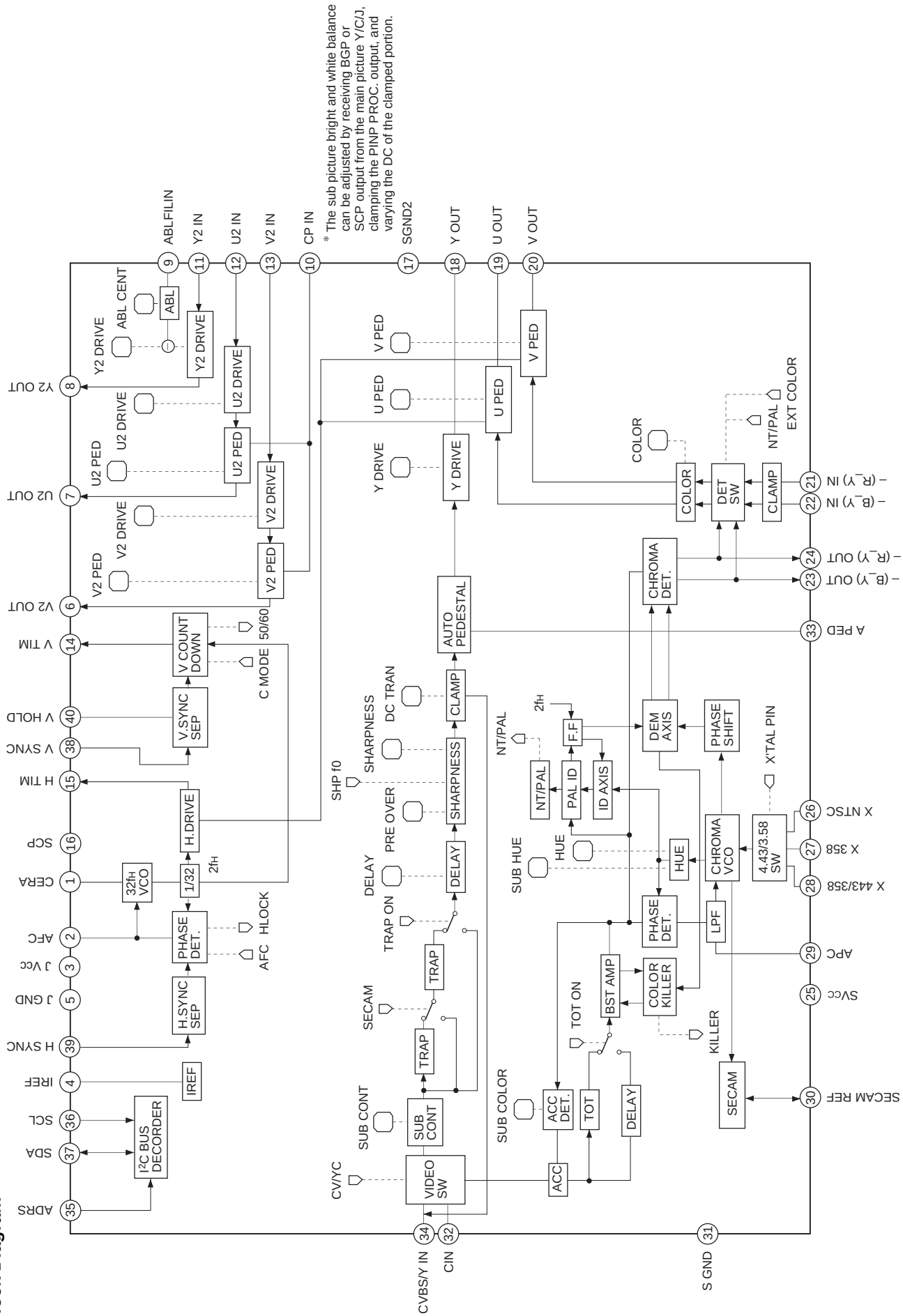
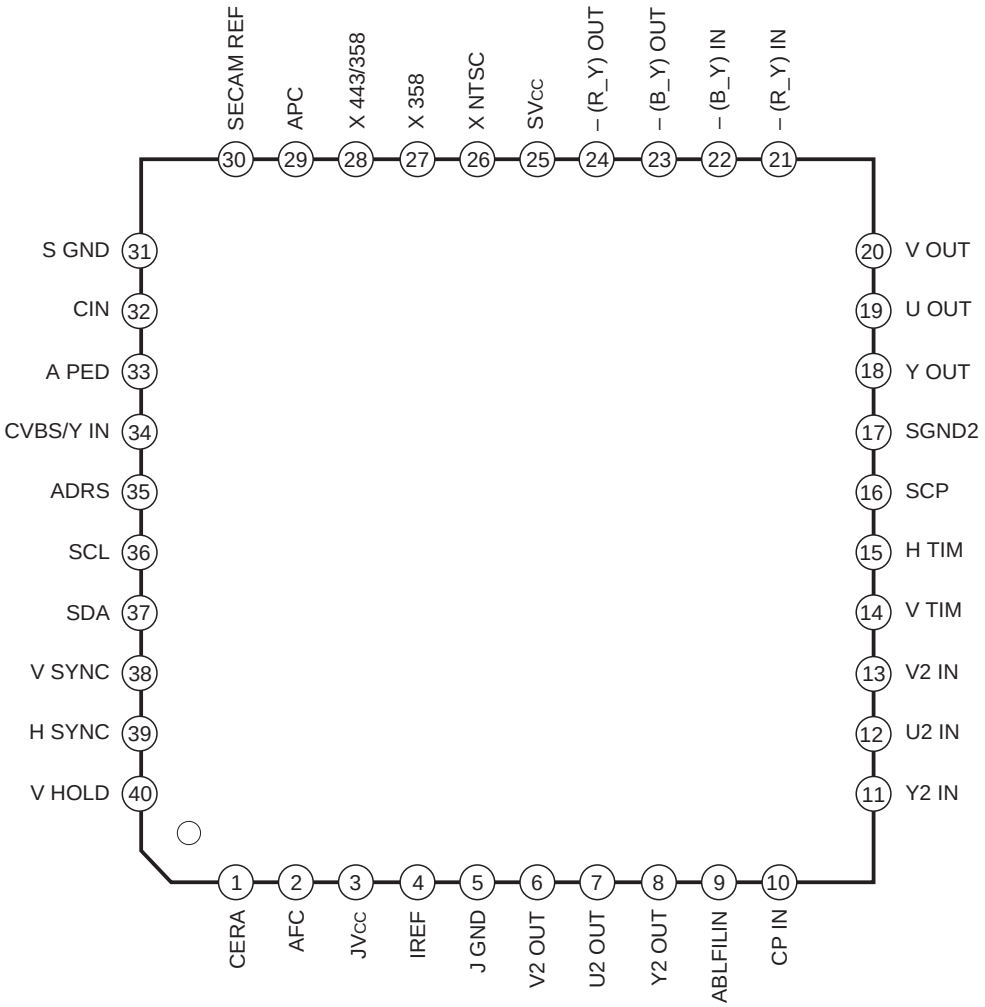
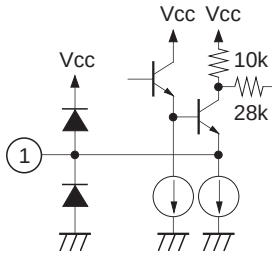
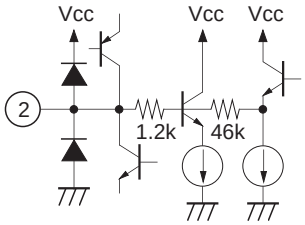
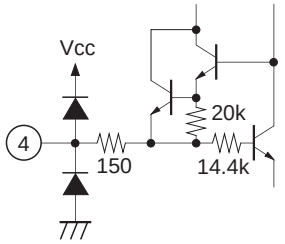
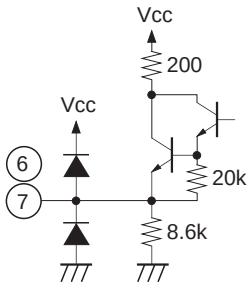
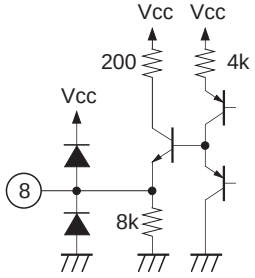
Block Diagram

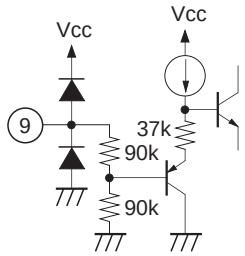
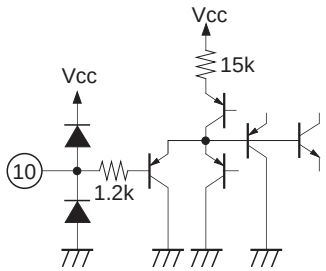
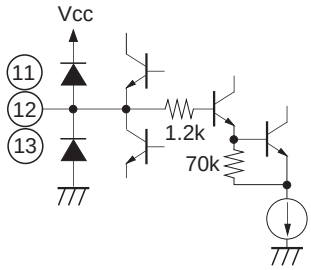
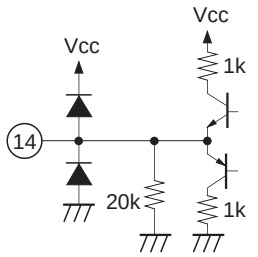
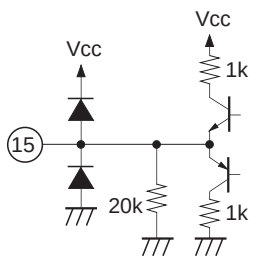


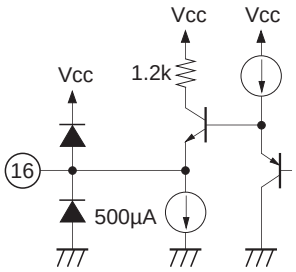
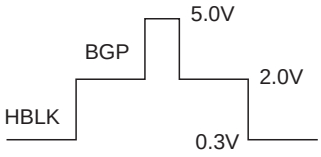
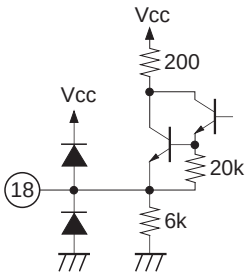
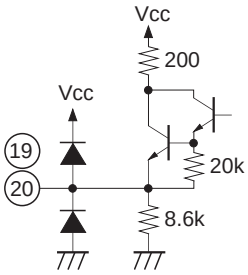
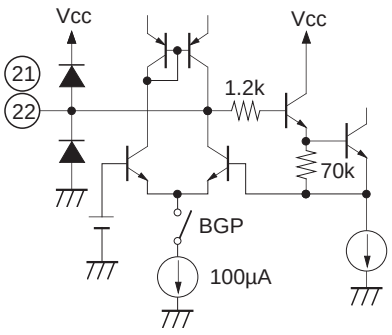
Pin Configuration

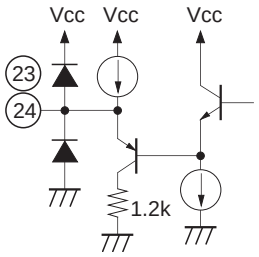
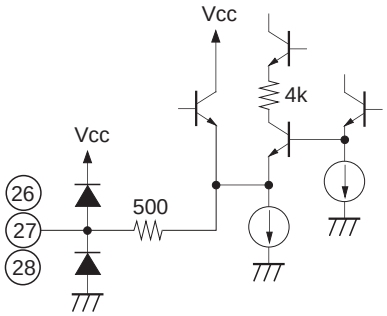
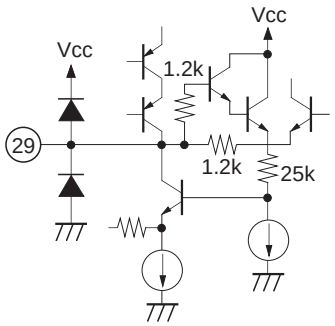
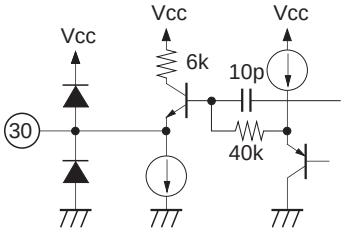


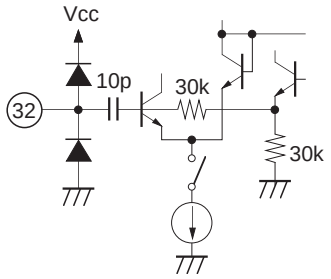
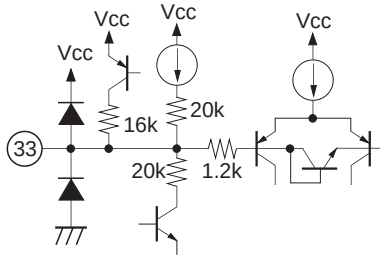
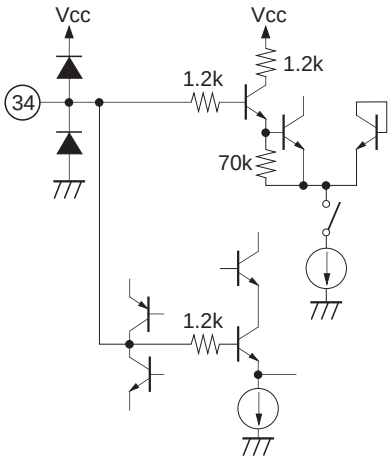
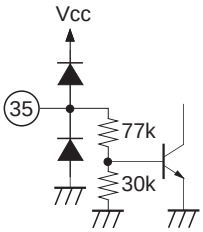
Pin Description

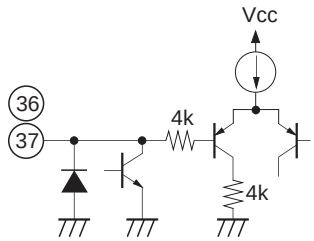
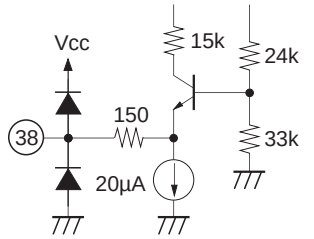
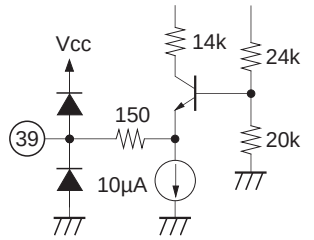
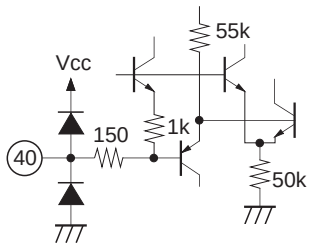
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	CERA	—		32f_H (500 or 503.5kHz) ceramic oscillator connection.
2	AFC	—		CR connection for AFC lag-lead filter.
3	JVcc	9.0V		Power supply.
4	IREF	1.8V		Connect a 10kΩ resistor between this pin and GND.
5	J GND	—		Jungle system (H/V) GND.
6 7	V2 OUT U2 OUT	3V		Reinput system outputs.
8	Y2 OUT	3V		Reinput system output.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	ABLFILIN	—		ABLFIL voltage input. Input the main picture Y/C/J ABLFIL voltage.
10	CP IN	—		Reinput system clamp pulse input. Input the main picture BGP (SCP). Vth: 2.5V
11 12 13	Y2 IN U2 IN V2 IN	4V		Reinput system inputs. Input via a capacitor.
14	V TIM	—		V timing pulse output. Outputs a 0 to 5V positive polarity pulse.
15	H TIM	—		H timing pulse output. Outputs a 0 to 5V positive polarity pulse.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	SCP	—		Outputs BGP and HBLK as SCP (sand castle pulse). The typ. waveform is as follows. 
17	SGND2	—		GND.
18	Y OUT	3V		Y (luminance signal) output. Standard output level: 1.1Vp-p
19 20	U OUT V OUT	3V		U/V (color difference signal) outputs. Output level: U = V = 1.2Vp-p (In case of setting data as shown in "I²C BUS Register Initial Settings.")
21 22	– (R_Y) IN – (B_Y) IN	5.6V		Color difference signal inputs. Input as negative polarity via a capacitor. Standard input levels: B-Y: 1.33Vp-p R-Y: 1.05Vp-p

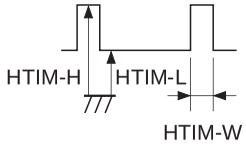
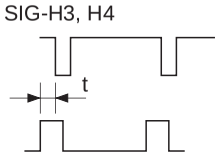
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
23 24	– (B_Y) OUT – (R_Y) OUT	5.6V		Color difference signal outputs. Output as negative polarity. Standard output levels: B-Y: 0.665Vp-p R-Y: 0.525Vp-p
25	SVcc	9.0V		Power supply.
26 27 28	X NTSC X 358 X443/358	—		Crystal oscillator connections. Connect the PALN and 4.43MHz crystal to Pin 28. Connect the PALM crystal to Pin 27, and the NTSC crystal to Pin 26.
29	APC	—		CR connection for APC lag-lead filter.
30	SECAM REF	1.5V		When the IC is set to SECAM identification mode, the 4.43MHz VCO oscillator waveform is output from this pin centering on DC 1.5V. If a 150µA current is led from this pin during this identification mode, the IC is set to SECAM mode. In SECAM mode, the 4.43MHz VCO oscillator waveform is output centering on DC = 5V only during the VBLK interval.
31	S GND	—		GND.

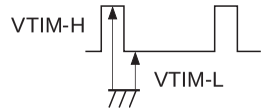
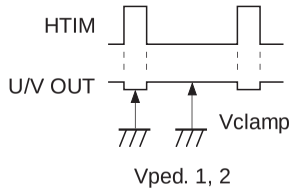
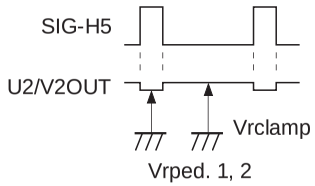
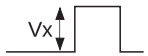
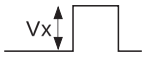
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
32	C IN	—		Chroma signal input. Standard input level (burst level) : 570mVp-p
33	A PED	—		Black peak hold for auto pedestal (black expansion). Connect a capacitor.
34	CVBS/Y IN	—		Y signal input. Input via a capacitor. Standard input level: 2Vp-p
35	ADRS	—		This pin is used to switch the slave address. Vcc: 9AH GND: 9EH Vth = 2.5 V

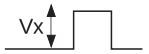
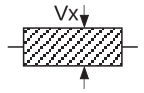
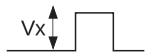
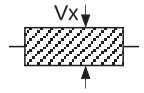
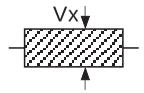
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
36 37	SCL SDA	—		I²C BUS SCL (Serial Clock) and SDA (Serial Data). Vilmax = 1.5V Vihmin = 3V Volmax = 0.4V
38	V SYNC	3.5V		V sync separation input. Input a 2Vp-p video signal via a capacitor and resistor.
39	H SYNC	2.5V		H sync separation input. Input a 2Vp-p video signal via a capacitor and resistor.
40	V HOLD	—		Peak hold for V sync separation. Connect a capacitor.

Electrical Characteristics

Setting conditions • Ta = 25°C, SV_{CC} = JV_{CC} = 9V
• Measures the following after setting the I^2C bus register as shown in "I^2C BUS Register Initial Settings".

No.	Item	Symbol	Measurement conditions	Measure-ment pins	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}	SV_{CC} = JV_{CC} = 9V	3, 25	Measure the pin inflow current.	46	68	94	mA
H system items									
2	Horizontal free-running frequency	f_H		15	HTIM output frequency	15.50	15.65	15.85	kHz
3	Horizontal sync pull-in range	Δf_H	AFC: 0	15	Confirm that I^2C bus register HLOCK is 1 (the pull-in range when f_H is shifted from 15.734kHz).	–400		400	Hz
4	HTIM output pulse width	HTIM-W		15		9.3	9.9	10.4	µs
5	HTIM output high level	HTIM-H				4.5	4.85	5.1	V
6	HTIM output low level	HTIM-L				0.0	0.1	0.5	V
7	SCP BLK output pulse width	SBLK-W		16		9.6	10.5	11.2	µs
8	SCP BGP output pulse width	SBGP-W	SCP BGR: 1 SCP BGF: 1			3.2	3.8	4.3	µs
9	AFC gain 1	$\Delta t1$	AFC: 0 SYNCIN: SIG-H3/SIG-H4	15	 Δt = t (SIG-H3) – t (SIG-H4)		0.4		µs
10	AFC gain 2	$\Delta t2$	AFC: 1 SYNCIN: SIG-H3/SIG-H4				0.6		µs
11	AFC gain 3	$\Delta t3$	AFC: 2 SYNCIN: SIG-H3/SIG-H4				1.2		µs

No.	Item	Symbol	Measurement conditions	Measure-ment pins	Measurement contents	Min.	Typ.	Max.	Unit
V system items									
12	Vertical free-running frequency 1	fV1	VFREQ: 0	14	VTIM output frequency (for 60Hz mode)	55	60	65	Hz
13	VTIM output high level	VTIM-H		14		4.7	5.0	5.3	V
14	VTIM output low level	VTIM-L		14		0.0	0.2	0.5	V
15	Vertical free-running frequency 2	fV2	VFREQ: 1	14	VTIM output frequency (for 50Hz mode)	45	50	55	Hz
YUV system items									
16	U/VOUT clamp	Vc1amp		19 20		2.7	3.0	3.2	V
17	U/VOUT pedestal variation 1	Vped1	U PED: 1F V PED: 1F			5	10	16	mV
18	U/VOUT pedestal variation 2	Vped2	U PED: 0 V PED: 0			–15	–8	–4	mV
19	U2/V2OUT clamp	Vrc1amp	CP IN: SIG-H5 (Normally input when reinput system is measured)	6 7		2.7	3.0	3.2	V
20	U2/V2OUT pedestal variation 1	Vrped1	U2 PED: 1F V2 PED: 1F			32	45	57	mV
21	U2/V2OUT pedestal variation 2	Vrped2	U2 PED: 0 V2 PED: 0			–41	–27	–13	mV
22	Y2 DRIVE variable range 1	Gy2dr1	Y2 IN: SIG-Y1 Y2 DRIVE: 1F	8		2.3	2.8	3.3	dB
23	Y2 DRIVE variable range 2	Gy2dr2	Y2 IN: SIG-Y1 Y2 DRIVE: 0		$Gy2dr = 20 \log \frac{Vx\ (Y2\ DRIVE: 1F/0)}{Vx\ (Y2\ DRIVE: F)}$	–4.9	–4.0	–3.3	dB
24	U2/V2 DRIVE variation 1	Grdr1	U2/V2 IN: SIG-Y1 U2 DRIVE: 1F V2 DRIVE: 1F	6 7		2.8	3.6	4.4	dB
25	U2/V2 DRIVE variation 2	Grdr2	U2/V2 IN: SIG-Y1 U2 DRIVE: 0 V2 DRIVE: 0		$Grdr = 20 \log \frac{Vx\ (U2/V2\ DRIVE: 1F/0)}{Vx\ (U2/V2\ DRIVE: F)}$	–8.0	–6.3	–4.5	dB

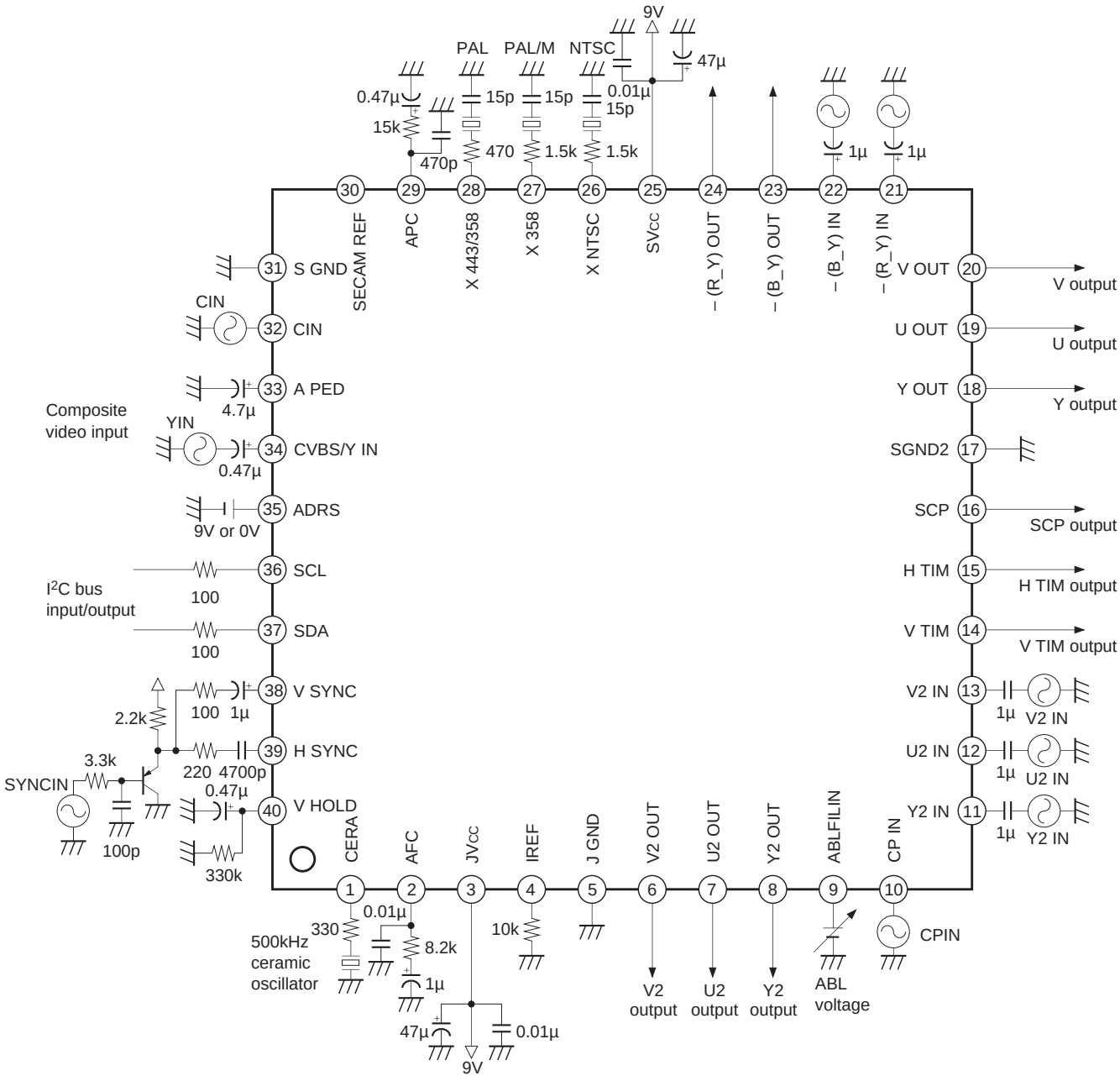
No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
Y system items									
26	Y OUT output amplitude	Vyout	Y IN: SIG-Y2 Y DRIVE: F	18	 Vyout = Vx (Y DRIVE: F)	0.9	1.1	1.3	V
27	Y DRIVE variable range 1	Gydr1	Y IN: SIG-Y2 Y DRIVE: 1F			2.8	3.5	4.2	dB
28	Y DRIVE variable range 2	Gydr2	Y IN: SIG-Y2 Y DRIVE: 0		$Gydr1, 2 = 20 \log \frac{Vx\ (Y\ DRIVE: 1F/0)}{Vx\ (Y\ DRIVE: F)}$	–6.9	–6.3	–5.7	dB
29	SHARPNESS center	Gshr	Y IN: SIG-Y3 SHARPNESS: 7	18		2.8	3.5	4.2	dB
30	SHARPNESS variable range 1	Gshr1	Y IN: SIG-Y3 SHARPNESS: F			6.8	7.6	8.3	dB
31	SHARPNESS variable range 2	Gshr2	Y IN: SIG-Y3 SHARPNESS: 0		$Gshr1, 2 = 20 \log \frac{Vx\ (f = 3MHz)}{Vx\ (f = 100kHz)}$	–6.3	–5.2	–4.1	dB
32	SUB CONT variable range 1	Gsc1	Y IN: SIG-Y2 SUB CONT: F	18		1.9	2.4	2.9	dB
33	SUB CONT variable range 2	Gsc2	Y IN: SIG-Y2 SUB CONT: 0		$Gsc1, 2 = 20 \log \frac{Vx\ (SUB\ CONT: F/0)}{Vx\ (SUB\ CONT: 7)}$	–3.5	–3.1	–2.7	dB
34	Y OUT frequency response	fyout	Y IN: SIG-Y4	18	 $fyout = 20 \log \frac{Vx\ (f = 8MHz)}{Vx\ (f = 100kHz)}$	–3.0	–0.5	2.2	dB
35	C-TRAP attenuation 358	C-trap1	Y IN: SIG-Y5 TRAP SW: 0/1 CTRAPADJ: adjustment value	18			–35	–25	dB
36	C-TRAP attenuation 443	C-trap2	Y IN: SIG-Y6 TRAP SW: 0/1 CTRAPADJ: adjustment value	18	$C\text{-}trap = 20 \log \frac{Vx\ (TRAP\ SW: 1)}{Vx\ (TRAP\ SW: 0)}$		–35	–25	dB

No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
C system items									
37	UOUT output amplitude	Vuout	C IN: SIG-C1 (No.37 to 42)	19		0.9	1.2	1.5	V
38	VOUT output amplitude	Vvout	C IN: SIG-C2 (No.37 to 42)	20		0.9	1.2	1.5	V
39	COLOR variable range 1	Gcol1	COLOR: 3F	19 20	Gcol1, 2 = 20 log $\frac{\text{Vx (COLOR: 3F/0)}}{\text{Vx (COLOR: 1F)}}$	5.8	6.3	6.8	dB
40	COLOR variable range 2	Gcol2	COLOR: 0					10	mV
41	SUB COLOR variable range 1	Gscol1	SUB COLOR: F	19 20	Gscol1, 2 = 20 log $\frac{\text{Vx (SUB COLOR: F/0)}}{\text{Vx (SUB COLOR: 7)}}$	2.1	2.7	3.3	dB
42	SUB COLOR variable range 2	Gscol2	SUB COLOR: 0			–5.0	–3.6	–2.3	dB
43	HUE center offset	ϕoffset		—		–11	–3	5	deg
44	Killer point	KP	CVBS: burst only During NTSC input	—			–33		dB
45	APC pull-in range	ΔfAPC		—	Confirm that the burst frequency is pulled in at 3.58MHz ± 400Hz.	–400		400	Hz

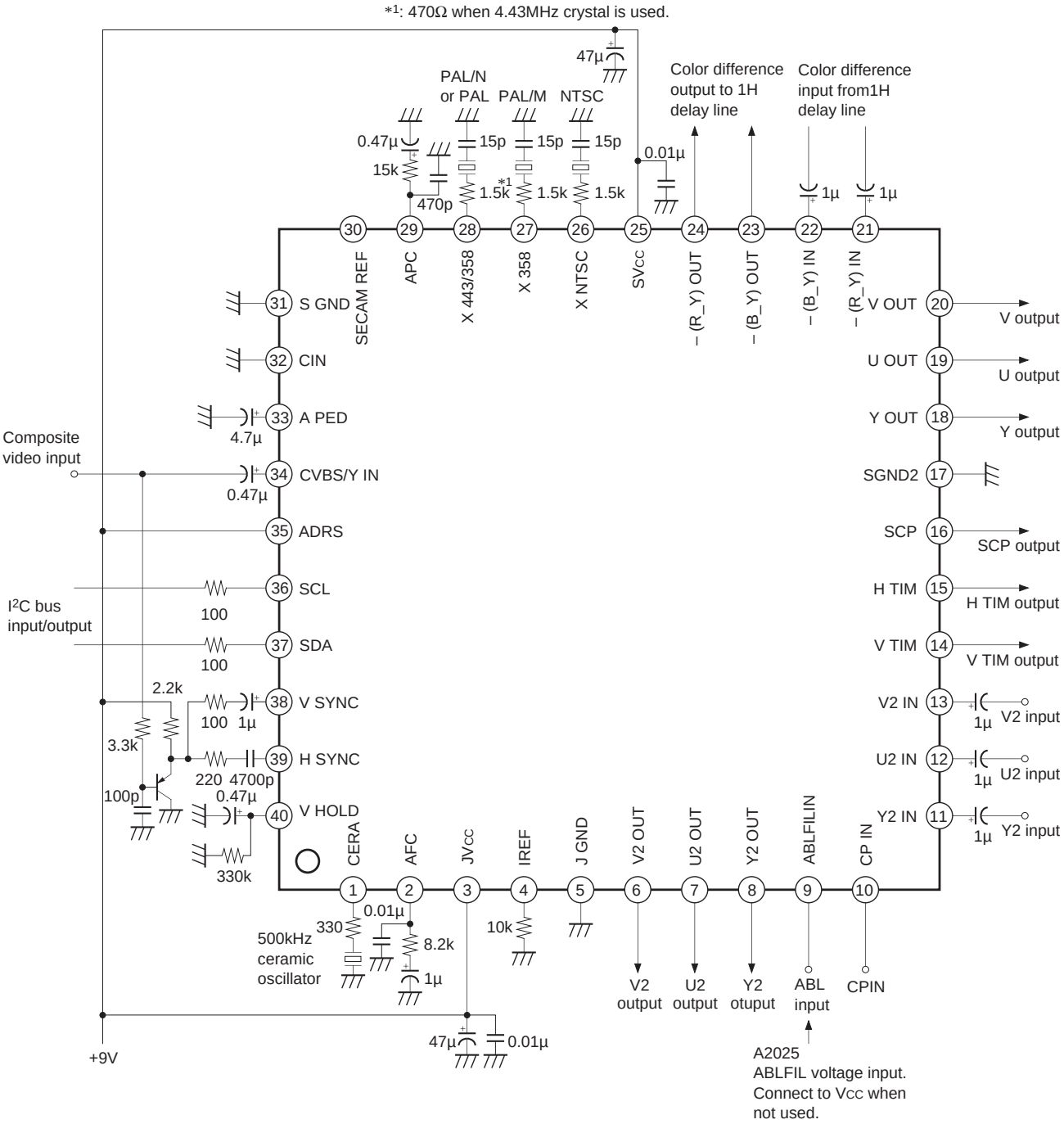
I²C BUS System Items

No.	Item	Symbol	Min.	Typ.	Max.	Unit
46	High level input voltage	Vih	3.0	—	5.0	V
47	Low level input voltage	Vil	0	—	1.5	V
48	High level input current	Iih	—	—	10	µA
49	Low level input current	Iil	—	—	10	µA
50	Low level output voltage During current inflow of 3 mA to SDA (Pin 37)	Vol	0	—	0.4	V
51	SDA inflow current	Iol	3	—	—	mA
52	Input capacitance	Ci	—	—	10	pF
53	Clock frequency	fscl	0	—	100	kHz
54	Minimum waiting time for data change	tbuf	4.7	—	—	µs
55	Waiting time for data transfer start	thd;sta	4.0	—	—	µs
56	Low level clock pulse width	tlow	4.7	—	—	µs
57	High level clock pulse width	thigh	4.0	—	—	µs
58	Waiting time for start preparation	tsu;sta	4.7	—	—	µs
59	Data hold time	thd;dat	0	—	—	µs
60	Data preparation time	tsu;dat	250	—	—	ns
61	Rise time	tr	—	—	300	ns
62	Fall time	tf	—	—	300	ns
63	Waiting time for stop preparation	tsu;sto	4.7	—	—	µs

Electrical Characteristics Measurement Circuit

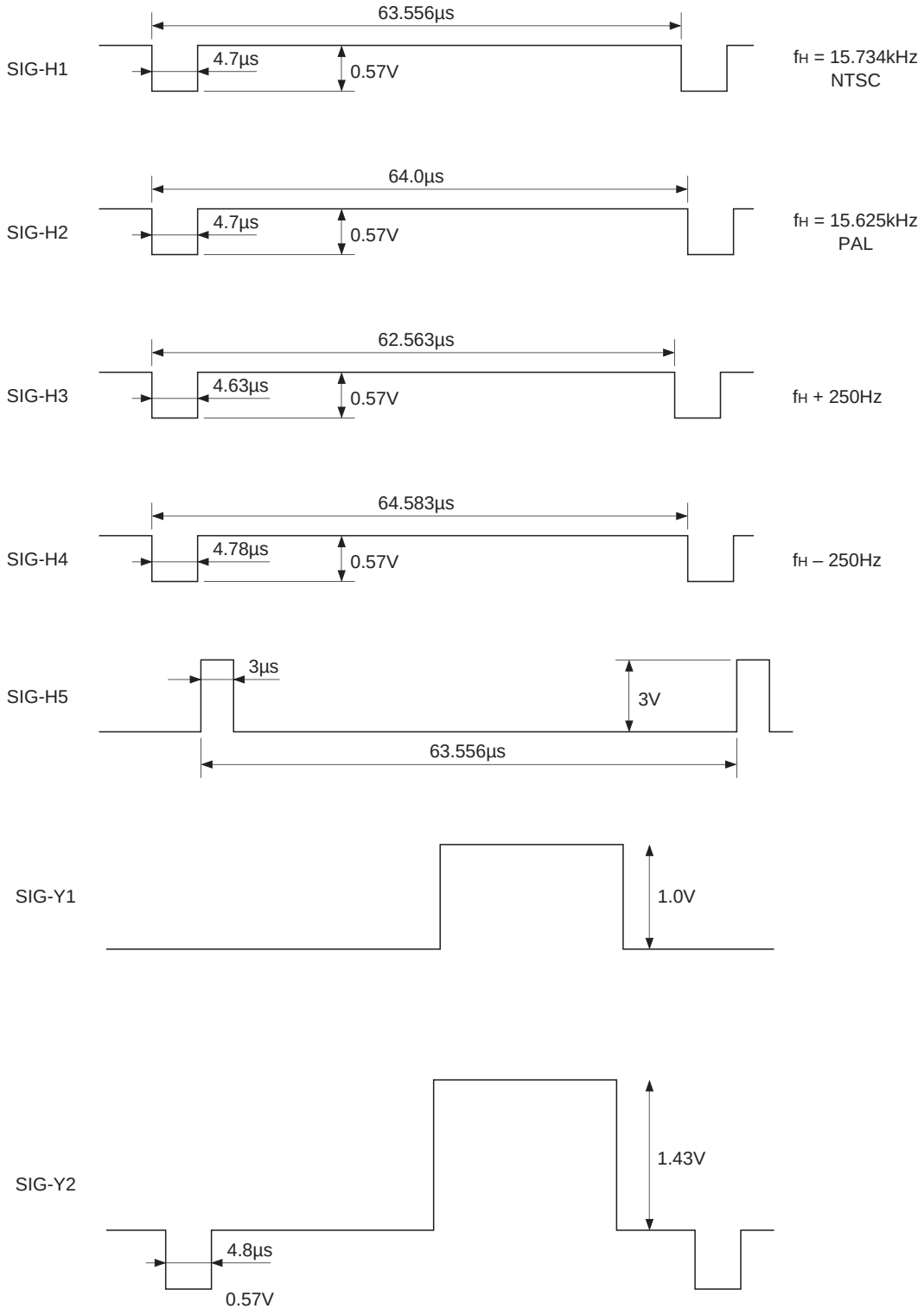


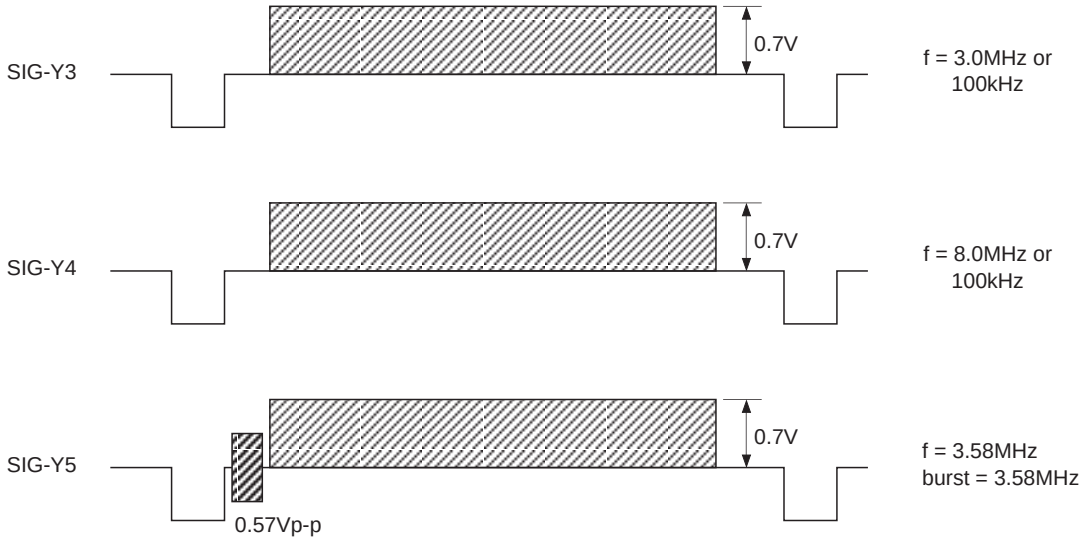
Application Circuit



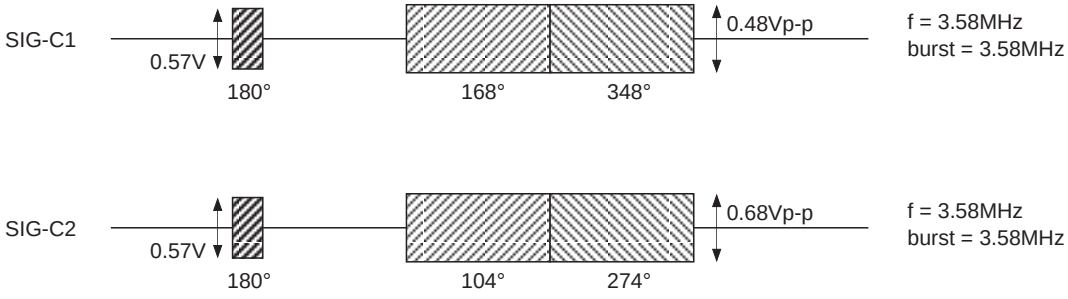
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Signals Used for Measurements





SIG-Y6: f = 4.43MHz, burst = 4.43MHz for SIG-Y5 signal



Description of Operation

1. Sync System

The video signals (standard input level: 2Vp-p) input to Pins 38 and 39 are sync separated by the horizontal and vertical sync separation circuits.

The resulting horizontal sync signal and the signal obtained by frequency dividing the $32f_H$-VCO output using the ceramic oscillator (frequency 500kHz or 503.5kHz) by 32 are phase compared, the AFC loop is constructed, and an H pulse (HTIM) synchronized with the H sync is output from Pin 15.

The vertical sync signal is sent to the V countdown block where the most appropriate window processing is performed to obtain V sync timing information which resets the counter. A V pulse (VTIM) synchronized with the V sync is output from Pin 14. In addition, BGP, HBLK and VBLK are output from Pin 16 as SCP (sand castle pulse).

2. Y System

There are two input systems.

Composite video input (2Vp-p) → 1 system
Y/C separation input (2Vp-p) → 1 system

The Y signal (specified input level: 2Vp-p) input to Pin 34 passes through the subcontrast control, chroma trap, delay line, sharpness control, clamp and auto pedestal circuits, is gain adjusted by the YDRIVE circuit and is then output.

The CXA2019AQ has a built-in chroma trap, enabling the video signal to be input directly. The trap frequency is automatically adjusted inside the IC. However, the trap frequency is affected by variations among the ICs, so fine adjustment through the I^2C bus may be required.

Because the f0 of the filter is not specified when the color killer function is operating, turn the trap OFF if there are any difficulties.

The Y signal delay time can be varied in approximately 60ns increments through the I^2C bus register (DELAY). In addition, when the C system TOT is ON, the Y signal delay time is increased by approximately 140ns to cope with the increase in the C system delay time caused by the TOT filter.

The sharpness control is a delay line type and the sharpness f0 can be switched to 1.5MHz or 3MHz.

3. C System

The CVBS or chroma signal (specified input level: burst level of 570mVp-p) selected by the internal video switch passes through the ACC, TOT, chroma amplifier and demodulation circuits, is demodulated into the R-Y and B-Y color difference signals, and is then inversed and output from Pins 23 and 24. However, during NTSC the signals are 6dB amplified by the internal DET switch and gain adjusted by the COLOR circuit. During PAL the signals are 6dB amplified by the 1H delay line, input to Pins 21 and 22, and gain adjusted by the COLOR circuit. Signals that have passed through the 1H delay line can also be input to the COLOR circuit during NTSC by using the I^2C bus register (EXT COLOR). This provides comb filter effects.

In addition, the color system (NTSC/PAL) and the subcarrier frequency (3.58MHz/4.43MHz) are automatically identified according to the input chroma signal, and the internal VCO and demodulation circuit, etc., are adjusted automatically. Furthermore, SECAM signals can also be automatically identified by connecting an external SECAM decoder to Pin 30. In this case, Pins 23 and 24 and the SECAM decoder color difference output are linked together directly, and one side goes to high impedance and the other side goes to low impedance according to the input chroma signal, and then they are input to the external 1H delay line.

System identification can be set to automatic or forced mode by the I^2C bus register. The color system is output to the status register.

The pedestal levels of the U and V color difference signals are clamped by UPED and VPED, respectively, and then these signals are output. However, the DC of the video portion can be controlled by the I^2C bus register, allowing the offset to be adjusted at the PINP processor input.

4. YUV Reinput System

The U and V color difference signals (output from the PINP processor) input to Pins 12 and 13 are clamped according to the pulse input to Pin 10, gain controlled by the U2 and V2 drive circuits, the DC of their video portion is controlled by the U2PED and V2PED circuits, and then these signals are output from Pins 6 and 7. This function allows adjustment of the white balance and black level of the PINP sub picture.

In addition, the Y signal input to Pin 11 is clamped in the same manner, gain controlled by the Y2 drive circuit, and output from Pin 8. At this time, bright ABL with a polarity opposite that of the main picture ABL can be applied by inputting the main picture Y/C/J IC ABLFIL voltage to Pin 9. This allows fluctuation of the black level of the sub picture caused by the main picture ABL to be suppressed. This reverse polarity ABL can be turned ON and OFF and the gain and control curve center values can be set by the I^2C bus register.

Notes on Operation

- The CXA2019AQ does not perform the initial settings during power ON. This initial data should be input from a microcomputer.
- Because the YUV signal output from the CXA2019AQ are DC direct connected, the board pattern must be designed consideration given to minimizing interference from around the power supply and GND.
  Do not separate the GND patterns for each pin; a solid earth is ideal. Locate the power supply side of the bypass capacitor which is inserted between the power supply and GND as near to the pin as possible. Also, locate the XTAL oscillator, ceramic oscillator and IREF resistor as near to the pin as possible, and do not wire signal lines near this pin.
- Use lead type (HC-49/U type) for each XTAL oscillator. Confirm that there is no problem for capture range color response and others at resistors and capacitors as shown in Application Circuit.
- Murata's Ceralock is recommended for ceramic oscillator. When using only for NTSC, 503.5kHz Ceralock; for NTSC/PAL, 500kHz Ceralock is recommended.
- Use a resistor (such as a metal film resistor) with an error of less than 1% for the IREF pin.
- For unused pins, leave them open.

Definition of I^2C BUS Registers

Slave Addresses

Slave Receiver	**Slave Transmitter**
9AH: ADRS = "High"	9BH: ADRS = "High"
9EH: ADRS = "Low"	9FH: ADRS = "Low"

Register Table

×: Don't care, ∗: Undefined

Control Register

Sub Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
×××× 0 0 0 0	HUE						DPIC OFF	CV/YC
×××× 0 0 0 1	COLOR						HMASK	CANAL
×××× 0 0 1 0	SHARPNESS				SUB CONT			
×××× 0 0 1 1	SUB HUE				SUB COLOR			
×××× 0 1 0 0	CTRAPADJ				AFC		TRAP ON	TOT ON
×××× 0 1 0 1	Y DRIVE					SHP-f0	FSC OUT	CD MODE2
×××× 0 1 1 0	U PED				V PED			
×××× 0 1 1 1	U2 PED				V2 PED			
×××× 1 0 0 0	Y2 DRIVE					DC TRAN		
×××× 1 0 0 1	U2 DRIVE					PRE OVER		ABL OFF
×××× 1 0 1 0	V2 DRIVE					ABL CENT		ABL
×××× 1 0 1 1	COL SYSTEM		X'TAL PIN		V FREQ		DELAY	
×××× 1 1 0 0	COL LOOP		SCP BGF		SCP BGR		EXT COLOR	1

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
H LOCK	KILLER	NT/PAL	50/60	SECAM	VCO-F	∗	∗

Description of I²C BUS Registers

Sub Address 0000

HUE (6): Hue control
0 = Flesh color appears red.
63 = Flesh color appears green.

DPIC OFF (1): Y black expansion ON/OFF switch
0 = ON
1 = OFF

CV/YC (1): Input selector switch
0 = CVBS input
1 = Y/C input

Sub Address 0001

COLOR (6): Color control
0 = Minimum
63 = Maximum

HMASK (1): Macrovision measures
0 = OFF
1 = ON

CANAL (1): When this register is set to "1", the first and last 3H of the video are replaced by DC during YUV output.
0 = No video portion DC replacement
1 = DC replacement

Sub Address 0010

SHARPNESS (4): Sharpness control
0 = Minimum
15 = Maximum

SUB CONT (4): Sub contrast adjustment
0 = Minimum
15 = Maximum

Sub Address 0011

SUB HUE (4): Hue center adjustment
0 = Flesh color appears red.
15 = Flesh color appears green.

SUB COLOR (4): Color center adjustment
0 = Minimum
15 = Maximum

Sub Address 0100

C-TRAP ADJ (4): Chroma trap f0 adjustment
0 = High
7 = Center
15 = Low

AFC (2): AFC loop gain selector
0 = AFC loop gain high
1 = AFC loop gain medium
2 = AFC loop gain low
3 = AFC loop open, free-running mode

TRAP ON (1): Y system chroma trap ON/OFF
0 = OFF
1 = ON

TOT ON (1): Chroma TOT filter ON/OFF
0 = OFF
1 = ON

Sub Address 0101

Y DRIVE (5): Y output gain control
0 = –6.3dB
31 = +3.5dB

SHP-f0 (1): Sharpness f0 selector
0 = 3MHz
1 = 1.5MHz

FSC OUT (1): When this register os set to "1", the subcarrier frequency is output constantly from Pin 30.
0 = Output only during the VBLK interval in SECAM mode
1 = Constantly output

CD MODE2 (1): V sync signal pull-in speed selector
0 = Standard
1 = High speed

Sub Address 0110

U PED (4): DC control of pedestal portion of U output (for video)
0 = –8mV
7 = Center
15 = +10mV

V PED (4): DC control of pedestal portion of V output (for video)
0 = –8mV
7 = Center
15 = +10mV

Sub Address 0111

U2 PED (4): DC control of pedestal portion of U2 output reinput from PinP processor (for video)
0 = –35mV
7 = Center
15 = +40mV

V2 PED (4): DC control of pedestal portion of V2 output reinput from PinP processor (for video)
0 = –35mV
7 = Center
15 = +40mV

Sub Address 1000

Y2 DRIVE (5): Y2 output gain control
0 = –4dB
31 = +2.8dB

DC TRAN (3): DC transmission ratio setting
0 = Maximum (100%)
7 = Minimum (78%)

Sub Address 1001

U2 DRIVE (5): U2 output gain control
0 = –6.3dB
31 = +3.6dB

PRE OVER (2): Sharpness preshoot/overshoot ratio setting
0 = 1:2 (PRE:OVER)
3 = 2:1

ABL OFF (1): ON/OFF for ABL applied to Y2 OUT
0 = ON
1 = OFF

Sub Address 1010

V2 DRIVE (5): V2 output gain control
0 = –6.3dB
31 = +3.6dB

ABL CENT (2): ABL center voltage control
0 = Minimum
3 = Maximum

ABL (1): ABL gain control
0 = Standard
1 = Low

Sub Address 1011

COL SYSTEM (2): Selects the color system identification method.
0 = Fixed to NTSC
1 = Fixed to PAL
2 = Fixed to SECAM
3 = Automatic identification

X'TAL PIN (2): Selects the crystal.
0 = Fixed to Pin 26 (XNTSC)
1 = Fixed to Pin 27 (X358)
2 = Fixed to Pin 28 (X443/358)
3 = Automatic identification

V FREQ (2): Inputs the V frequency during no signal.
0 = Force to 60Hz
1 = Force to 50Hz
2 = Automatic (previous status maintained)

DELAY (2): Allows the following delay times to be added to the Y signal.
0 = 0ns
1 = 60ns
2 = 120ns
3 = 180ns

Sub Address
1100

COL LOOP (2): Specifies the identified color system when COL SYSTEM is set to automatic identification.
0 = PALM/PALN/NTSC
(Pin 28 = PALN crystal, Pin 27 = PALM crystal, Pin 26 = NTSC crystal)
1 = PAL/SECAM/4.43NTSC/NTSC
(Pin 28 = 4.43MHz crystal, Pin 27 = open, Pin 26 = NTSC crystal)
2 = PAL/SECAM (Pin 28 = 4.43MHz crystal, Pin 27 = open, Pin 26 = open)
3 = PALM/NTSC (Pin 28 = open, Pin 27 = PALM crystal, Pin 26 = NTSC crystal)

SCP BGF (2): Controls the phase of the falling edge of the BGP in the SCP output.
(0.4µs per step)
0 = +0.4µs
1 = Center
3 = –0.8µs

SCP BGR (2): Controls the phase of the rising edge of the BGP in the SCP output.
(0.4µs per step)
0 = +0.4µs
1 = Center
3 = –0.8µs

EXT COLOR (1): Forcibly switches the DET switch input to external input (R-Y IN, B-Y IN).
0 = Switched by the NTSC/PAL identification results
1 = External input

H LOCK (1): Returns whether or not the IC's H oscillator and the signal input to H SYNC are locked.
0 = Not locked
1 = Locked

KILLER (1): Returns the color killer ON/OFF status.
0 = OFF
1 = ON

NT/PAL (1): Identifies whether the input signal is NTSC or PAL and returns the results.
0 = NTSC
1 = PAL

50/60 (1): Returns the 50/60Hz identification results.
0 = 60Hz
1 = 50Hz

SECAM (1): Identifies whether or not the input signal is SECAM and returns the results.
0 = Not SECAM
1 = SECAM

VCO-F (1): Detects the input signal burst frequency and returns the results.
0 = 3.58MHz
1 = 4.43MHz

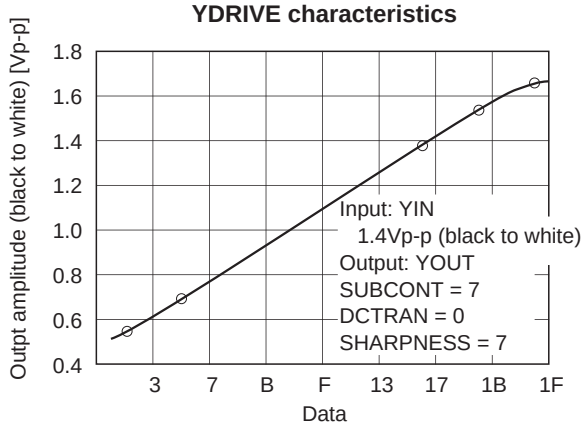
I²C BUS Register Initial Settings

Register name	No. of bits	Initial setting	Description
HUE	6	1FH	Center value
DPIC OFF	1	0H	DPIC ON
CV/YC	1	1H	Y/C input selection
COLOR	6	1FH	Center value
HMASK	1	0H	Macrovision measures OFF
CANAL	1	0H	CANAL OFF
SHARPNESS	4	7H	Center value
SUB CONT	4	7H	Center value
SUB HUE	4	7H	Center value
SUB COLOR	4	7H	Center value
CTRAP ADJ	4	7H	Center value
AFC	2	1H	Center value
TRAP ON	1	0H	TRAP OFF
TOT ON	1	0H	TOT OFF
Y DRIVE	5	FH	Center value
SHP-f0	1	0H	SHP = 3MHz
FSC OUT	1	0H	FSC OUT OFF
CD MODE2	1	0H	Standard
U PED	4	7H	Center value
V PED	4	7H	Center value

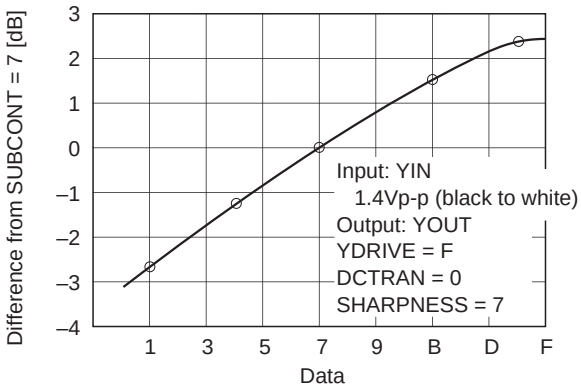
Register name	No. of bits	Initial setting	Description
U2 PED	4	7H	Center value
V2 PED	4	7H	Center value
Y2 DRIVE	5	FH	Center value
DC TRAN	3	0H	Minimum value
U2 DRIVE	5	FH	Center value
PRE OVER	2	0H	Minimum value
ABL OFF	1	1H	ABL OFF
V2 DRIVE	5	FH	Center value
ABL CENT	2	0H	Minimum value
ABL	1	0H	Standard
COL SYSTEM	2	0H	NTSC
X'TAL PIN	2	0H	Pin 26 selection
VFREQ	2	0H	60Hz fixed
DELAY	2	0H	Minimum value
COL LOOP	2	0H	PAL M/N/NTSC
SCP BGF	2	1H	Center value
SCP BGR	2	1H	Center value
EXT COLOR	1	0H	Automatic identification

Example of Representative Characteristics

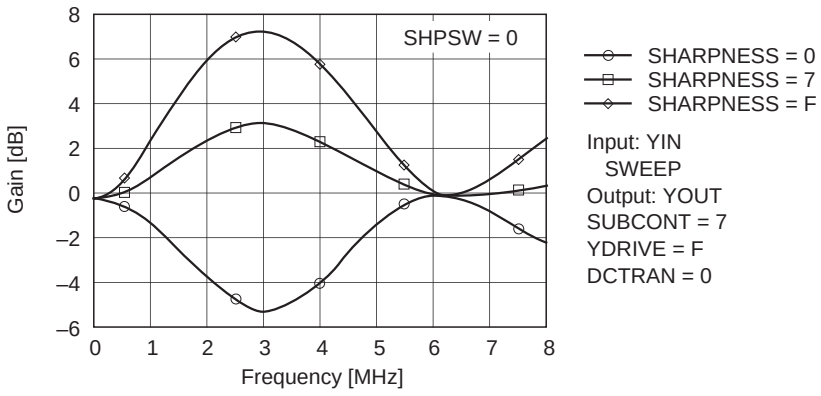
YDRIVE characteristics



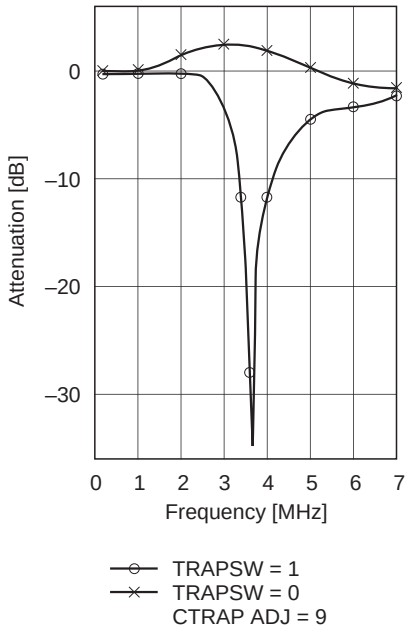
SUBCONT characteristics



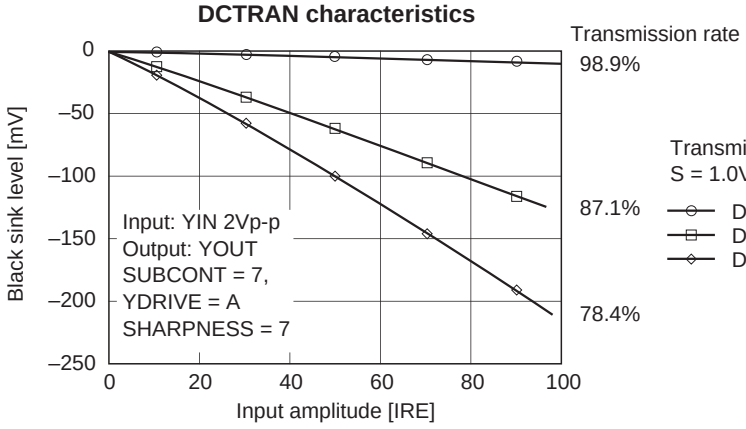
SHARPNESS characteristics



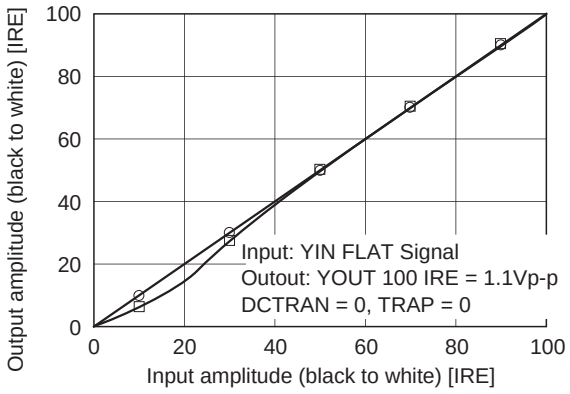
TRAP attenuation



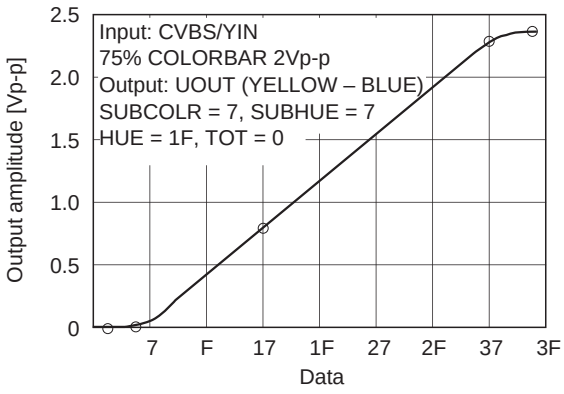
DCTRAN characteristics



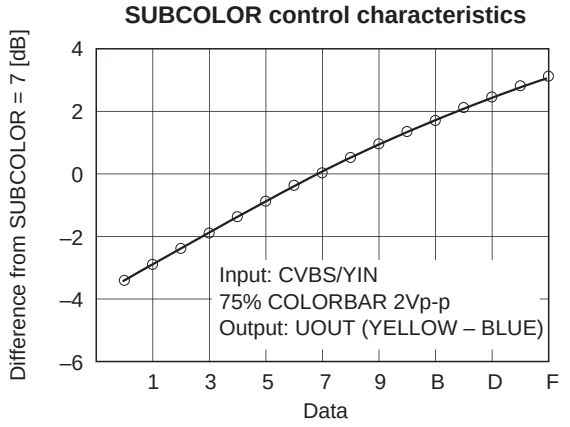
AUTOPED characteristics



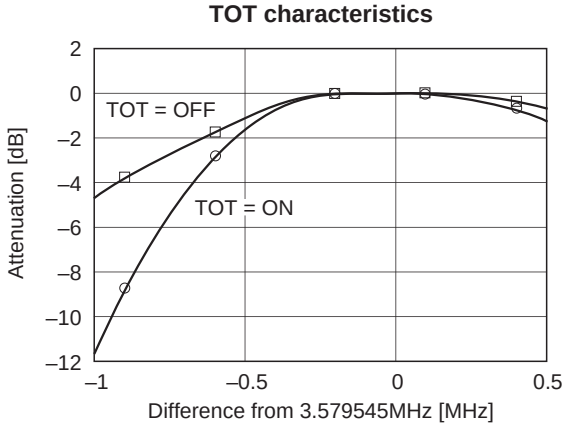
COLOR control characteristics



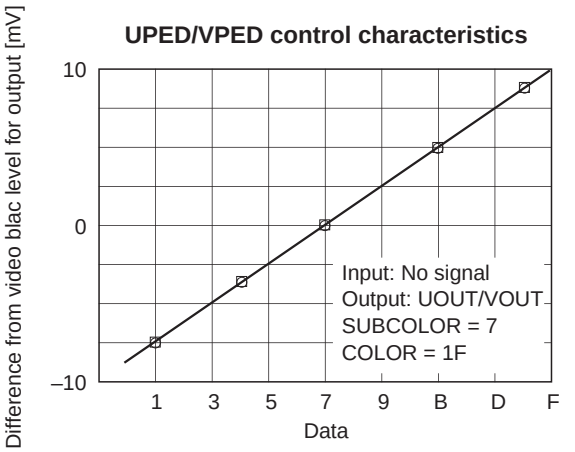
SUBCOLOR control characteristics



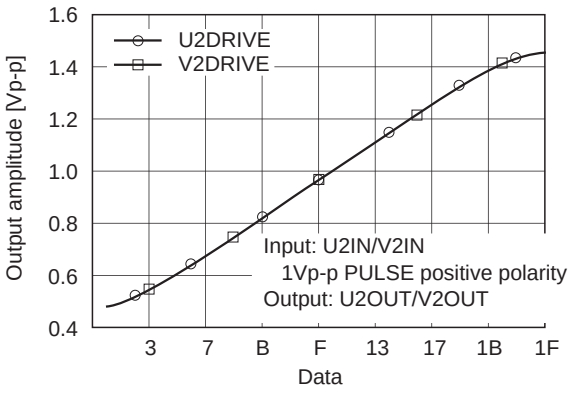
TOT characteristics



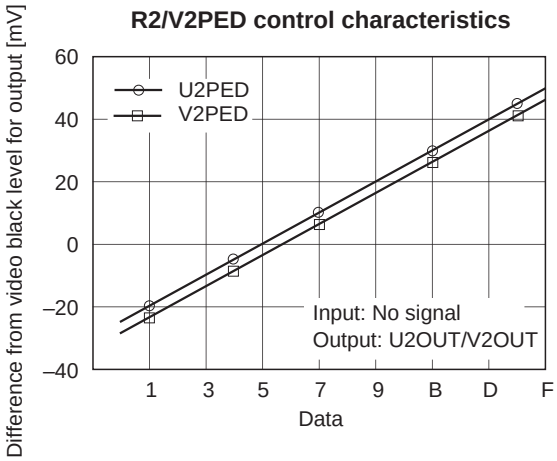
UPED/VPED control characteristics



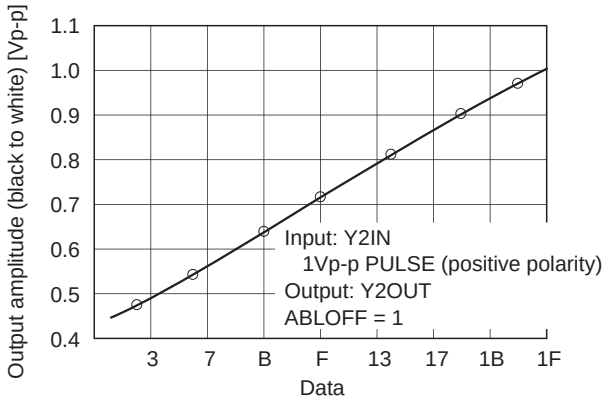
R2/V2DRIVE control characteristics



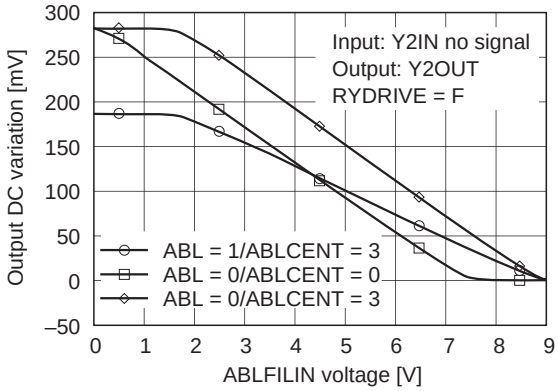
R2/V2PED control characteristics



Y2DRIVE control characteristics

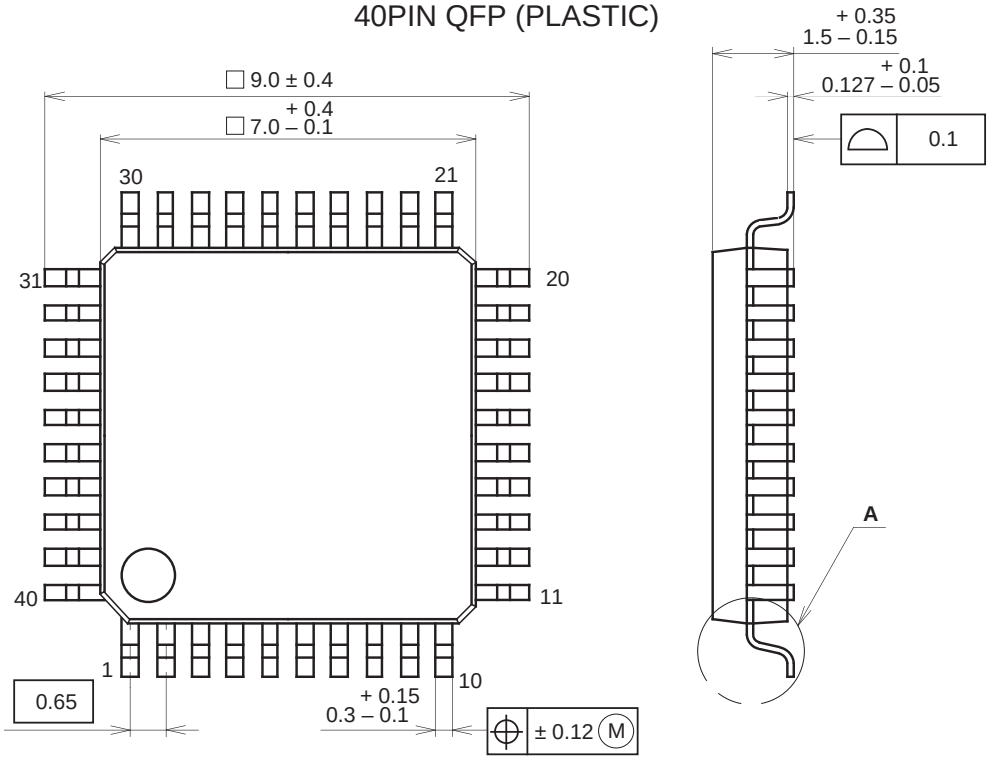


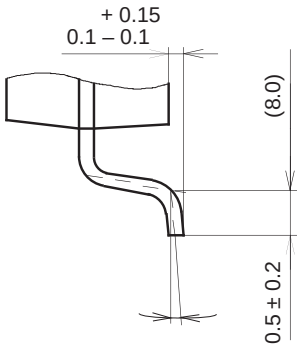
ABL control characteristics



Package Outline Unit: mm

40PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).