SONY

CXA2054S

US Audio Multiplexing Decoder

Description

The CXA2054S is an IC designed as a decoder for the Zenith TV Multi-channel System and also corresponds with I²C BUS. Functions include stereo demodulation, SAP (Separate Audio Program) demodulation, dbx noise reduction and sound processor. Various kinds of filters are built in while adjustment, mode control and sound processor control are all executed through I²C BUS.

Features

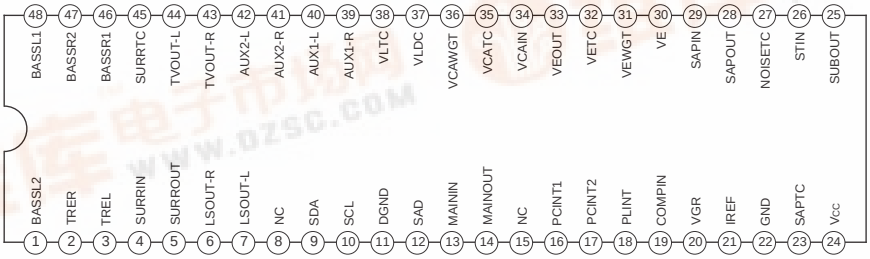
- Audio multiplexing decoder, dbx noise reduction decoder and sound processor (surround, volume limiter, bass · treble, volume) are all included in a single chip. Almost any sort of signal processing is possible through this IC.
- All adjustments are possible through I²C BUS to allow for automatic adjustment.
- Various built-in filter circuits greatly reduce external parts.
- There are two channel external inputs for LSOUT outputs.
- Automatic volume control between input sources is possible through volume limiter.

Standard I/O Level

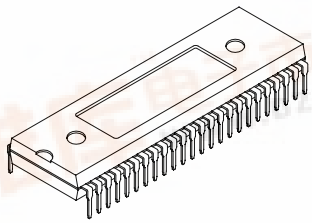
- Input level

COMPIN (Pin 19)	245 mVrms
AUX1-L/R (Pins 40 and 39)	490 mVrms
AUX2-L/R (Pins 42 and 41)	490 mVrms
SURRIN (Pin 4)	490 mVrms

Pin Configuration (Top View)



48 pin SDIP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	2.2	W

Range of Operating Supply Voltage

9±0.5 V

Applications

TV, VCR and other decoding systems for US audio multiplexing TV broadcasting

Structure

Bipolar silicon monolithic IC

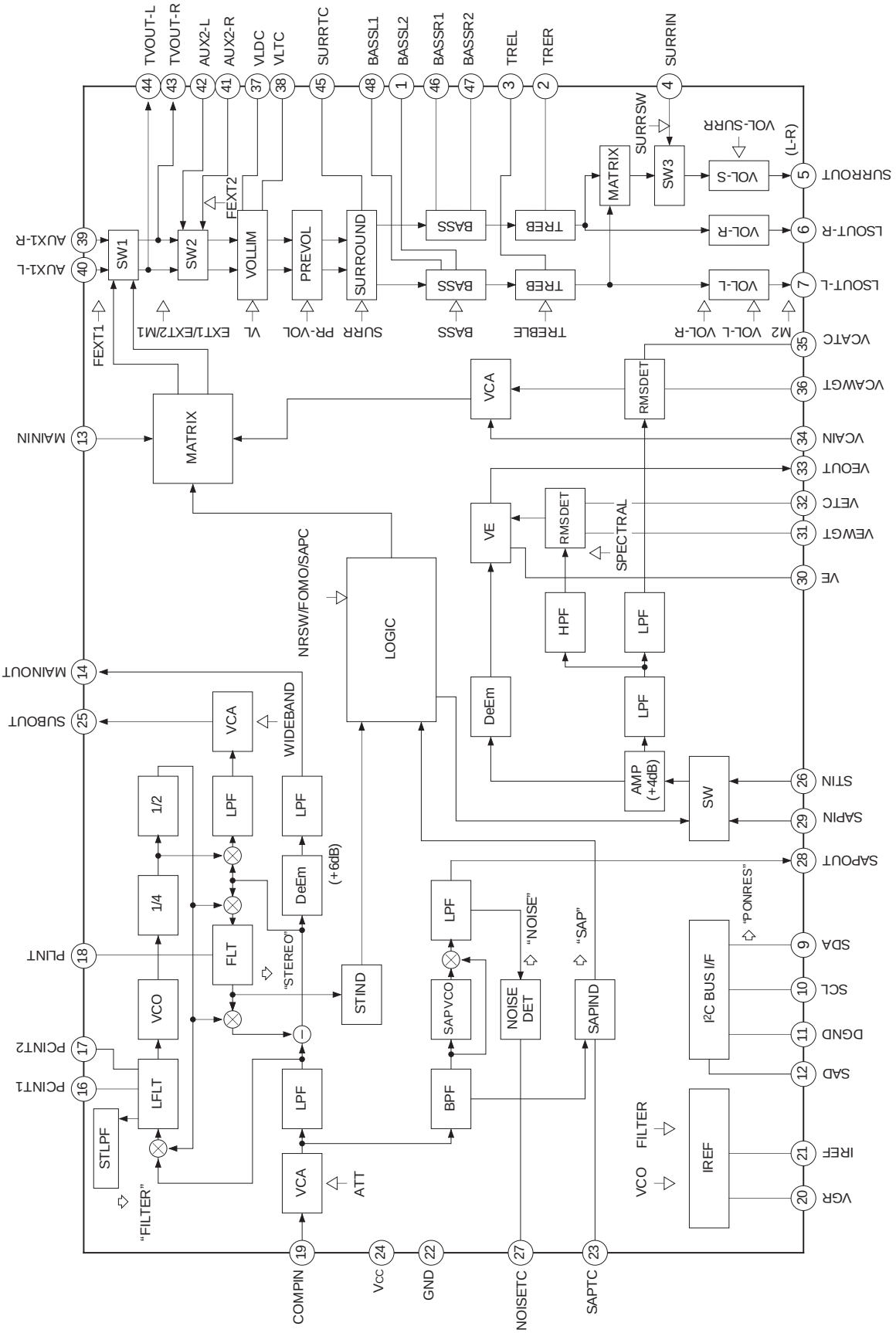
- Output level

TVOUT-L/R (Pins 44 and 43)	490 mVrms
LSOUT-L/R (Pins 7 and 6)	490 mVrms
SURROUT (Pin 5)	490 mVrms

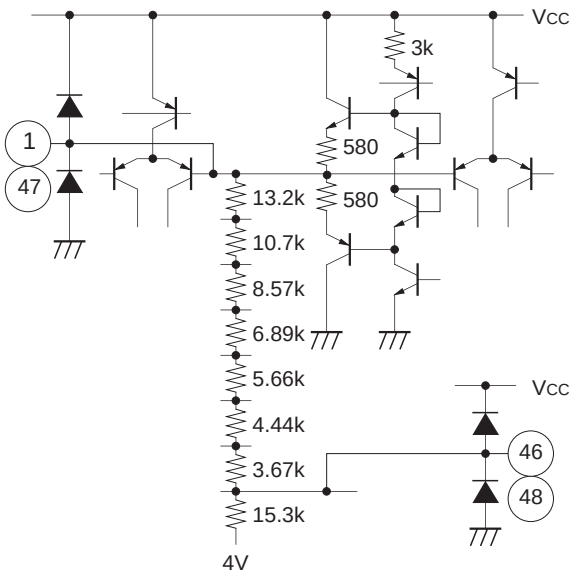
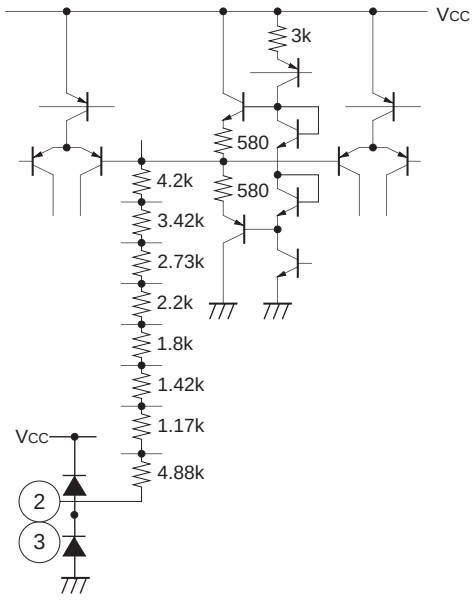
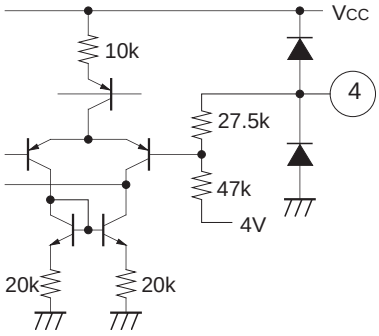
∗A license of the dbx-TV noise reduction system is required for the use this device.

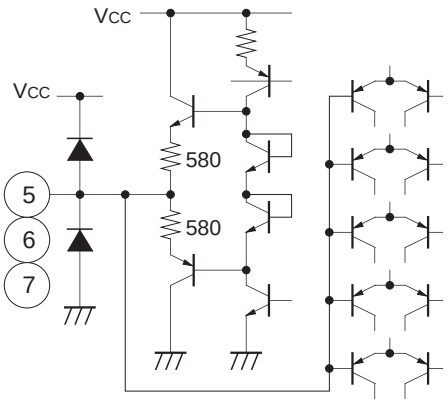
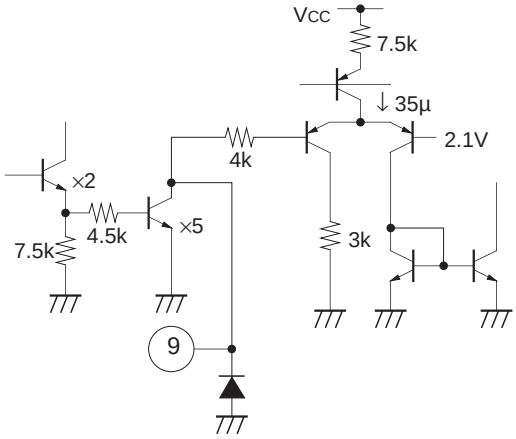
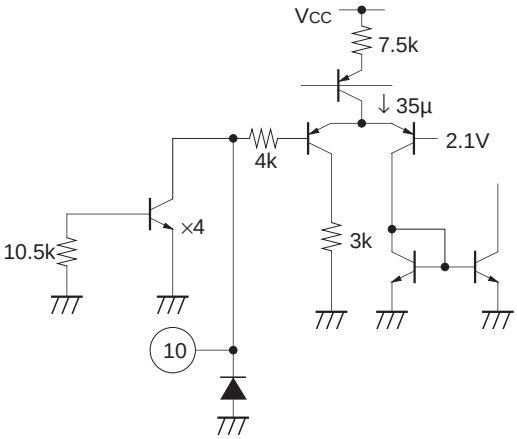
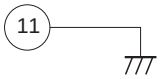
E96Y15B86-TE

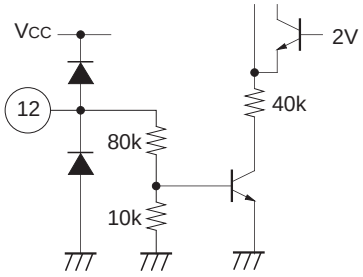
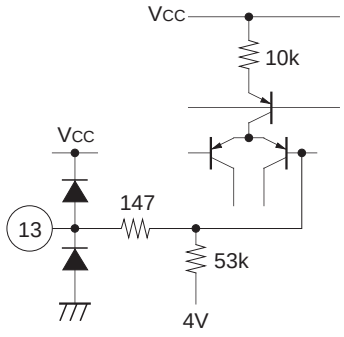
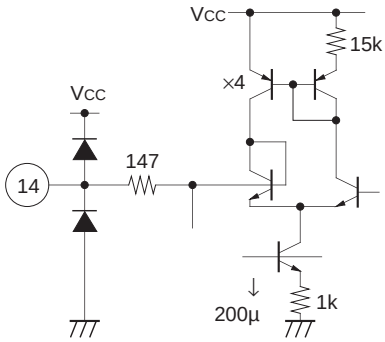
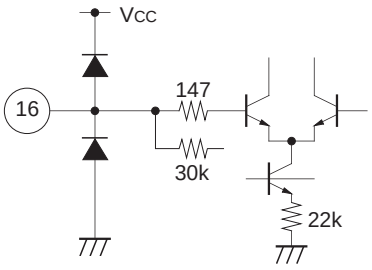
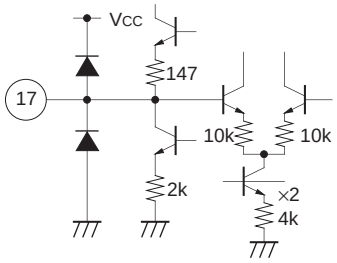
Block Diagram

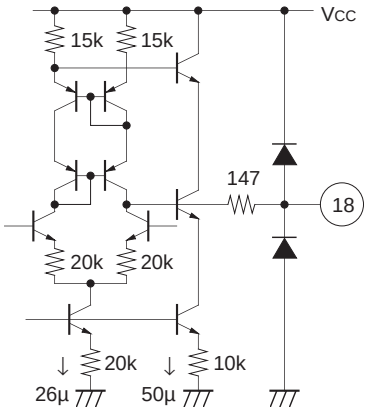
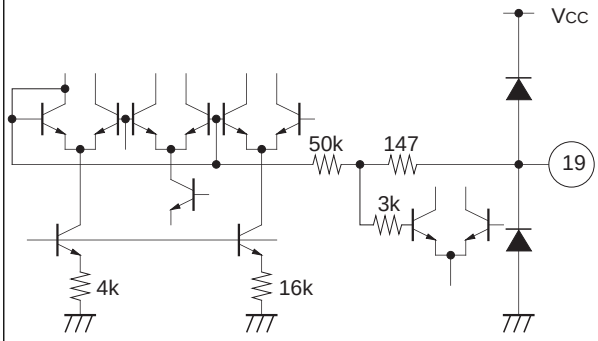
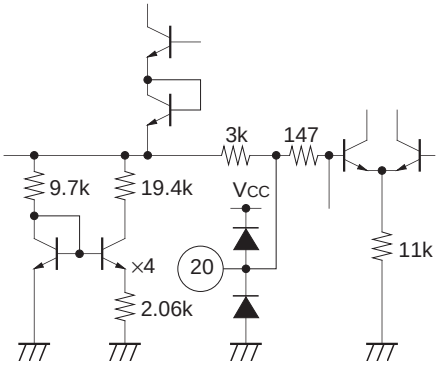
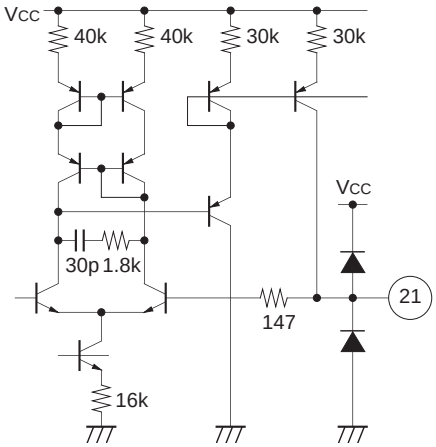


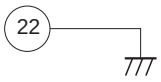
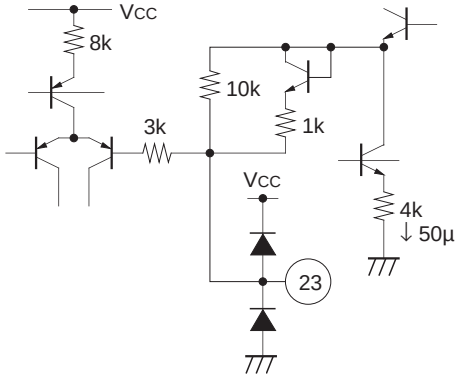
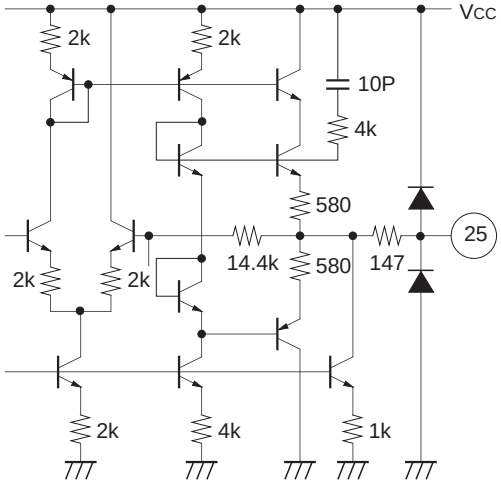
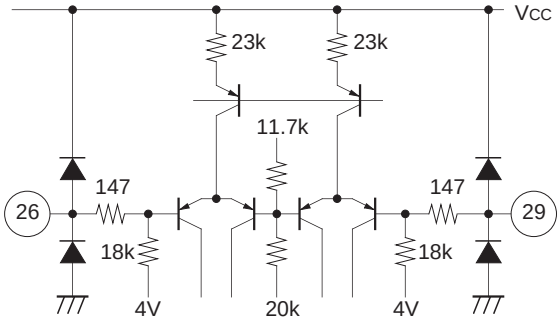
Pin Description (Ta=25 °C, Vcc=9 V)

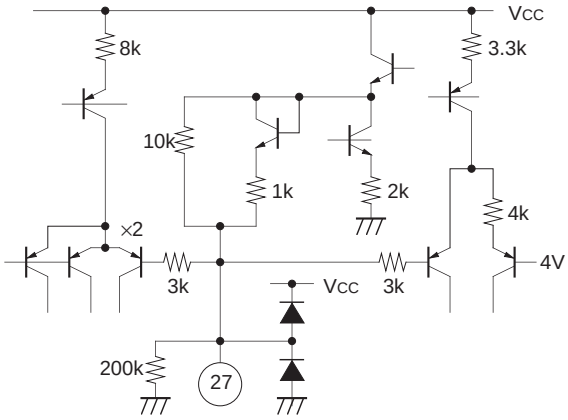
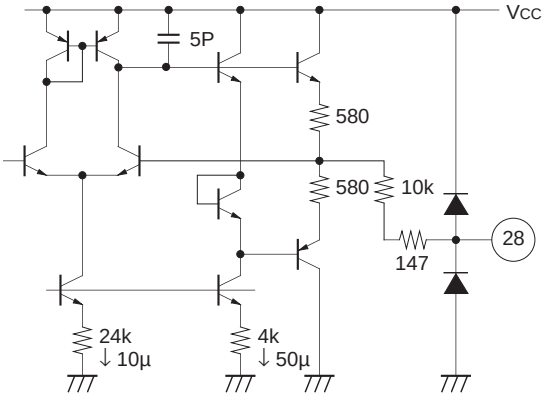
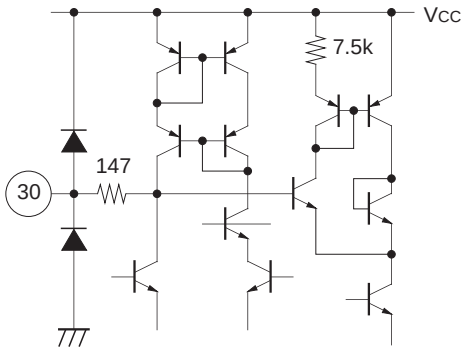
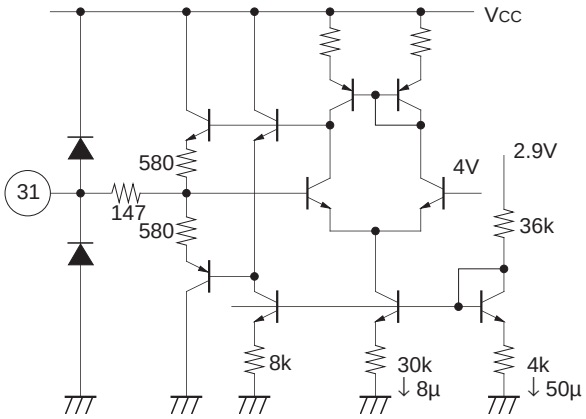
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	BASSL2	4.0 V		BASS filter pin. (Left channel) (Connect a 15 nF capacitor between Pins 1 and 48.) The cutoff frequency is determined by the built-in resistor and the external capacitance.
48	BASSL1	4.0 V		
47	BASSR2	4.0 V		BASS filter pin. (Right channel) (Connect a 15 nF capacitor between Pins 47 and 46.) The cutoff frequency is determined by the built-in resistor and the external capacitance.
46	BASSR1	4.0 V		
2	TRER	4.0 V		TREBLE filter pin. (Right channel) (Connect a 6.8 nF capacitor between this pin and GND.)
3	TREL	4.0 V		TREBLE filter pin. (Left channel) (Connect a 6.8 nF capacitor between this pin and GND.)
4	SURRIN	4.0 V		Surround external input pin.

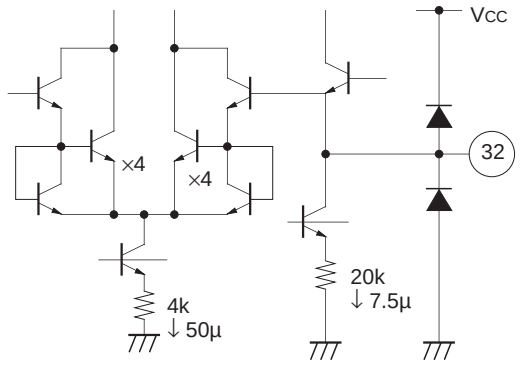
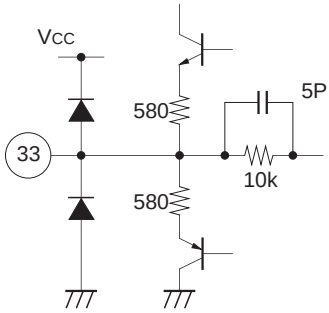
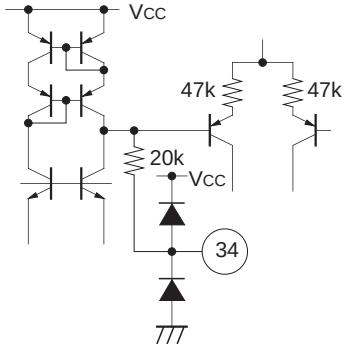
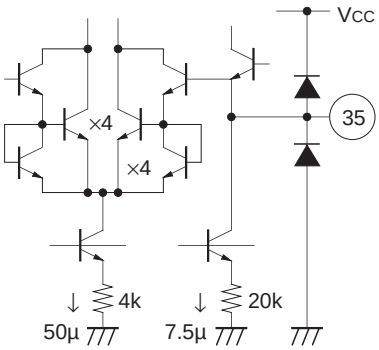
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
5	SURROUT	4.0 V		(L-R) signal output pin.
6	LSOUT-R	4.0 V		LSOUT right channel output pin.
7	LSOUT-L	4.0 V		LSOUT left channel output pin.
8	NC	—		—
9	SDA	—		Serial data I/O pin. V_{IH} > 3.0 V V_{IL} < 1.5 V
10	SCL	—		Serial clock input pin. V_{IH} > 3.0 V V_{IL} < 1.5 V
11	DGND	—		Digital block GND.

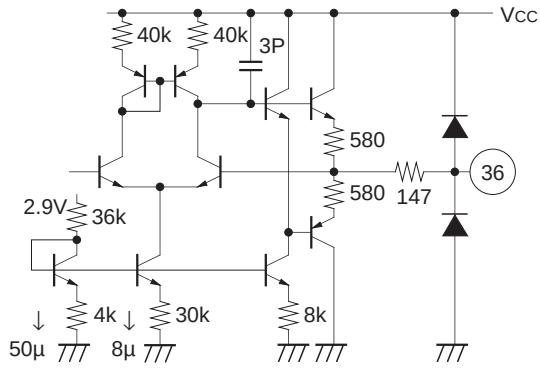
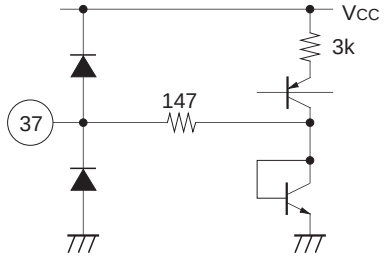
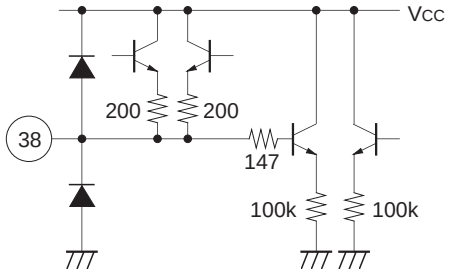
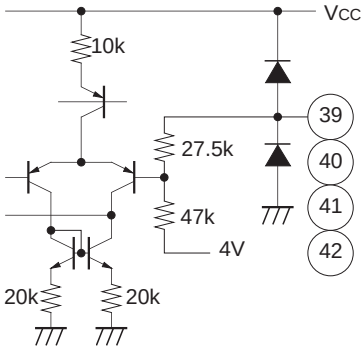
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	SAD	—		Slave address control switch. The slave address is selected by changing the voltage applied to this pin.
13	MAININ	4.0 V		Input the (L+R) signal from MAINOUT (Pin 14).
14	MAINOUT	4.0 V		(L+R) signal output pin.
15	NC	—		—
16	PCINT1	4.0 V		Stereo block PLL loop filter integrating pin.
17	PCINT2	4.0 V		

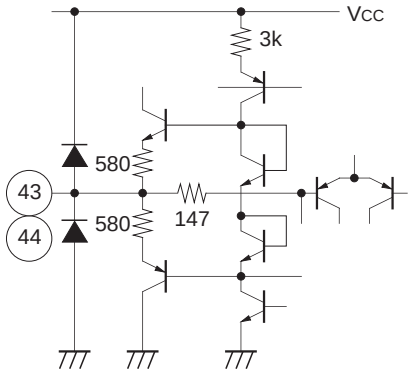
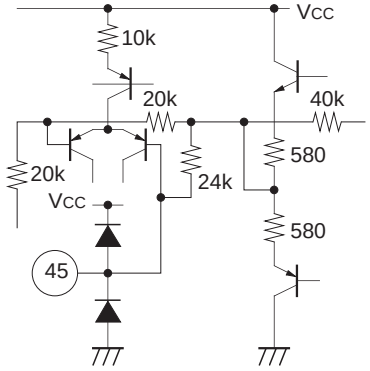
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
18	PLINT	5.1 V		Pilot cancel circuit loop filter integrating pin. (Connect a 1 µF capacitor between this pin and GND.)
19	COMPIN	4.0 V		Audio multiplexing signal input pin.
20	VGR	1.3 V		Band gap reference output pin. (Connect a 10 µF capacitor between this pin and GND.)
21	IREF	1.3 V		Set the filter and VCO reference current. The reference current is adjusted with the BUS DATA based on the current which flows to this pin. (Connect a 62 kΩ (±1 %) resistor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
22	GND	—		Analog block GND.
23	SAPTC	4.5 V		Set the time constant for the SAP carrier detection circuit. (Connect a 4.7 µF capacitor between this pin and GND.)
24	Vcc	—		Supply voltage pin.
25	SUBOUT	4.0 V		(L-R) signal output pin.
26	STIN	4.0 V		Input the (L-R) signal from SUBOUT (Pin 25).
29	SAPIN	4.0 V		Input the (SAP) signal from SAPOUT (Pin 28).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
27	NOISETC	3.0 V		Set the time constant for the noise detection circuit. (Connect a 4.7 µF capacitor between this pin and GND.)
28	SAPOUT	4.0 V		SAP FM detector output pin.
30	VE	4.0 V		Variable de-emphasis integrating pin. (Connect a 2700 pF capacitor and a 3.3 kΩ resistor in series between this pin and GND.)
31	VEWGT	4.0 V		Weight the variable de-emphasis control effective value detection circuit. (Connect a 0.047 µF capacitor and a 3 kΩ resistor in series between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
32	VETC	1.7 V		Determine the restoration time constant of the variable de-emphasis control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 3.3 µF capacitor between this pin and GND.)
33	VEOUT	4.0 V		Variable de-emphasis output pin. (Connect a 4.7 µF non-polar capacitor between Pins 33 and 34.)
34	VCAIN	4.0 V		VCA input pin. Input the variable de-emphasis output signal from Pin 33 via a coupling capacitor.
35	VCATC	1.7 V		Determine the restoration time constant of the VCA control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 10 µF capacitor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
36	VCAWGT	4.0 V		Weight the VCA control effective value detection circuit. (Connect a 1 µF capacitor and a 3.9 kΩ resistor in series between this pin and GND.)
37	VLDC	0.7 V		Volume limiter detection circuit bias pin. (Connect a 1 MΩ resistor between pins 37 and 38.)
38	VLTC			Set the time constant for the volume limiter detection circuit.
39	AUX1-R	4.0 V		Right channel external input 1 pin.
40	AUX1-L	4.0 V		Left channel external input 1 pin.
41	AUX2-R	4.0 V		Right channel external input 2 pin.
42	AUX2-L	4.0 V		Left channel external input 2 pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
43	TVOUT-R	4.0 V		TVOUT right channel output pin.
44	TVOUT-L			TVOUT left channel output pin.
45	SURRTC	4.0 V		Set the central frequency of the SURROUND circuit phase shifter. The frequency is determined by the built-in resistor and the external capacitance. (Connect a 0.022 µF capacitor between this pin and GND.)

Electrical Characteristics

COMP IN input level
(100 % modulation level)

Main (L+R) (Pre-Emphasis : OFF)	=245 mVrms
SUB (L–R) (dbX-TV : OFF)	=490 mVrms
Pilot	=49 mVrms
SAP Carrier	=147 mVrms
f_H	=15.734 kHz

(Ta=25 °C, V_{CC}=9 V)

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}			No signal				37	47	57	mA
2	Main output level	Vmain	MONO	19	Mono 1 kHz 100 % mod. Pre-em. on			43/44	440	490	540	mVrms
3	Main de-emphasis frequency characteristic	FCdeem	MONO	19	Mono 5 kHz 30 % mod. Pre-em. on	20 log ('5 k'/'1 k')		43/44	–1.2	0	1.0	dB
4	Main LPF frequency characteristic	FCmain	MONO	19	Mono 12 kHz 30 % mod. Pre-em.on	20 log ('12 k'/'1 k')		43/44	–3.0	–1.0	1.0	dB
5	Main distortion	THDm	MONO	19	Mono 1 kHz 100 % mod. Pre-em. on		15 kLPF	43/44	—	0.1	0.5	%
6	Main overload distortion	THDmmax	MONO	19	Mono 1 kHz 200 % mod. Pre-em off		15 kLPF	43/44	—	0.15	0.5	%
7	Main S/N	SNmain	MONO	19	Mono 1 kHz, Pre-em on	20 log ('100 %'/'0 %')	15 kLPF	43/44	61	69	—	dB
8	Sub output level	Vsub	ST	19	SUB (L-R), 1 kHz, 100 % mod., NR OFF			25	150	190	230	mVrms
9	Sub LPF frequency characteristic	FCsub	ST	19	SUB (L-R) 12 kHz, 30 % mod., NR OFF	20 log ('12 k'/'1 k')		25	–3.0	–0.5	1.0	dB
10	Sub distortion	THDsub	ST	19	SUB (L-R) 1 kHz, 100 % mod., NR OFF		15 kLPF	25	—	0.1	1.0	%
11	Sub overload distortion	THDsmax	ST	19	SUB (L-R), 1 kHz, 200 % mod., NR OFF		15 kLPF	25	—	0.2	2.0	%
12	Sub S/N	SNsub	ST	19	SUB (L-R) 1 kHz, NR OFF	20 log ('100 %'/'0 %')	15 kLPF	25	56	64	—	dB
13	ST → SAP Cross talk	CTst	SAP	19	SUB (L-R) 1 kHz, 100 % mod., NR ON SAP Carrier (5 f_H)	20 log ('NRSW=0'/ 'NRSW=1')	1 kBPF	44	60	70	—	dB
14	Sub pilot leak	PCsub	ST	19	PILOT (f_H) 0 dB	20 log ('out'/'in')	f_H BPF	25	—	–42	–30	dB

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
15	Stereo ON level	THst	ST	19	Change PILOT (f_H) Level	0 dB=49 mVrms		BUS RETURN	–9.0	–6.0	–3.0	dB
16	Stereo ON/OFF hysteresis	HYst				20 log ('on level'/'off level')			2.0	6.0	10.0	dB
17	SAP output level	Vsap1	SAP	19	SAP 1 kHz 100 % mod. NR OFF			28	150	190	230	mVrms
18		Vsap2			SAP 1 kHz 100 % mod. NR ON			43/44	370	490	610	mVrms
19	SAP LPF frequency characteristic	FCsap	SAP	19	SAP 10 kHz, 30 % mod. NR OFF	20 log ('10 k'/'1 k')		28	–3.0	0	2.5	dB
20	SAP distortion	THDsap1	SAP	19	SAP 1 kHz 100 % mod. NR OFF		15 kLPF	28	—	2.5	6.0	%
21		THDsap2			SAP 1 kHz 100 % mod. NR ON		15 kLPF	43/44	—	0.6	1.5	%
22	SAP S/N	SNsap	SAP	19	SAP 1 kHz, NR OFF	20 log ('100 %'/'0 %')	15 kLPF	28	46	55	—	dB
23	SAP soft mute	Smute	SAP	19	SAP 1 kHz, 100 % mod. NR OFF			28	–8.5	–7.0	–5.5	dB
24	dbx out noise level	Ndbx	SAP	—	No signal		15 kLPF	43/44	—	–75	–54	dBm
25	SAP → ST Cross talk	CTsap	ST	19	SAP 1 kHz, 100 % mod. NR ON, Pilot (f_H)	20 log ('NRSW=1' /'NRSW=0')	1 kBPF	44	60	70	—	dB
26	SAP ON level	THsap	SAP	19	Change SAP Carrier (5 f_H) Level	0 dB=147 mVrms		BUS RETURN	–12.0	–9.0	–6.5	dB
27	SAP ON/OFF hysteresis	HYsap				20 log ('on level'/'off level')			2.0	4.0	6.0	dB
28	ST separation 1 L → R	STLsep1	ST	19	ST-L 300 Hz 30 % mod. NR ON	20 log ('Lch'/'Rch')	15 kLPF	43/44	23	35	—	dB
29	ST separation 1 R → L	STRsep1	ST	19	ST-R 300 Hz 30 % mod. NR ON	20 log ('Rch'/'Lch')	15 kLPF	43/44	23	35	—	dB
30	ST separation 2 L → R	STLsep2	ST	19	ST-L 3 kHz 30 % mod. NR ON	20 log ('Lch'/'Rch')	15 kLPF	43/44	23	35	—	dB
31	ST separation 2 R → L	STRsep2	ST	19	ST-R 3 kHz 30 % mod. NR ON	20 log ('Rch'/'Lch')	15 kLPF	43/44	23	35	—	dB
32	TVOUT output level	Vtv	EXT	39/40	Sine wave 1 kHz, 490 mVrms	0 dB=490 mVrms		43/44	–0.5	0	0.5	dB

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
33	TVOUT cross talk	CTtv1	INT	39/40	Sine wave 1 kHz, 490 mVrms	0 dB=490 mVrms EXT → INT	1 kBPF	43/44	—	–75	–60	dB
34		CTtv2	EXT	19	MONO 1 kHz, 100 %, mod. Pre-em. on	0 dB=490 mVrms INT → EXT		43/44	—	–90	–80	dB
35	TVOUT muted amount	MUtv1	INT	19	MONO 1 kHz, 100 %, mod. Pre-em. on	20 log (M1="0"/M1="1") 0 dB=490 mVrms	1 kBPF	43/44	—	–85	–70	dB
36		MUtv2	EXT	39/40	Sine wave 1 kHz, 490 mVrms	20 log (M1="0"/M1="1") 0 dB=490 mVrms		43/44	—	–90	–75	dB
37	TVOUT DC offset	OStv	INT EXT	—	No signal	Mute (M1=0)/DC difference when there is no signal		43/44	–25	0	25	mV
38	TVOUT distortion	THDtv	EXT	39/40	Sine wave 1 kHz, 490 mVrms		15 kLPF	43/44	—	0.01	0.5	%
39	TVOUT S/N	SNtv	EXT	39/40	Sine wave 1 kHz, 490 mVrms/No signal	20 log ('490 mVrms'/'No signal')	15 kLPF	43/44	75	88	—	dB
40	TVOUT overload distortion	THDtvmax	EXT	39/40	Sine wave 1 kHz, 2 Vrms		15 kLPF	43/44	—	0.1	1.0	%
41	LSOUT output level	Vls1	INT	19	MONO 1 kHz, 100 %, mod. Pre-em. on	0 dB=490 mVrms		6/7	–0.9	0	0.9	dB
		Vls2	EXT	39/40 41/42	Sine wave 1 kHz, 490 mVrms	0 dB=490 mVrms						
42	LSOUT cross talk	CTls1	INT	39/40 41/42	Sine wave 1 kHz, 490 mVrms	0 dB=490 mVrms EXT → INT	1 kBPF	6/7	—	–75	–60	dB
43		CTls2	EXT	19	MONO 1 kHz, 100 %, mod. Pre-em. on	0 dB=490 mVrms INT → EXT		6/7	—	–90	–80	dB
44	LSOUT muted amount	MUls	EXT	39/40 41/42	Sine wave 1 kHz, 490 mVrms	20 log (M2="0"/M2="1") 0 dB=490 mVrms	1 kBPF	6/7	—	–90	–75	dB
45	LSOUT DC offset	OSls	INT EXT	—	No signal	Mute (M2=0)/DC difference when there is no signal		6/7	–25	0	25	mV
46	LSOUT distortion	THDls	EXT	39/40 41/42	Sine wave 1 kHz, 490 mVrms		15 kLPF	6/7	—	0.01	0.5	%
47	LSOUT S/N	SNls	EXT	39/40 41/42	Sine wave 1 kHz, 490 mVrms	20 log ('490 mVrms'/'No signal')	15 kLPF	6/7	75	88	—	dB
48	LSOUT overload distortion	THDlsmax	EXT	39/40 41/42	Sine wave 1 kHz, 2 Vrms		15 kLPF	6/7	—	0.1	1.0	%
49	BASS maximum value	TBmax	EXT	39/40 41/42	Sine wave 100 Hz, 245 mVrms	BASS="F" 0 dB=245 mVrms		6/7	11	12	13	dB
50	BASS minimum value	TBmin	EXT	39/40 41/42	Sine wave 100 Hz, 245 mVrms	BASS="0" 0 dB=245 mVrms		6/7	–13	–12	–11	dB

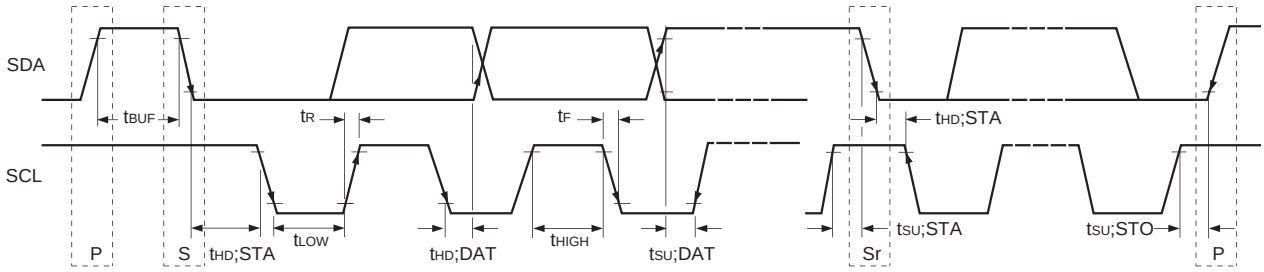
No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
51	TREBLE maximum value	TTmax	EXT	39/40 41/42	Sine wave 10 kHz, 245 mVrms	TREBLE="F" 0 dB=245 mVrms		6/7	11	12	13	dB
52	TREBLE minimum value	TTmin	EXT	39/40 41/42	Sine wave 10 kHz, 245 mVrms	TREBLE="0" 0 dB=245 mVrms		6/7	–13	–12	–11	dB
53	Volume minimum value	VOLmin	EXT	39/40 41/42	Sine wave 1 kHz, 490 mVrms	VOL-L="0", VOL-R="0" 0 dB=490 mVrms	1 kBPF	6/7	—	–90	–75	dB
54	SURROUT volume minimum value	SVOLmin	EXT	39/40 41/42	Sine wave 1 kHz, 490 mVrms	VOL-SURR="0" 0 dB=490 mVrms	1 kBPF	5	—	–90	–75	dB
55	SURROUND frequency characteristic 1	Sr1	EXT	40/42	Sine wave 330 Hz, 490 mVrms	SURR="1" 0 dB=490 mVrms		7	1.3	3.0	4.6	dB
56	SURROUND frequency characteristic 2	Sr2	EXT	40/42	Sine wave 10 kHz, 490 mVrms	SURR="1" 0 dB=490 mVrms		7	4.5	6.0	7.5	dB
57	VL limit level 1	VL1	EXT	39/40 41/42	Sine wave 1 kHz, 220 mVrms	VL="1"		6/7	175	220	265	mVrms
58	VL limit level 2	VL2	EXT	39/40 41/42	Sine wave 1 kHz, 1 Vrms	VL="1"		6/7	200	250	300	mVrms
59	TVOUT overload leak	Oltv	INT	19	Sine wave 1 kHz, 9 Vp-p	M1=M2="0"	1 kBPF	43/44	—	0.04	0.2	mVrms
60	LSOUT SURROUT overload leak	Olls	INT	19	Sine wave 1 kHz, 9 Vp-p	M1=M2="0" VOL-L=VOL-R= VOL-SURR="0"	1 kBPF	5/6/7	—	0.04	0.2	mVrms

I²C BUS block items (SDA, SCL)

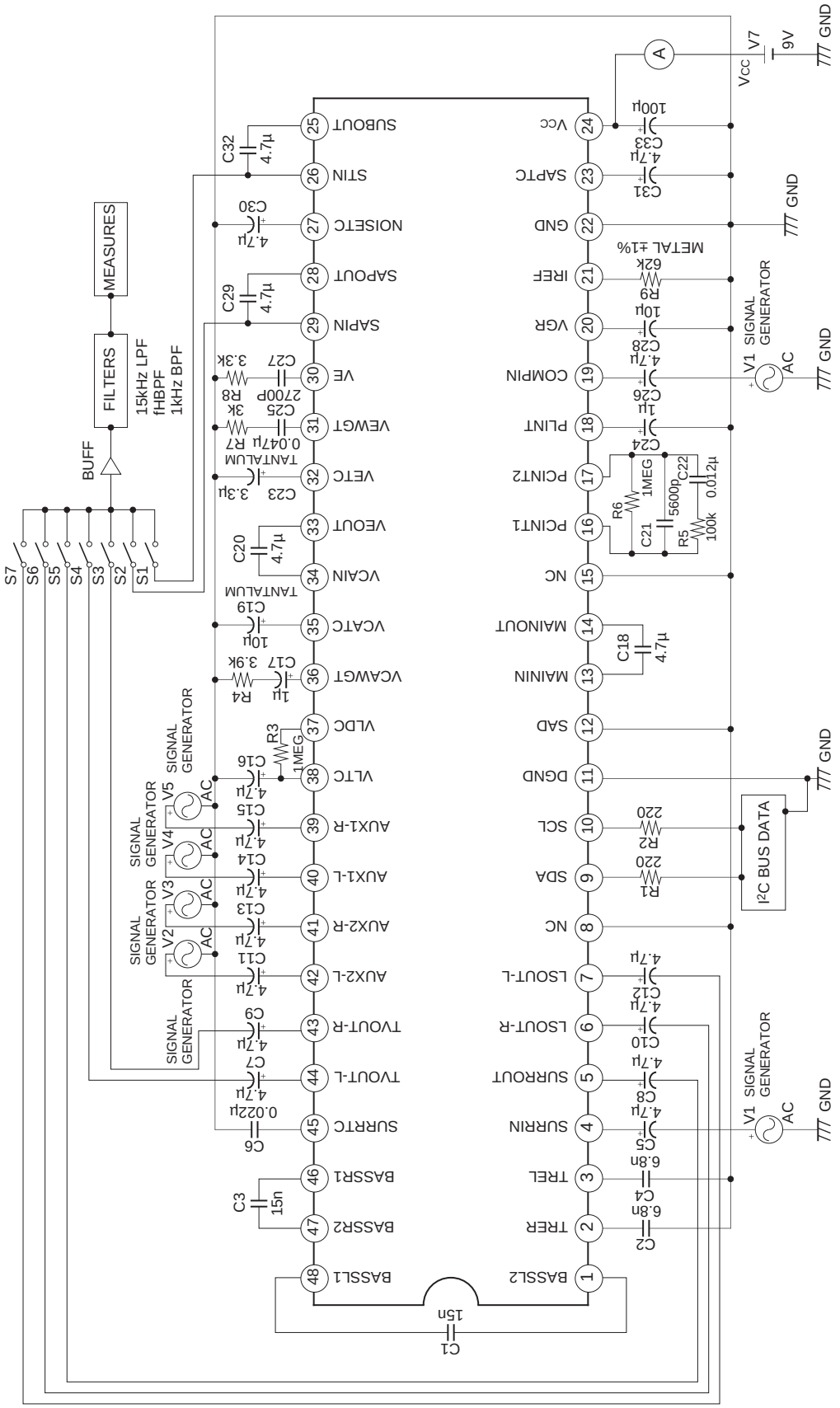
No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	
3	High level input current	I_{IH}	—	—	10	µA
4	Low level input current	I_{IL}	—	—	10	
5	Low level output voltage SDA (Pin 9) during 3 mA inflow	V_{OL}	0	—	0.4	V
6	Maximum inflow current	I_{OL}	3	—	—	mA
7	Input capacitance	C_I	—	—	10	pF
8	Maximum clock frequency	f_{SCL}	0	—	100	kHz
9	Minimum waiting time for data change	t_{BUF}	4.7	—	—	µs
10	Minimum waiting time for start of data transfer	t_{HD} : STA	4.0	—	—	
11	Low level clock pulse width	t_{LOW}	4.7	—	—	
12	High level clock pulse width	t_{HIGH}	4.0	—	—	
13	Minimum waiting time for start preparation	t_{SU} : STA	4.7	—	—	
14	Minimum data hold time	t_{HD} : DAT	0	—	—	
15	Minimum data preparation time	t_{SU} : DAT	250	—	—	ns
16	Rise time	t_R	—	—	1	µs
17	Fall time	t_F	—	—	300	ns
18	Minimum waiting time for stop preparation	t_{SU} : STO	4.7	—	—	µs

I²C BUS load conditions : Pull-up resistor 4 kΩ (Connect to +5 V)
Load capacity 200 pF (Connect to GND)

I²C BUS Control Signal



Electrical Characteristics Measurement Circuit



I²C BUS Register Data Standard Setting Values

Register	Number of bit	Classification	Standard setting	Contents	Setting value when electrical characteristics are measured
ATT	4	A	9	Center point	Adjustment point
VCO	6	A	1 F		
FILTER	6	A	1 F		
SPECTRAL	6	A	1 F		
WIDEBAND	6	A	1 F		
TEST-DA	1	T	0	Normal mode	
TEST1	1	T	0		
FST	1	T	0		
PR-VOL	4	U	F	F=0 dB	
VOL-L	6	U	3 F	3 F=0 dB	
VOL-R	6	U	3 F	3 F=0 dB	
VOL-SURR	6	U	3 F	3 F=0 dB	
TREBLE	4	U	8	7 or 8=0 dB	
BASS	4	U	8	7 or 8=0 dB	
NRSW	1	U	—	According to the modecontrol table	
FOMO	1	U	—		
FEXT1	1	U	0	AUX1 forced MONO OFF	
FEXT2	1	U	0	AUX2 forced MONO OFF	
VL	1	U	0	VL OFF	
SURR	1	U	0	Surround OFF	
SURRSW	1	U	0	Internal mode selection	
EXT1	1	U	0	TV decoder output selection	
EXT2	1	U	0		
M1	1	U	1	Mute OFF	
M2	1	U	1		
ATTSW	1	S	—	Fixed by the set specifications	
SAPC	1	S	—		

Classification A : Adjustment
U : User control
S : Proper to set
T : Test

List of Adjustment Contents

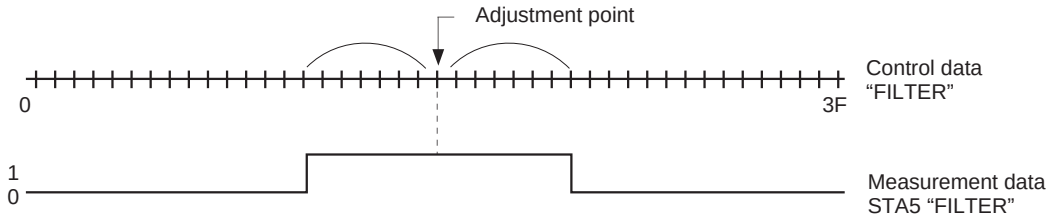
	Adjustment item	Adjustment data	Input pin	Input signal data	Measurement	Adjustment contents	Test mode setting
1	MAIN VCA	ATT	COMPIN (Pin 19)	100 Hz 245 mVrms	TVOUT-L output level	Adjust as close to 490 mVrms as possible	
2	ST & SAP VCO	VCO	None	None	TVOUT-R output frequency	Adjust as close to 62.936 kHz as possible	TEST-DA=1
3	ST & SAP & dbx FILTER	FILTER	COMPIN (Pin 19)	9.4 kHz 600 mVrms	STA5 (FILADJ)	Adjust to the center of the FILADJ=1 condition	TEST1=1
4	Low frequency ST separation	WIDEBAND	COMPIN (Pin 19)	ST-L 30 % 300 Hz	TVOUT-R output level	Minimize the output level	
	High frequency ST separation	SPECTRAL	COMPIN (Pin 19)	ST-L 30 % 3 kHz	TVOUT-R output level	Minimize the output level	

Adjustment Method (Adjust this through Tuner and IF when this IC is mounted on the set.)

1. ATT adjustment
   1) TEST BIT is set to “TEST1=0” and “TEST-DA=0”.
   2) Input a 100 Hz, 245 mVrms sine wave signal to COMPIN and monitor the TVOUT-L output level. Then, adjust the “ATT” data for ATT adjustment so that the TVOUT-L output goes to the standard value (490mVrms).
   3) Adjustment range : ±30 %
      Adjustment bits : 4 bits

2. Stereo, SAP VCO adjustment
   1) TEST BIT is set to “TEST1=0” and “TEST-DA=1”.
   2) Monitor the TVOUT-R output (4 f_H free running) frequency in a no input state, and adjust “VCO” adjustment data so that this frequency is as close to 4 f_H (62.936 kHz) as possible.
   3) Adjustment range : ±20 %
      Adjustment bits : 6 bits

3. Stereo, SAP, dbx filter adjustment
   1) TEST BIT is set to “TEST1=1” and “TEST-DA=0”.
   2) Input a 9.4 kHz, 600 mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA5) condition, adjust the “FILTER” adjustment data.
   3) Adjustment range : ±20 %
      Adjustment bits : 6 bits
      Align with the center of the STA5=1 (adjustment OK) condition range.



4. Separation adjustment
   1) TEST BIT is set to “TEST1=0” and “TEST-DA=0”.
   2) Set the unit to stereo mode and input the left channel only signal (modulation factor 30 %, frequency 300 Hz NR-ON) to COMPIN. At this time, adjust the “WIDEBAND” adjustment data to reduce TVOUT-R output to the minimum.
   3) Next, set the frequency only of the input signal to 3 kHz and adjust the “SPECTRAL” adjustment data to reduce TVOUT-R output to the minimum.
   4) Then, the adjustments in 2 and 3 above are performed to optimize the separation.
   5) “WIDEBAND” “SPECTRAL”
      Adjustment range : ±30 % Adjustment range: ±15 %
      Adjustment bits : 6 bits Adjustment bits: 6 bits

Description of Operation

The US audio multiplexing system possesses the base band spectrum shown in Fig. 1.

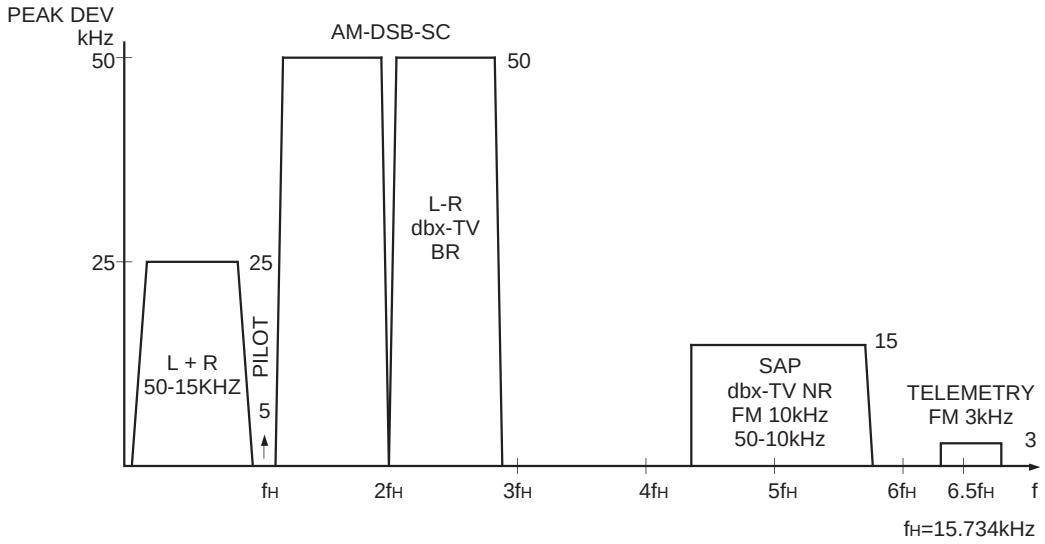


Fig. 1. Base band spectrum

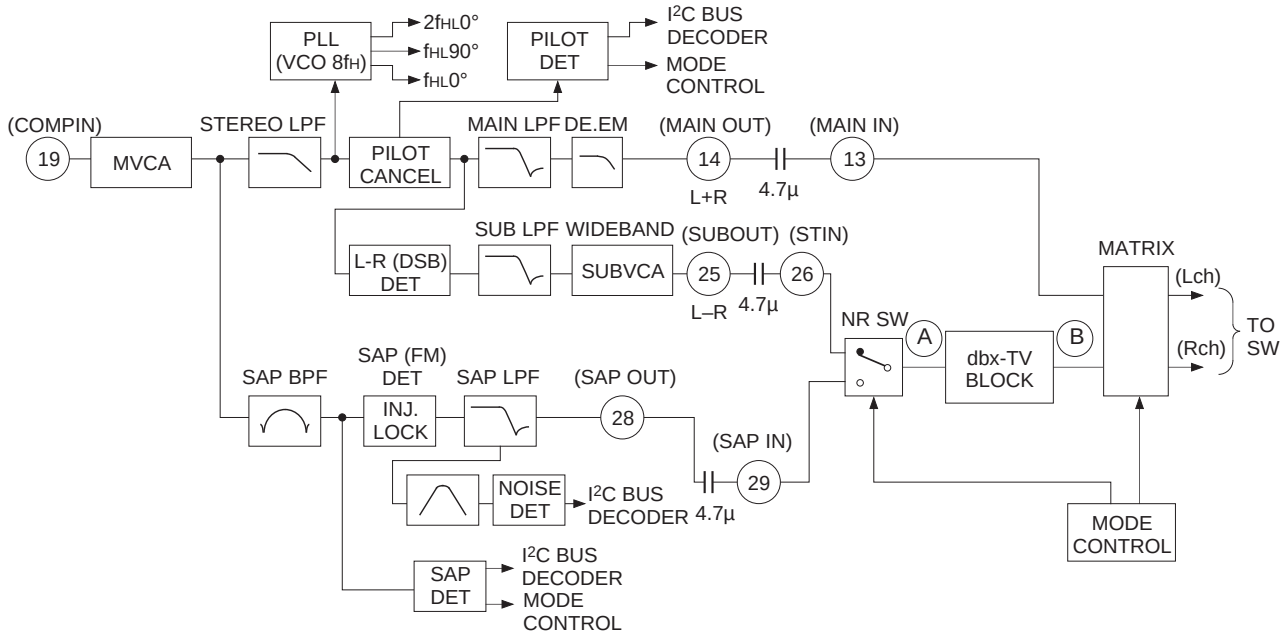


Fig. 2. Overall block diagram (See Fig. 3 for the dbx-TV block)

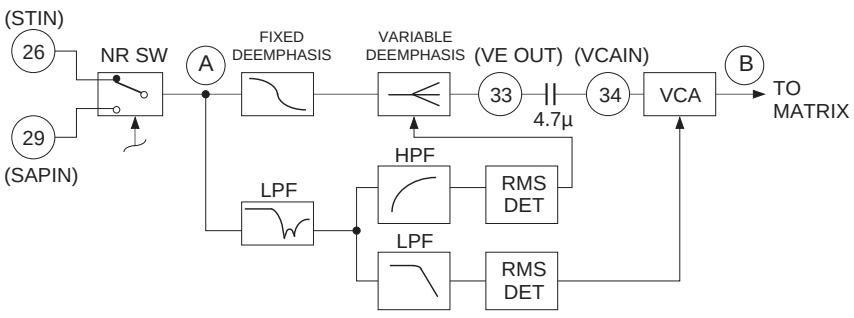


Fig 3. dbx-TV block

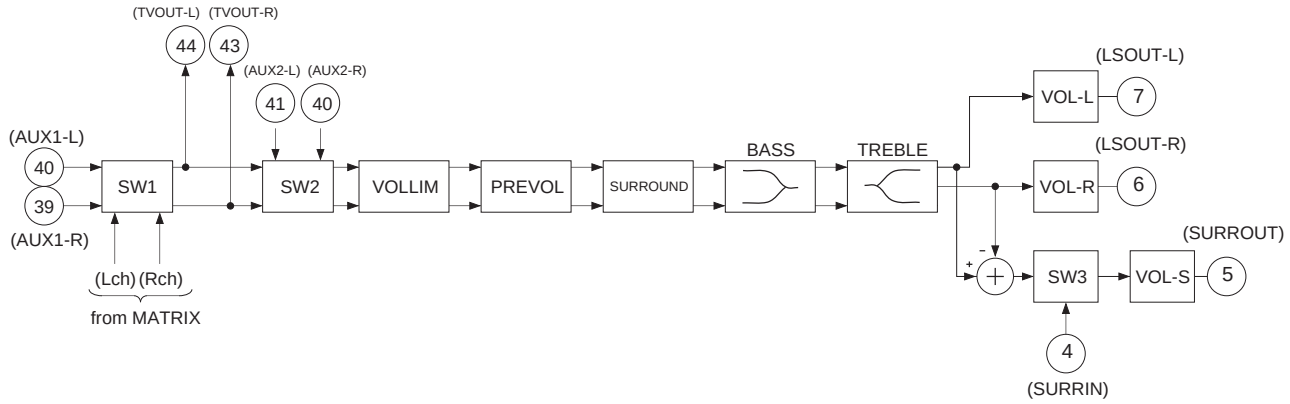


Fig. 4. Sound processor block

(1) L+R (MAIN)

After the audio multiplexing signal input from COMPIN (Pin 19) passes through MVCA, the SAP signal and telemetry signal are suppressed by STEREO LPF. Next, the pilot signals are canceled. Finally, the L-R signal and SAP signal are removed by MAIN LPF, and frequency characteristics are flattened (de-emphasized) and input to the matrix.

(2) L-R (SUB)

The L-R signal follows the same course as L+R before the pilot signal is canceled. L-R has no carrier signal, as it is a suppressed-carrier double-sideband amplitude modulated signal (DSB-AM modulated). For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for the demodulation of the L-R signal. In the last stage, the residual high frequency components are removed by SUB LPF and the L-R signal is input to the dbx-TV block via the NRSW circuit after passing through SUBVCA.

(3) SAP

SAP is an FM signal using 5 f_H as a carrier as shown in the Fig. 1. First, the SAP signal only is extracted using SAP BPF. Then, this is subjected to FM detection. Finally, residual high frequency components are removed and frequency characteristics flattened using SAP LPF, and the SAP signal is input to the dbx-TV block via the NRSW circuit. When there is no SAP signal, the Pin 28 output is soft muted.

(4) Mode discrimination

Stereo discrimination is performed by detecting the pilot signal amplitude. SAP discrimination is performed by detecting the 5 f_H carrier amplitude. NOISE discrimination is performed by detecting the noise near 25 kHz after FM detection of SAP signal.

(5) dbx-TV block

Either the SAP signal or L-R signal input respectively from ST IN (Pin 26) or SAP IN (Pin 29) is selected by the mode control and input to the dbx-TV block.

The input signal then passes through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The signal output from the variable de-emphasis circuit passes through an external capacitor and is applied to VCA (voltage control amplifier). Finally, the VCA output is converted from a current to a voltage using an operational amplifier and then input to the matrix.

The variable de-emphasis circuit transmittance and VCA gain are respectively controlled by Each of effective value detection circuits. Each of the effective value detection circuits passes the input signal through a predetermined filter for weighting before the effective value of the weighted signal is detected to provide the control signal.

(6) Matrix, SW1, SW2

The signals (L+R, L-R, SAP) input to "MATRIX" become the outputs for the ST-L, ST-R, MONO and SAP signals according to the BUS data and whether there is ST/SAP discrimination.

"SW1" switch the "MATRIX" output signal, external input signal (input to AUX1-L, R (Pins 40 and 39)) and external forced MONO.

"SW2" switch the "SW1" output signal, external input signal (input to AUX2-L, R (Pins 42 and 41)) and external forced MONO.

(7) Sound processor block

The sound processor block contains "VOLUME LIMITER", "PREVOL", "BASS/TREBLE" tone control functions, "SURROUND" (quasi-surround function) and "VOLUME".

VL : 250 mVrms (limit level)
BASS : ±12 dB (±1.7 dB/STEP at 100 Hz)
TREBLE : ±12 dB (±1.7 dB/STEP at 10 kHz)
VOLUME : 0 to –80 dB (–1.25 dB/STEP)

- Prevolume

"PREVOL" controls the input signal level of the sound processor block. When turning on the bass boost, treble boost or surround, attenuate the input signal to the sound processor block using "PREVOL" so that the signal is not dissipated inside the processor.

PR-VOL : 0 to –13.75 dB (–1.25 dB/STEP)

- Surround

At "SURROUND", the L and R differential components are phase-shifted and these components are added to the left and right channels.

When surround is OFF (SURR=0)
Inputs are output as is.

$$\begin{cases} Lout = Lin \\ Rout = Rin \end{cases}$$

When surround is ON (SURR=1)

$$\begin{cases} Lout = Lin - \dfrac{1-j\omega RC}{1+j\omega RC} \quad (Lin\text{-}Rin) \\ Rout = Rin + \dfrac{1-j\omega RC}{1+j\omega RC} \quad (Lin\text{-}Rin) \end{cases}$$

$$\begin{cases} R = 24\ k\Omega \text{ (IC on-chip)} \\ C = 0.022\ \mu F \text{ (Externally attached to Pin 45)} \end{cases}$$

(Lin, Lout) and (Rin, Rout) indicate the left- and right- channel I/O of the surround circuit.

(8) Others

"MVCA" is a VCA which adjusts the input signal level to the standard level of this IC.

"Bias" supplies the reference voltage and reference current to the other blocks. The current flowing to the resistor connecting IREF (Pin 21) with GND become the reference current.

Standard input and output levels

Input pin	Pin No.	Input level	TVOUT output level	LSOUT output level *3
COMPIN	19	245 mVrms *1	490 mVrms *2	490 mVrms *2
AUX1-L/AUX1-R	40/39	490 mVrms	490 mVrms	490 mVrms
AUX2-L/AUX2-R	42/41	490 mVrms	—	490 mVrms
SURRIN	4	490 mVrms	—	490 mVrms *4

*1 MONO, 25 kHz Deviation, Pre-Em. off

*2 MONO, 25 kHz Deviation, Pre-Em. on

*3 VOLUME MAX, PREVOL MAX, BASS & TREBLE CENTER, SURROUND OFF, VL OFF

*4 Only SURROUT output

Register Specifications

Slave address

SAD pin	SLAVE RECEIVER	SLAVE TRANSMITTER
GND	80 H	81 H
Vcc	8 AH	8 BH

Register table

SUB ADDRESS	DATA							
MSB LSB	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
****0000	*		TEST-DA	TEST1	ATT (4)			
****0001	*		VCO (6)					
****0010	*		FILTER (6)					
****0011	*		SPECTRAL (6)					
****0100	*		WIDEBAND (6)					
****0101	*	EXT1	EXT2	M2	NRSW	FOMO	SAPC	M1
****0110	*			ATTSW	SURRSW	FST	FEXT1	FEXT2
****0111	*		VL	SURR	PR-VOL (4)			
****1000	*		VOL-L (6)					
****1001	*		VOL-R (6)					
****1010	*		VOL-SURR (6)					
****1011	*				TREBLE (4)			
****1100	*				BASS (4)			

* : Don't care

Status Registers

When TEST1=0

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	—	—	—	—

When TEST1=1

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	FILADJ	—	—	—

Description of Registers

Control registers

Register	Number of bits	Classification*	Contents
ATT	4	A	Input level adjustment
VCO	6	A	STEREO VCO and SAP VCO free running frequency adjustment
FILTER	6	A	STEREO, SAP and dbx filter adjustment
SPECTRAL	6	A	Adjustment of stereo separation (3 kHz)
WIDEBAND	6	A	Adjustment of stereo separation (300 Hz)
TEST-DA	1	T	Turn to DAC test mode and STVCO adjustment mode by means of TEST-DA=1.
TEST1	1	T	Turn to test mode by means of TEST=1. (Adjustment of FILTER)
FST	1	T	Turn to forced stereo by means of FST=1.
PR-VOL	4	U	Input signal level control of sound processor block
VOL-L	6	U	LSOUT-L output signal level control
VOL-R	6	U	LSOUT-R output signal level control
VOL-SURR	6	U	SURROUT output signal level control
TREBLE	4	U	LSOUT output treble control
BASS	4	U	LSOUT output bass control
NRSW	1	U	Selection of the output signal (Stereo mode, SAP mode)
FOMO	1	U	Turn to forced MONO by means of FOMO=1. (Left channel only is MONO during SAP output.)
FEXT1	1	U	External input 1 forced MONO (1 : forced MONO ON)
FEXT2	1	U	External input 2 forced MONO (1 : forced MONO ON)
VL	1	U	Selection of volume limiter function ON/OFF (0 : OFF, 1 : ON)
SURR	1	U	Selection of quasi-surround function ON/OFF (0 : OFF, 1 : ON)
SURRSW	1	U	Selection of internal or external mode for SURROUT output
EXT1	1	U	Selection of TV mode or external input mode for TVOUT output
EXT2	1	U	Selection of internal mode or external input mode for LSOUT output
M1	1	U	Selection of TVOUT mute ON/OFF (0 : mute ON, 1 : mute OFF)
M2	1	U	Selection of LSOUT mute ON/OFF (0 : mute ON, 1 : mute OFF)
ATTSW	1	S	Turn the input stage MVCA off when ATTSW=1.
SAPC	1	S	Selection of SAP mode or L+R mode according to the presence of SAP broadcasting

*Classification U : User control
U : Adjustment
S : Proper to set
T : Test

Status registers

Register	Number of bits	Contents	
PONRES	1	POWER ON RESET detection;	1 : RESET
STEREO	1	Stereo discrimination of the COMPIN input signal;	1 : Stereo
SAP	1	SAP discrimination of the COMPIN input signal;	1 : SAP
NOISE	1	Noise level discrimination of the SAP signal;	1 : Noise
FILADJ	1	Status of FILTER adjustment;	1 : OK range

Description of Control Registers

ATT (4) : Adjust the signal level input to COMPIN (Pin 19) to the standard input level.
Variable range of the input signal : 245 mVrms –5.0 dB to +3.0 dB
0 = Level min.
F = Level max.

VCO (6) : Adjust STEREO & SAP VCO free running frequency (fo).
Variable range : fo ±20 %
0 = Free running frequency min.
3F = Free running frequency max.

FILTER (6) : Adjust the filter fo of the ST, SAP and dbx blocks.
Variable range : fo ±20 %
0 = Frequency min.
3F = Frequency max.

SPECTRAL (6) : Perform high frequency (fs=3 kHz) separation adjustment.
0 = Level max.
3F = Level min.

WIDEBAND (6) : Perform low frequency (fs=300 Hz) separation adjustment.
0 = Level min.
3F = Level max.

TEST-DA (1) : Set DAC output test mode and VCO adjustment mode.
0 = Normal mode
1 = DAC output test mode and STVCO adjustment mode
In addition, the following outputs are present at Pins 44 and 43.
TVOUT-L (Pin 44) : DA control DC level
TVOUT-R (Pin 43) : STEREO VCO oscillation frequency ($4f_H$)

TEST1 (1) : Set filter adjustment mode.
0 = Normal mode
1 = FILTER (STA5) adjustment mode
In addition, the following outputs are present at Pins 44 and 43.
TVOUT-L (Pin 44) : SAP BPF OUT
TVOUT-R (Pin 43) : NR BPF OUT

FST (1) : Select forced STEREO mode
0 = Normal mode
1 = Forced stereo mode

PR-VOL (4) : Input signal level control of sound processor block
When turning on the bass boost, treble boost or surround, attenuate the input signal to the sound processor block using “PR-VOL” so that the signal is not dissipated inside the processor.
4 = Volume Min. (–13.75 dB)
F = Volume Max. (0 dB)
–1.25 dB/STEP

VOL-L (6) : LSOUT-L output signal level control
0 = Volume Min. (–80 dB)
3F = Volume Max. (0 dB)
–1.25 dB/STEP

VOL-R (6) : LSOUT-R output signal level control
0 = Volume Min. (–80 dB)
3F = Volume Max. (0 dB)
–1.25 dB/STEP

VOL-SURR (6) : SURROUT output signal level control
0 = Volume Min. (–80 dB)
3F = Volume Max. (0 dB)
–1.25 dB/STEP

TREBLE (4) : LSOUT output treble control
0 = Treble Min.
7 & 8 = Treble Center (0 dB)
F = Treble Max.

BASS (4) : LSOUT output bass control
0 = Bass Min.
7 & 8 = Bass Center (0 dB)
F = Bass Max.

NRSW (1) : Select stereo mode or SAP mode
0 = Stereo mode
1 = SAP mode

FOMO (1) : Select forced MONO mode
0 = Normal mode
1 = Forced MONO mode

FEX1 (1) : Turn external input [1] to forced MONO.
0 = Normal mode
1 = External input [1] is forced MONO.
Input the same signal to both AUX1-L and AUX1-R.

FEX2 (1) : Turn external input [2] to forced MONO.
0 = Normal mode
1 = External input [2] is forced MONO.
Input the same signal to both AUX2-L and AUX2-R.

VL (1) : Volume limiter function selection
0 = Volume limiter OFF
1 = Volume limiter ON

SURR (1) : Surround function selection
0 = Surround OFF
1 = Surround ON

SURRSW (1) : Select INT mode or EXT mode for SURROUT output
0 = INT mode
1 = EXT mode

EXT1 (1) : Select TV mode or external input mode for TVOUT output.
0 = TV mode
1 = External input mode

EXT2 (1) : Select internal mode or external input mode for LSOUT output.
0 = internal mode
1 = External input mode

M1 (1) : Mute the TVOUT-L and TVOUT-R output.
0 = Mute ON
1 = Mute OFF

M2 (1) : Mute the LSOUT-L and LSOUT-R output.
0 = Mute ON
1 = Mute OFF

ATTSW (1) : Select BYPASS SW of Main VCA
0 = Normal mode
1 = Main VCA is passed

SAPC (1) : Select the SAP signal output mode
When there is no SAP signal, the conditions for selecting SAP output are selected by SAPC.
0 = L+R output is selected
1 = SAP output is selected

Description of Mode Control

Priority ranking : M1/M2 > EXT1/EXT2 > TEST-DA > TEST1 > (NRSW & FOMO & SAPC)

Mode control	SAPC=0	SAPC=1
NRSW	"Select dbx input and TV decoder output" Conditions : FOMO = 0 NRSW=0 (MONO or ST output) • During ST input : left channel: L, right channel: R • During other input : left channel: L+R, right channel: L+R NRSW=1 (SAP output) • When there is "SAP" during SAPdiscrimination –left channel : SAP, right channel : SAP • When there is "No SAP", output is the same as when NRSW=0.	"Select dbx input and TV decoder output" Conditions : FOMO = 0 NRSW=0 (MONO or ST output) As on the left NRSW = 1 (SAP output) • Regardless of the presence of SAP discrimination, dbx input : "SAP" left channel : SAP, right channel : SAP However, when there is no SAP, SAPOUT output is soft muted (–7 dB)
FOMO	"Forced MONO" FOMO=1 • During SAP output: left channel : L+R, right channel : SAP • During ST or MONO output: left channel : L+R, right channel : L+R	
SAPC	Change the selection conditions for "MONO or ST output" and "SAP output". SAPC=0 : Switch to SAP output when there is SAP discrimination. Do not switch to SAP output when there is no SAP discrimination. SAPC=1 : Switch to SAP output regardless of whether there is SAP discrimination.	
M1/M2	"MUTE" M1=0 : TVOUT output is muted. M2=0 : LSOUT output is muted.	
EXT1/EXT2	"TV mode/external input mode selection" EXT1=0 : Set TVOUT output to TV mode. EXT1=1 : Set TVOUT output to external input [1] mode. EXT2=0 : Set LSOUT output to internal mode. EXT2=1 : Set LSOUT output to external input [2] mode.	
TEST1	"TEST1" TEST1=1 Return adjustment data with STATUS REGISTER as an adjustment mode. In addition, outputs are as follows. left channel : SAP BPF OUT right channel : NR BPF OUT	
TEST-DA	"TEST-DA" TEST-DA=1 Used to adjust the D/A TEST and STVCO. left channel : D/A output right channel : STVCO oscillation frequency ($4f_H$)	

Decoder Output and Mode Control Table 1 (SAPC=1)

Input signal mode	Mode detection			Mode control			dbx	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC	input	Lch	Rch
MONO [1)]	0	0	0	0	*	1	MUTE	L+R	L+R
	0	0	0	1	0	1	SAP	SAP	SAP
	0	0	0	1	1	1	SAP	L+R	SAP
	0	*	1	0	*	1	MUTE	L+R	L+R
	0	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	*	1	1	1	1	(SAP)	L+R	(SAP)
STEREO [1)]	1	0	*	0	0	1	L-R	L	R
	1	0	*	0	1	1	MUTE	L+R	L+R
	1	1	1	0	0	1	L-R	L	R
	1	1	1	0	1	1	MUTE	L+R	L+R
	1	0	0	1	0	1	SAP	SAP	SAP
	1	0	0	1	1	1	SAP	L+R	SAP
	1	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	*	1	1	1	1	(SAP)	L+R	(SAP)
MONO & SAP	0	1	*	0	0	1	MUTE	L+R	L+R
	0	1	*	0	1	1	MUTE	L+R	L+R
	0	1	0	1	0	1	SAP	SAP	SAP
	0	1	0	1	1	1	SAP	L+R	SAP
	0	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	1	(SAP)	L+R	(SAP)
STEREO & SAP	1	1	*	0	0	1	L-R	L	R
	1	1	*	0	1	1	MUTE	L+R	L+R
	1	1	0	1	0	1	SAP	SAP	SAP
	1	1	0	1	1	1	SAP	L+R	SAP
	1	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	1	(SAP)	L+R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately –7 dB).
The signal is soft muted when NOISE=1.

* : Don't care.

1) : SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Decoder Output and Mode Control Table 2 (SAPC=0)

Input signal mode	Mode detection			Mode control			dbx	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC	input	Lch	Rch
MONO [1)]	0	0	*	*	*	0	MUTE	L+R	L+R
	0	1	1	0	0	0	MUTE	L+R	L+R
	0	1	1	0	1	0	MUTE	L+R	L+R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L+R	(SAP)
STEREO [1)]	1	0	*	0	0	0	L-R	L	R
	1	0	*	0	1	0	MUTE	L+R	L+R
	1	0	*	1	0	0	L-R	L	R
	1	0	*	1	1	0	MUTE	L+R	L+R
	1	1	1	0	0	0	L-R	L	R
	1	1	1	0	1	0	MUTE	L+R	L+R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L+R	(SAP)
MONO & SAP	0	1	0	0	0	0	MUTE	L+R	L+R
	0	1	0	0	1	0	MUTE	L+R	L+R
	0	1	0	1	0	0	SAP	SAP	SAP
	0	1	0	1	1	0	SAP	L+R	SAP
	0	1	1	0	0	0	MUTE	L+R	L+R
	0	1	1	0	1	0	MUTE	L+R	L+R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L+R	(SAP)
STEREO & SAP	1	1	0	0	0	0	L-R	L	R
	1	1	0	0	1	0	MUTE	L+R	L+R
	1	1	0	1	0	0	SAP	SAP	SAP
	1	1	0	1	1	0	SAP	L+R	SAP
	1	1	1	0	0	0	L-R	L	R
	1	1	1	0	1	0	MUTE	L+R	L+R
	1	1	1	1	0	0	(SAP)	SAP	(SAP)
	1	1	1	1	1	0	(SAP)	L+R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately –7 dB).
The signal is soft muted when NOISE=1.

* : Don't care.

1) : SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Mode Control Table 3

EXT1	EXT2	FEXT1	FEXT2	M1	M2	TV OUT-L	TV OUT-R	LS OUT-L	LS OUT-R
0	0	*	*	1	1	TV-L	TV-R	TV-L	TV-R
1	0	0	*	1	1	AUX1-L	AUX1-R	AUX1-L	AUX1-R
1	0	1	*	1	1	AUX1-L	AUX1-L	AUX1-L	AUX1-L
*	1	*	0	1	1	Selected according to the EXT1, FEXT1 conditions	Selected according to the EXT1,FEXT1, conditions	AUX2-L	AUX2-R
*	1	*	1	1	1	Selected according to the EXT1, FEXT1 conditions	Selected according to the EXT1,FEXT1, conditions	AUX2-L	AUX2-L
*	*	*	*	0	1	MUTE	MUTE	Selected according to the EXT2, FEXT2, conditions	Selected according to the EXT2, FEXT2, conditions
*	*	*	*	1	0	Selected according to the EXT1, FEXT1 conditions	Selected according to the EXT1,FEXT1, conditions	MUTE	MUTE

TV-L/TV-R are selected in Matrix.

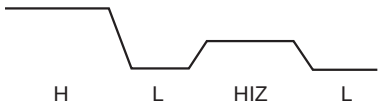
TV-L : MONO, ST-L, SAP (SAPBFout, D/A out)

TV-R : MONO, ST-R, SAP (NRBPFout, STVCO free run ($4f_H$))

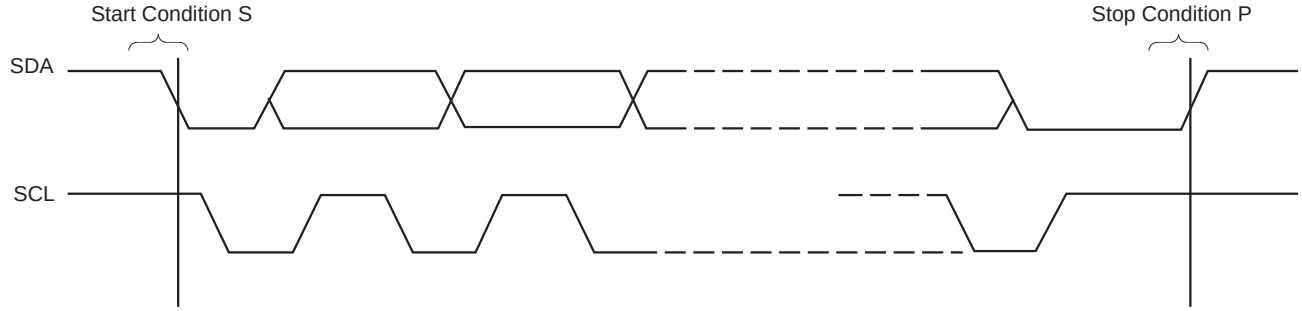
I²C BUS Signal

There are two I²C signals, SDA (Serial DATA) and SCL (Serial CLOCK) signals. SDA is a bidirectional signal.

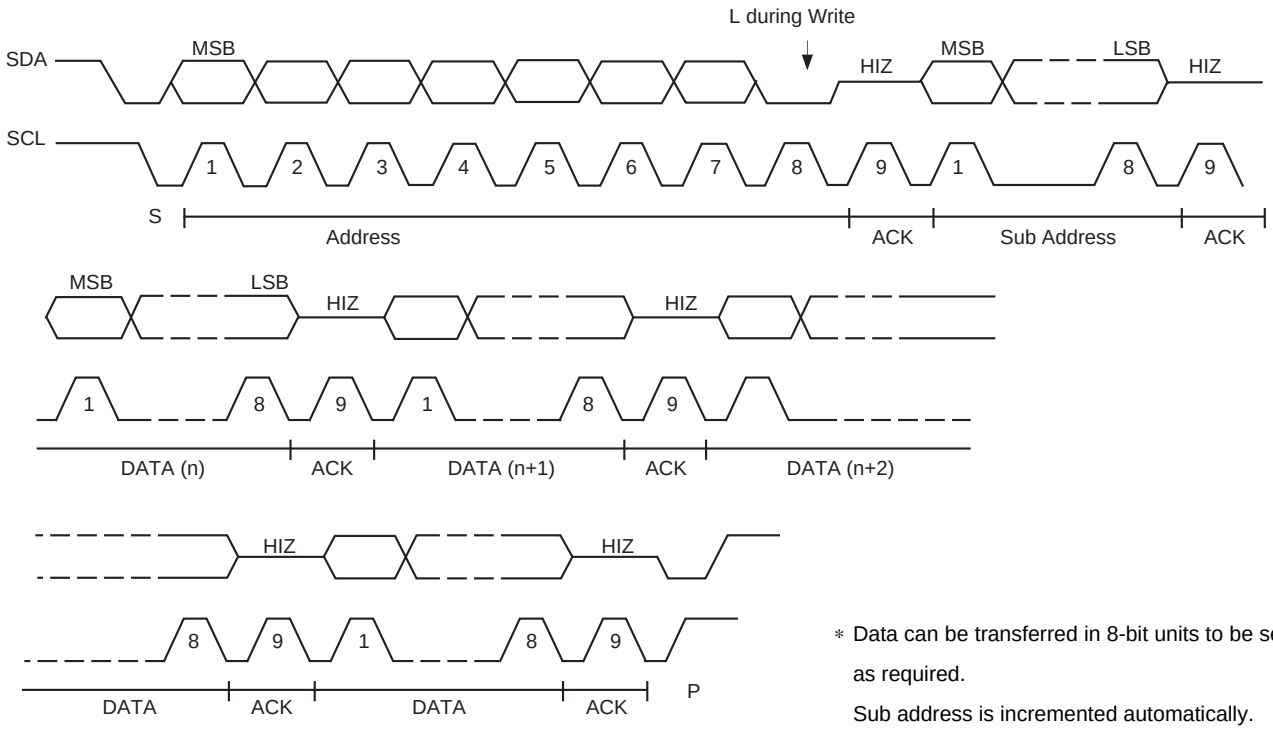
- Accordingly there are 3 values outputs, H, L and HIZ.



- I²C transfer begins with Start Condition and ends with Stop Condition.

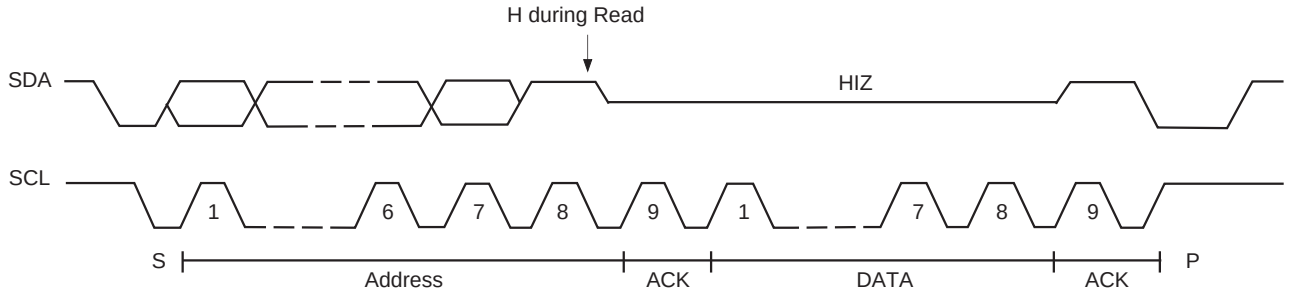


• **I²C data Write** (Write from I²C controller to the IC)

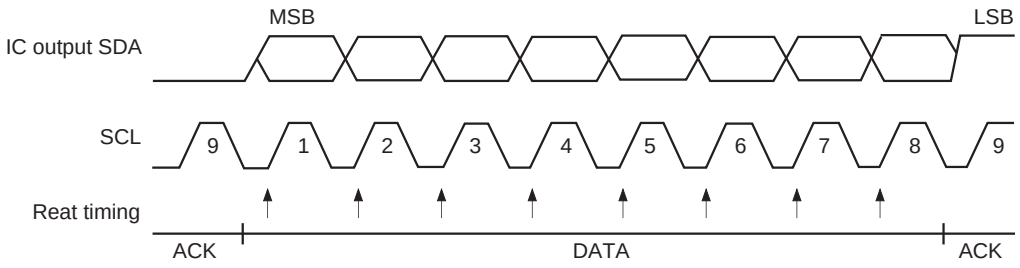


∗ Data can be transferred in 8-bit units to be set as required.
Sub address is incremented automatically.

• **I²C data Read** (Read from the IC to I²C controller)

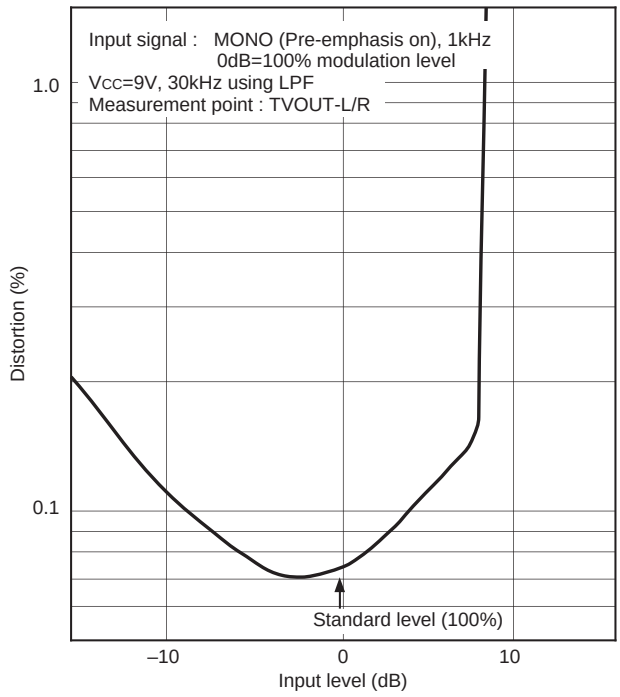


• **Read timing**

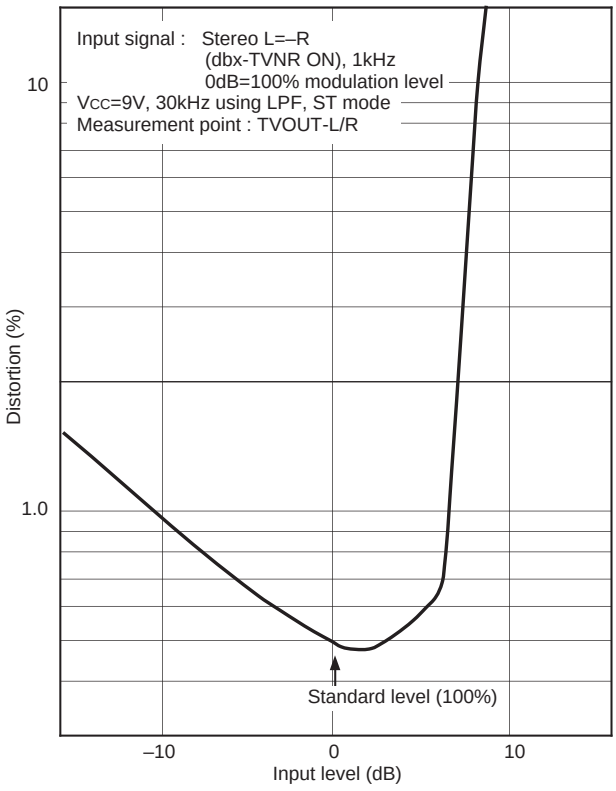


∗ Data Read is performed during SCL rise.

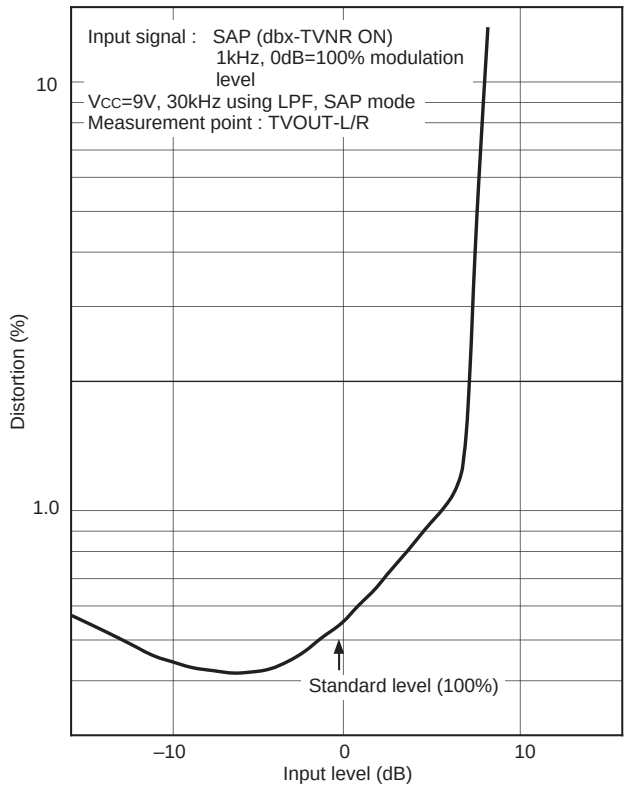
Input level vs. Distortion characteristics 1 (MONO)



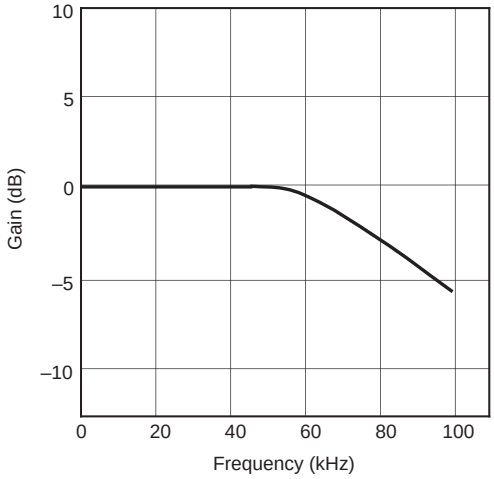
Input level vs. Distortion characteristics 2 (Stereo)



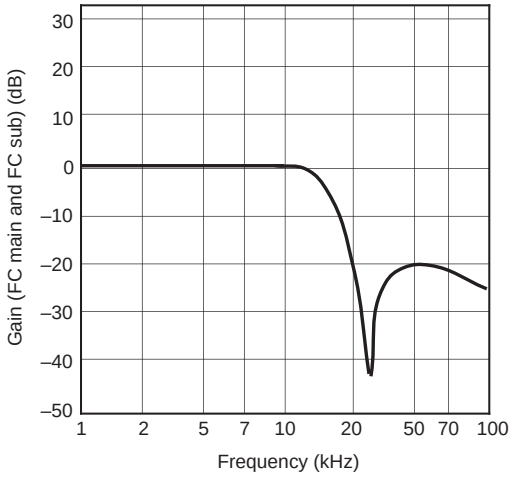
Input level vs. Distortion characteristics 3 (SAP)



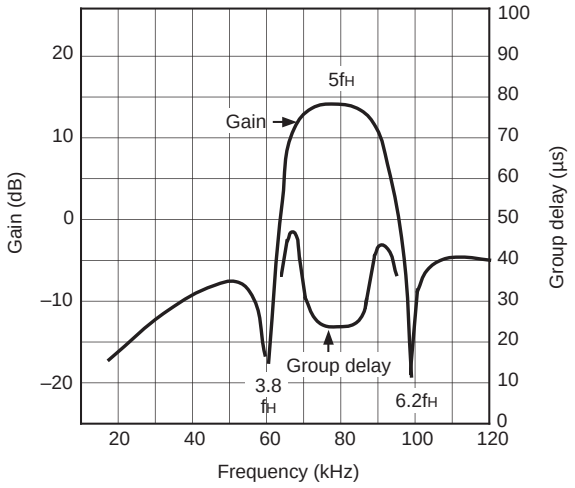
Stereo LPF frequency characteristics



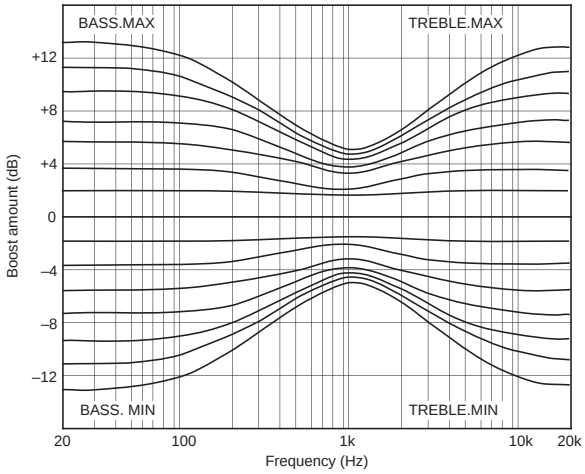
Main LPF and Sub LPF frequency characteristics



SAP frequency characteristics and group delay

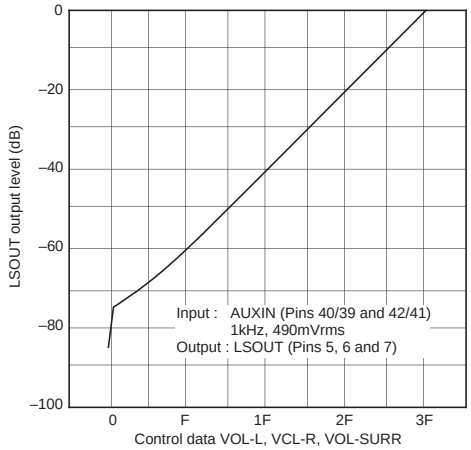


BASS - TREBLE characteristics

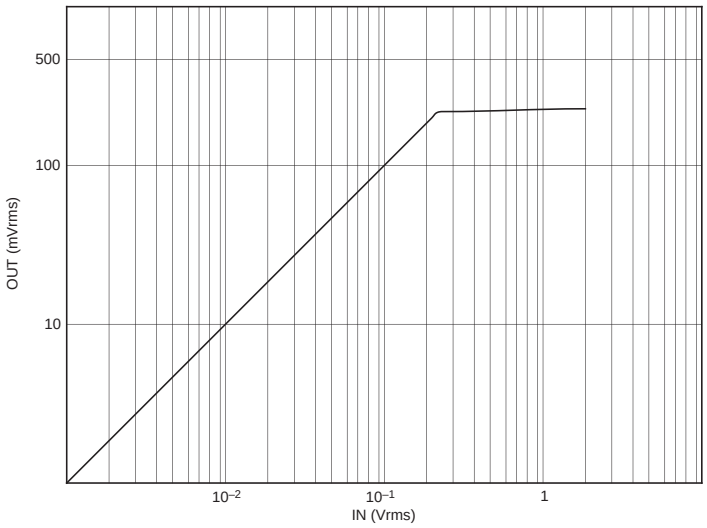


Input : AUXIN (Pins 40/39 and 42/41) 245 mVrms
Output : LSOUT (PINS 5, 6 and 7)

Volume characteristics

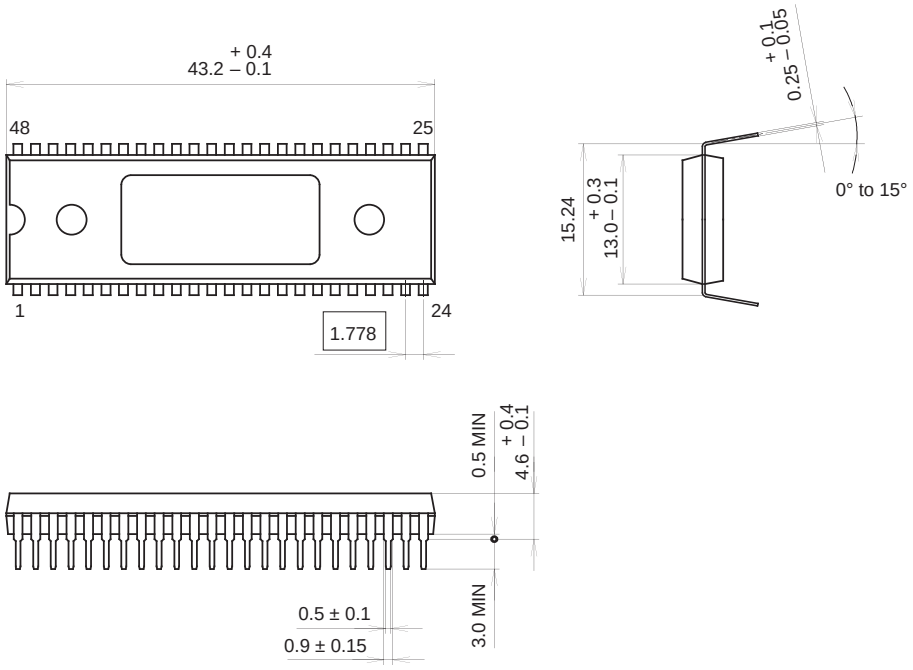


Volume limiter characteristics



Package Outline Unit : mm

48PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.Center part is mirror surface.

SONY CODE	SDIP-48P-02
EIAJ CODE	SDIP048-P-0600
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	5.1g