SONY

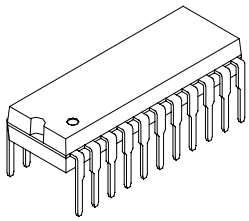
CXA2093S

Sharpness for Display

Description

The CXA2093S is a bipolar IC which performs contour accentuation for display RGB signals.

22 pin SDIP (Plastic)



Features

- Sharpness time constant selection (50ns/100ns)
- Built-in sync separator for sync on green
- Differential output pins
- Built-in wide-band amplifier (200MHz/–3dB@0.7Vp-p)

Applications

Display

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

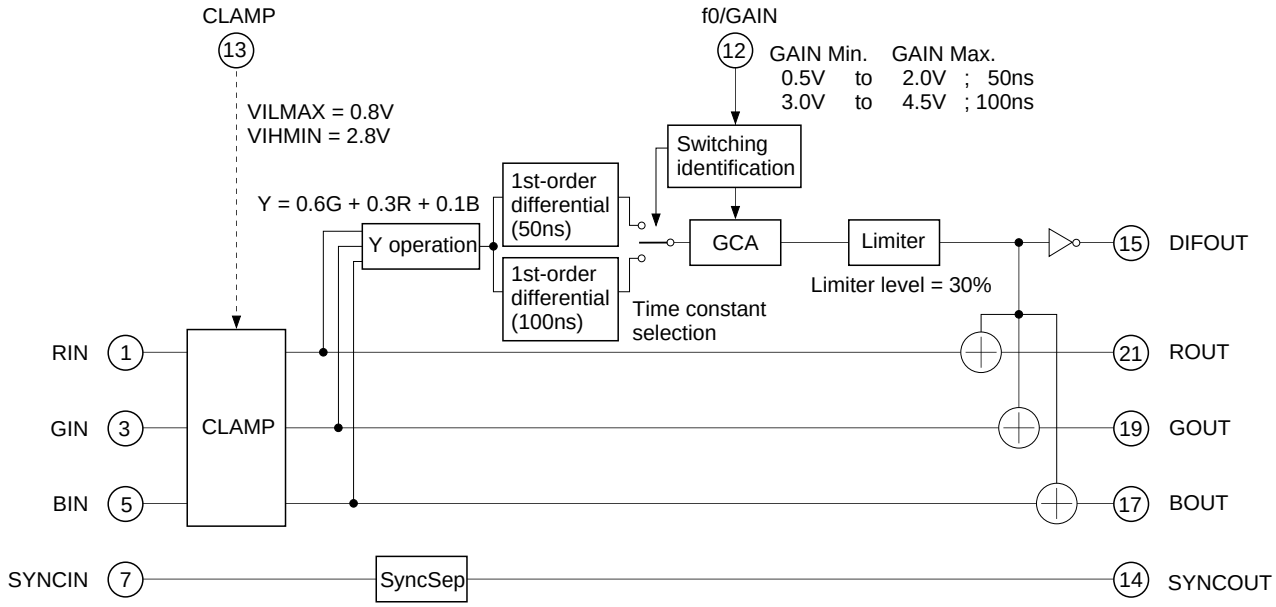
• Supply voltage	V_{CC}	7	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.13	W

Operating Conditions

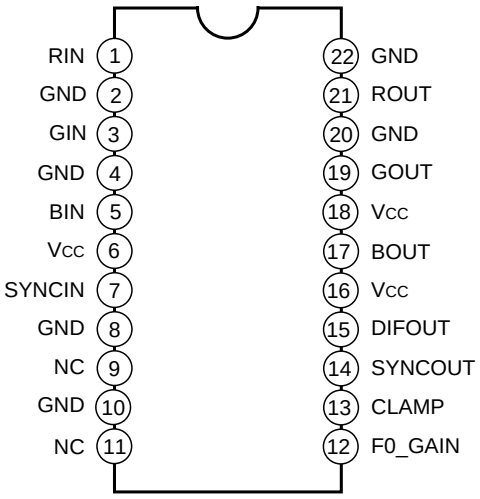
Supply voltage	V_{CC}	5 ± 0.25	V

E97680A26-PS

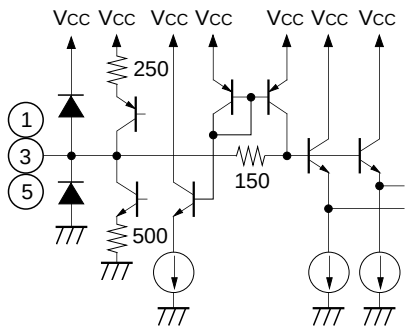
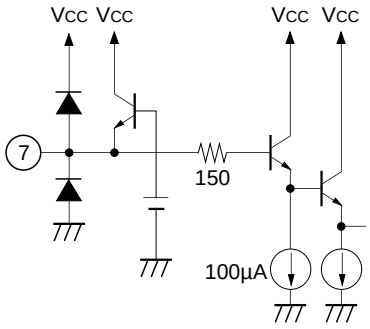
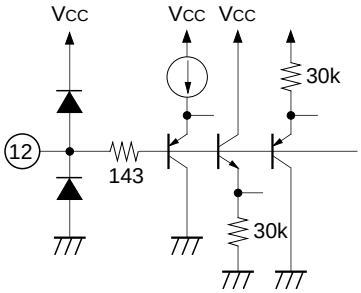
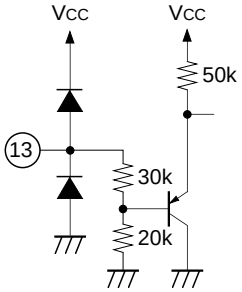
Block Diagram

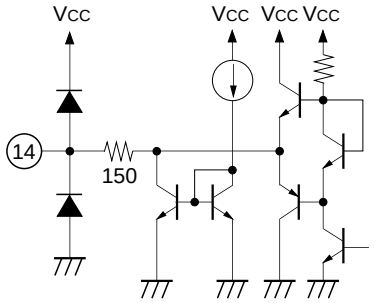
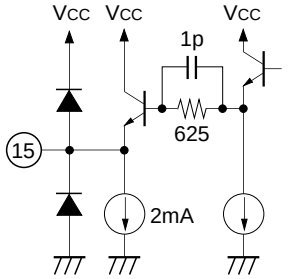
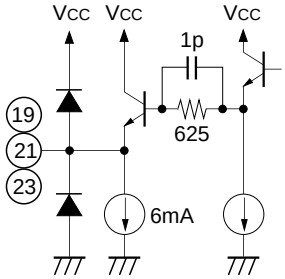


Pin Configuration

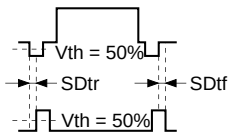


Pin Description

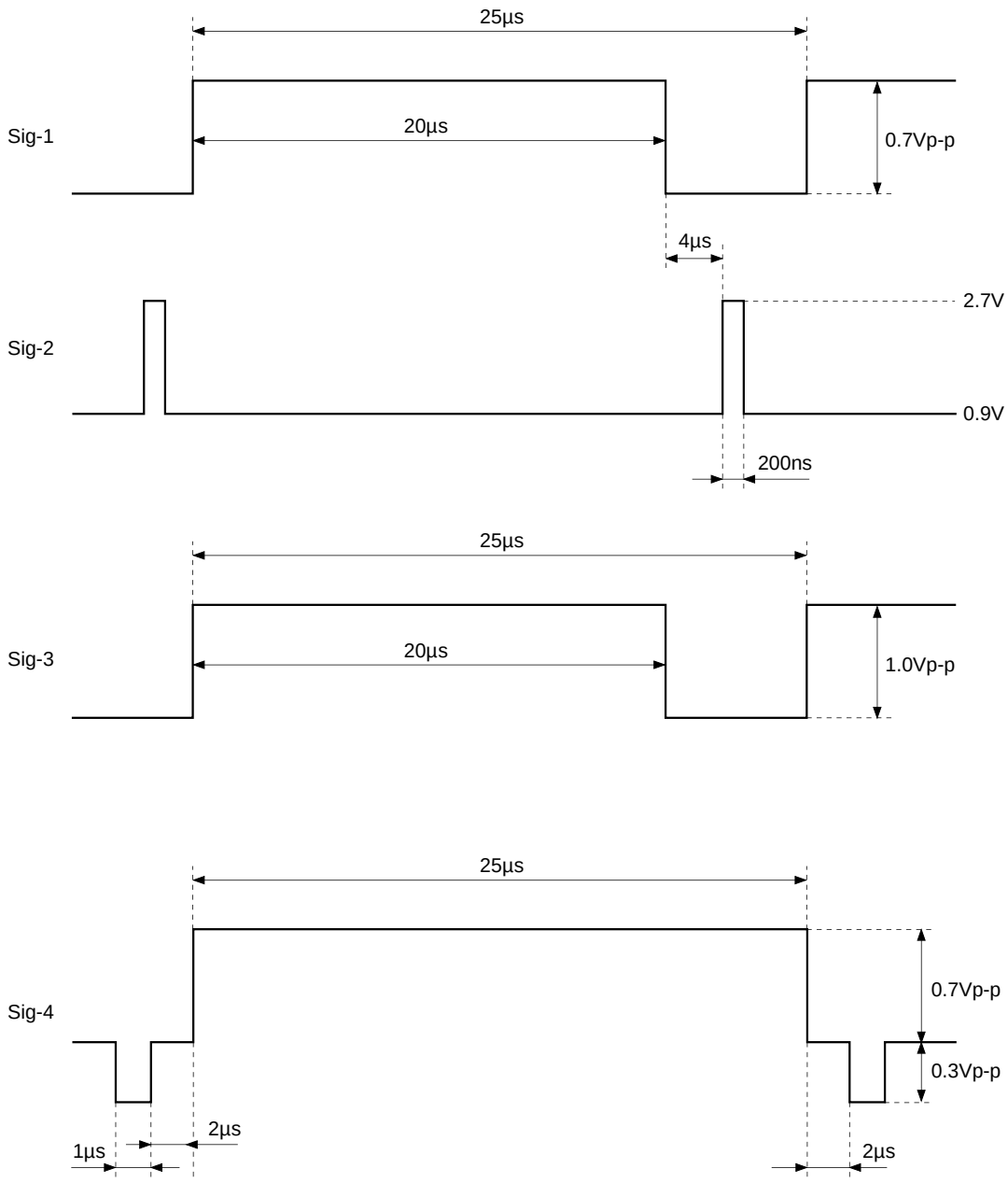
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 3 5	RIN GIN BIN			RGB input pins. Input these pins through capacitor.
2, 4 8, 10 20, 22	GND			GND pins.
7	SYNCIN			Sync input pin for sync on green. Input this pin through capacitor.
12	F0_GAIN			Sharpness time constant selection and gain control pin.
13	CLAMP			Clamp pulse input pin. ILMAX; 0.8V IHMIN; 2.8V

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	SYNCOUT			Sync output pin. 0 to 4.3V positive polarity pulse is output in synchronizing with sync.
15	DIFOUT			Differential signal output pin.
6, 16 18, 20	V_{CC}	5V (applied)		Power supply pins.
19 21 23	BOUT GOUT ROUT			RGB signal output pins.

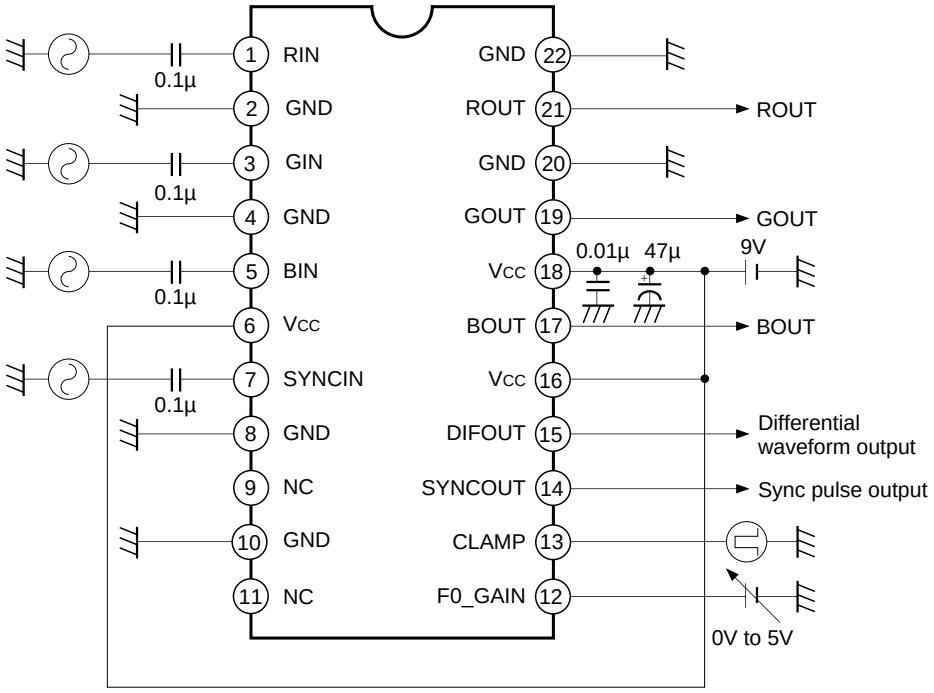
Electrical Characteristics (Ta = 25°C, Vcc = 5V)

No.	Item	Symbol	Measure-ment pins	Input signals	Measurement contents	Min.	Typ.	Max.	Unit
1	Power consumption	Icc	6 16 18		Vcc pin inflow current	45	69	95	mA
2	I/O gain R	VGR	21	Pins 1, 3, 5: Sig-1 Pin 13: Sig-2	Input video signal to Pins 1, 3 and 5, input clamp pulse to Pin 13, and measure the output amplitude of each output pin. Then calculate the I/O gain. $VGR = 20 \log \frac{\text{output amplitude}}{0.7}$	–0.5	0.5	1.5	dB
3	I/O gain G	VGG	19			–0.5	0.5	1.5	dB
4	I/O gain B	VGB	17			–0.5	0.5	1.5	dB
5	Input dynamic range	Drng	17 19 21	Pins 1, 3, 5: Sig-3 Pin 13: Sig-2	Input video signal to Pins 1, 3 and 5, input clamp pulse to Pin 13, and measure the output amplitude of each output pin.	0.9	1.05	1.2	Vp-p
6	Sharpness gain 1	VSG1	19	Pins 1, 3, 5: CW Pin 13: 5 V Pin 12: 0.5 V	Input 30MHz and 0.1Vp-p sine wave to Pins 1, 3 and 5, and measure the output amplitude of Pin 19.	60	110	150	mVp-p
7	Sharpness gain 2	VSG2	19	Pins 1, 3, 5: CW Pin 13: 5 V Pin 12: 2.5 V	Input 30MHz and 0.1Vp-p sine wave to Pins 1, 3 and 5, and measure the output amplitude of Pin 19. Then calculate the I/O gain. $VGR = 20 \log \frac{\text{output amplitude}}{0.1}$	5.0	7.0	9.0	dB
8	Sharpness gain 3	VSG3	19	Pins 1, 3, 5: CW Pin 13: 5 V Pin 12: 3.0 V	Input 30MHz and 0.1Vp-p sine wave to Pins 1, 3 and 5, and measure the output amplitude of Pin 19.	60	110	150	mVp-p
9	Sharpness gain 4	VSG4	19	Pins 1, 3, 5: CW Pin 13: 5 V Pin 12: 4.5 V	Input 30MHz and 0.1Vp-p sine wave to Pins 1, 3 and 5, and measure the output amplitude of Pin 19. Then calculate the I/O gain. $VGR = 20 \log \frac{\text{output amplitude}}{0.1}$	5.0	7.0	9.0	dB
10	DIFOUT output level	VDF	15	Pin 1: CW Pin 13: 5 V Pin 12: 4.5 V	Input 30MHz and 0.3Vp-p sine wave to Pin 1, and measure the output amplitude of Pin 15.	290	375	455	mVp-p
11	SYNCSEP output high level	VSHi	14	Pin 7: Sig-4	Input video signal to Pin 7, and measure the high level of Pin 14.	3.9	4.2	4.5	V
12	SYNCSEP output low level	VSLo			Input video signal to Pin 7, and measure the low level of Pin 14.	0.1	0.18	0.26	V
13	SYNCSEP output delay 1	SDtr				0	19	40	ns
14	SYNCSEP output delay 1	SDtf				30	51	70	ns

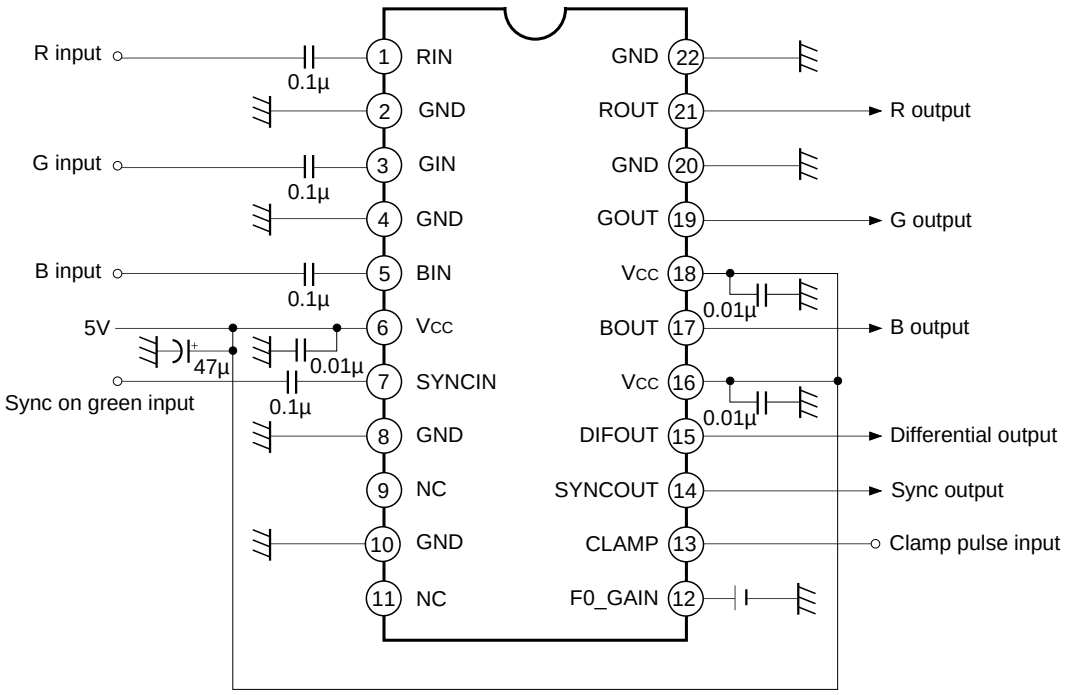
Signals Used for Measurement



Electrical Characteristics Measurement Circuit



Application Circuit

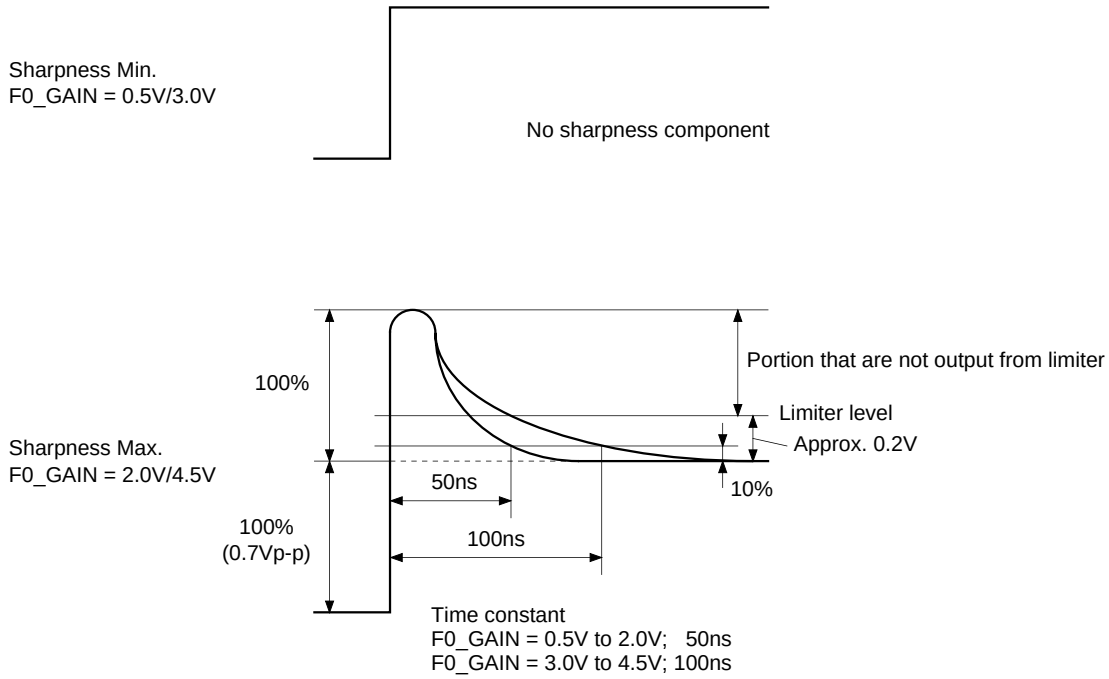


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Video signal system

RGB signals input to Pins 1, 3 and 5 is synchronous clamped by the clamp pulse input from Pin 13. This RGB signals are mixed in the ratio of 0.6G + 0.3R + 0.1B, and Y signal is generated. The high frequency component is pulled out from a Y signal through a differential circuit, and the amplitude is varied according to the gain control circuit. The selecting of gain control and differential circuit time constant is performed by the DC voltage input from Pin 12. Gain controlled signal is output from Pin 15 after amplitude limited from a limiter circuit. At the same time, its signal is added to RGB signals input to Pins 1, 3 and 5, and then is output from Pins 17, 19 and 21.



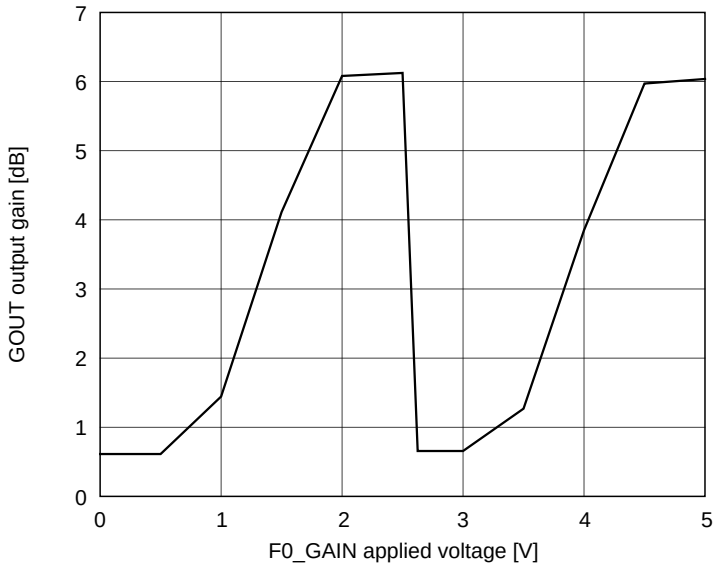
2. Synchronous system

The sync on green signal input to Pin 7 is synchronous separated by the sync separation circuit after diode clamped, and is output from Pin 14 as a positive polarity pulse.

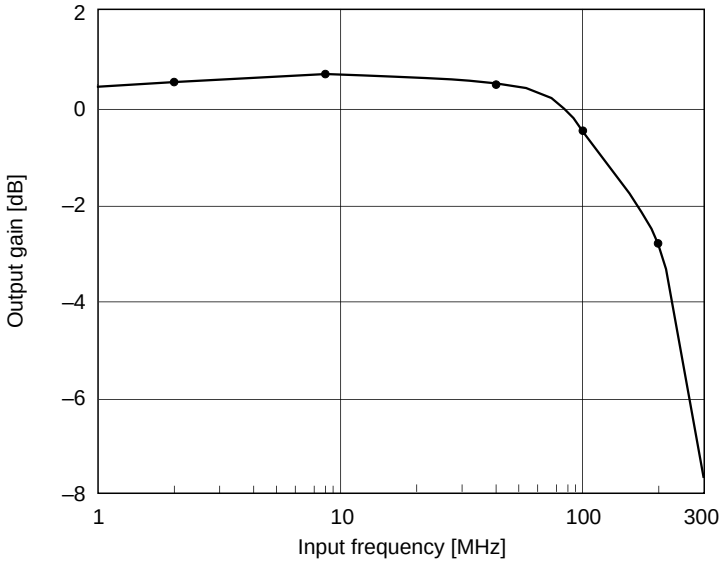
The input signal is not sync on green signal, video portion is sliced and then is output as a positive polarity pulse.

Example of Representative Characteristics

F0_GAIN control characteristics



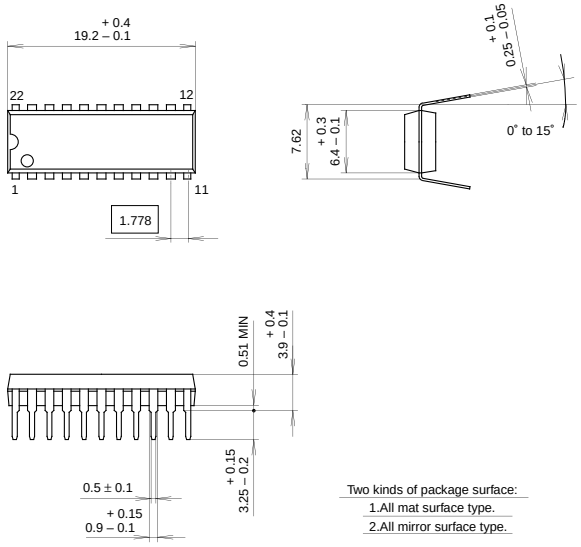
Frequency characteristics



Package Outline

Unit: mm

22PIN SDIP (PLASTIC)

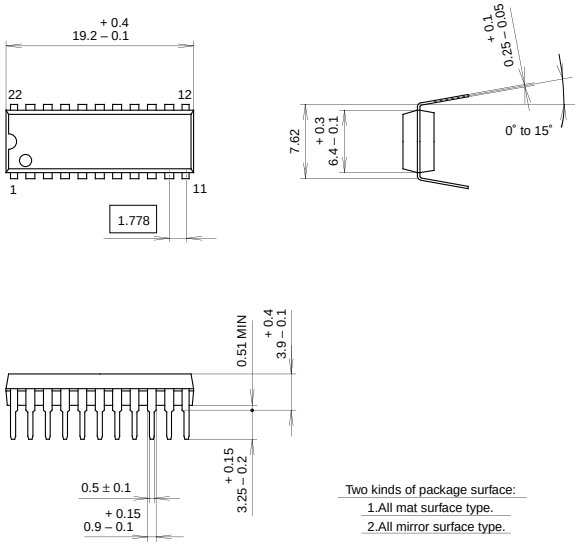


PACKAGE STRUCTURE

SONY CODE	SDIP-22P-01
EIAJ CODE	SDIP022-P-0300
JEDEC CODE	————

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.95g

22PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-22P-01
EIAJ CODE	SDIP022-P-0300
JEDEC CODE	————

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.95g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm