SONY

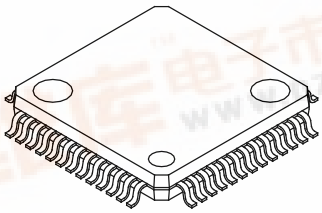
CXA2111R

LCD Signal Processor (Gamma Correction)

Description

The CXA2111R is a signal processor IC developed for LCD panels. Gamma correction, gain and bias, etc., can be adjusted using the I²C bus and external adjustment pins. The output of this IC is ideal as the input of the CXA2112R (LCD sample-and-hold driver IC), and the sample-and-hold position, etc., can also be adjusted using the I²C bus.

52 pin LQFP (Plastic)



Features

- Independent R, G and B gamma adjustment
- Three-point gamma gain and position adjustment (one white side point, two black side points)
- Independent R, G and B output amplifier gain and bias adjustment
- Various I²C bus-based controls and adjustment of various characteristics by external DC input
- Input signal clamp function (variable clamp voltage)
- Black side limiter adjustment
- CXA2112R adjustment output
- Precharge output (for CXA2112R)
- High frequency response
- High slew rate output

Applications

- Liquid crystal projectors
- Compact liquid crystal monitors

Structure

Bipolar silicon monolithic IC

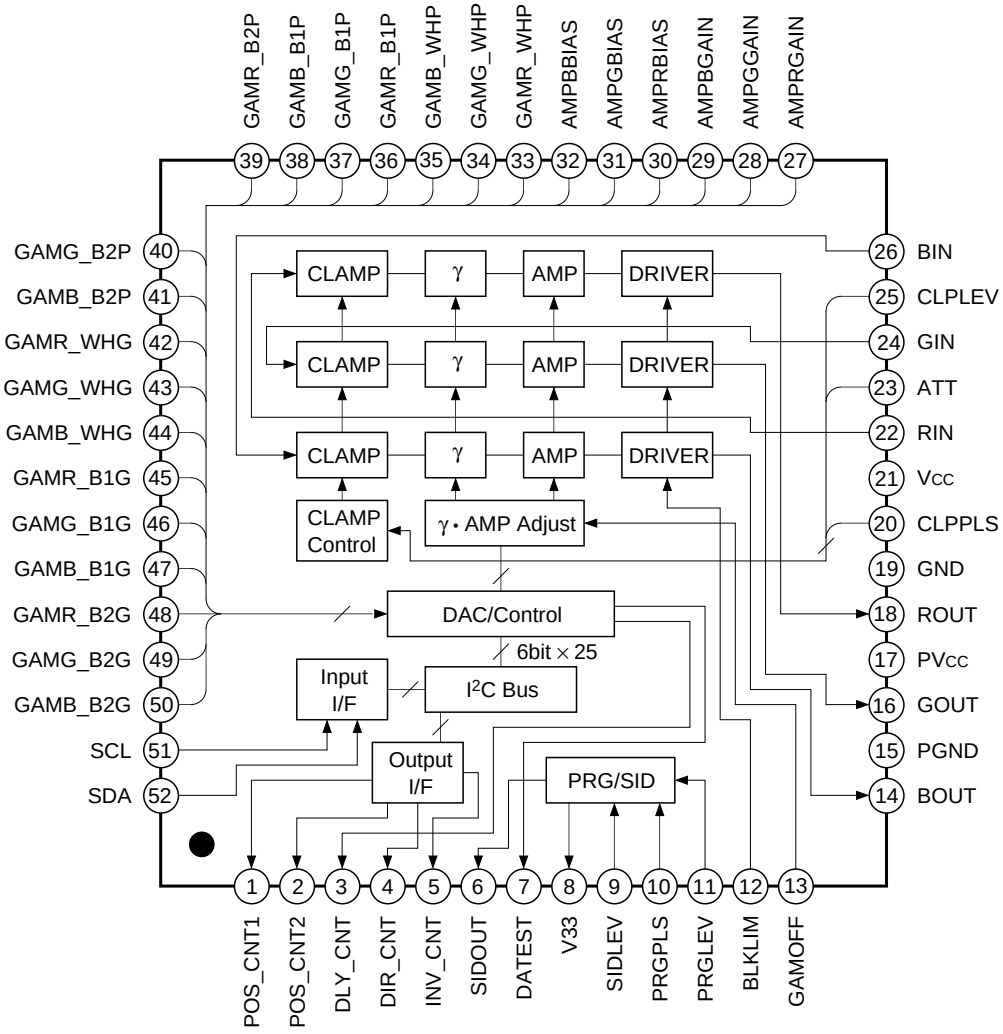
Absolute Maximum Ratings

• Supply voltage	V_{CC}	–0.3 to +5.5	V
• Input voltage	V_I	–0.3 to V_{CC} + 0.3	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1000	mW

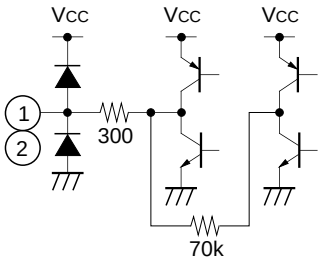
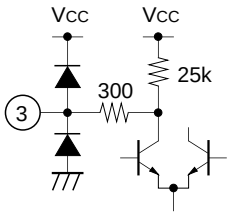
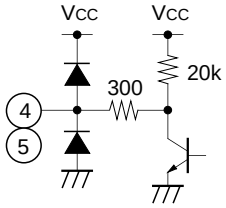
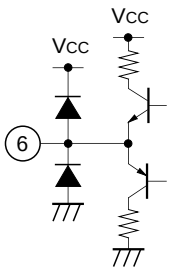
Operating Conditions

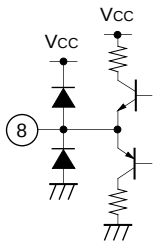
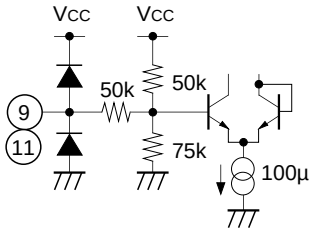
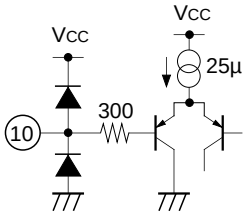
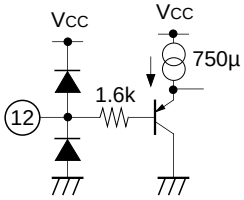
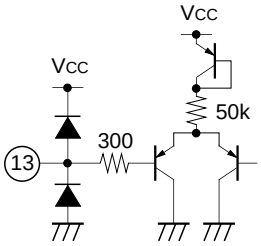
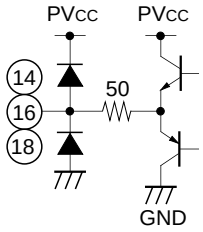
• Supply voltage	V_{CC}	4.75 to 5.25	V
• Digital input voltage high	V_H	2.2 to V_{CC}	V
• Digital input voltage low	V_L	0 to 0.8	V
• Operating temperature	Topr	–20 to +70	V

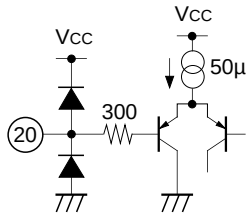
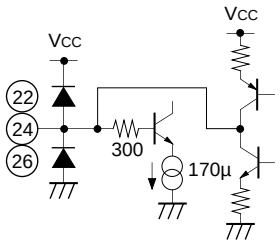
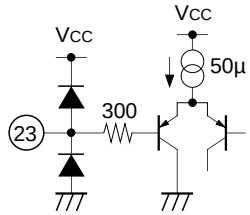
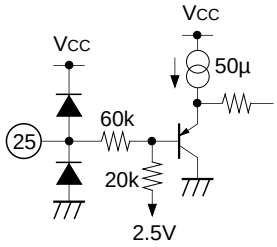
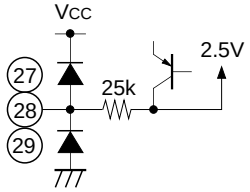
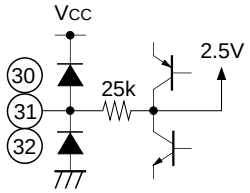
Pin Configuration and Block Diagram

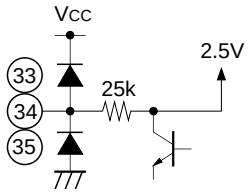
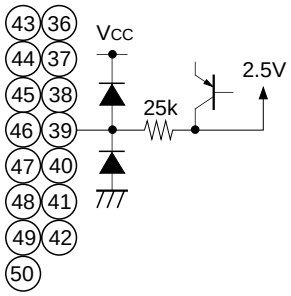
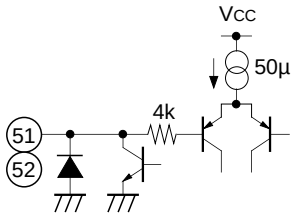


Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Typical pin voltage</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>1</td><td>POS_CNT1</td><td rowspan="2">O</td><td rowspan="2">0 to 5V (4 value)</td><td rowspan="2"> 
</td><td rowspan="2">CXA2112R control.
The sample-and-hold position is determined by the I²C data.
POS_CNT1 is the low-order 4-value output and POS_CNT2 is the high-order 4-value output for a total of 16-value control.
<table>
<tr><th>I²C data input (2 bits)</th><th>Pin output</th></tr>
<tr><td>00</td><td>L</td></tr>
<tr><td>01</td><td>↓</td></tr>
<tr><td>10</td><td>↓</td></tr>
<tr><td>11</td><td>H</td></tr>
</table></td></tr>
<tr><td>2</td><td>POS_CNT2</td></tr>
<tr><td>3</td><td>DLY_CNT</td><td>O</td><td>3 to 5V</td><td> 
</td><td>CXA2112R control.
The clock delay time is controlled by output analog value using I²C data.
<table>
<tr><th>I²C data input (6 bits)</th><th>Pin output</th></tr>
<tr><td>all 0</td><td>5V</td></tr>
<tr><td>↓</td><td>↓</td></tr>
<tr><td>all 1</td><td>3V</td></tr>
</table></td></tr>
<tr><td>4</td><td>DIR_CNT</td><td rowspan="2">O</td><td rowspan="2">L/H (0V/5V)</td><td rowspan="2"> 
</td><td>CXA2112R control.
The scan direction is determined by the I²C data.
<table>
<tr><th>I²C data input (1 bit)</th><th>Pin output</th></tr>
<tr><td>0</td><td>H</td></tr>
<tr><td>1</td><td>L</td></tr>
</table></td></tr>
<tr><td>5</td><td>INV_CNT</td><td>CXA2112R control.
The clock polarity is determined by the I²C data.
<table>
<tr><th>I²C data input (1 bit)</th><th>Pin output</th></tr>
<tr><td>0</td><td>H</td></tr>
<tr><td>1</td><td>L</td></tr>
</table></td></tr>
<tr><td>6</td><td>SIDOUT</td><td>O</td><td>2.3 to 3.3V</td><td> 
</td><td>Output for CXA2112R.
This pin outputs the precharge signal.
<table>
<tr><th>Pin 10 input</th><th>Pin 6 output</th></tr>
<tr><td>H</td><td>Level controlled by Pin 11</td></tr>
<tr><td>L</td><td>Level controlled by Pin 9</td></tr>
</table></td></tr>
<tr><td>7</td><td>DATEST</td><td></td><td></td><td></td><td>DAC test output.
Set the I²C data to "1". This pin is normally open.</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Typical pin voltage</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>8</td><td>V33</td><td>O</td><td>3.3V</td><td> 
</td><td>Output for CXA2112R.
This pin outputs 3.3V.</td></tr>
<tr><td>9</td><td>SIDLEV</td><td rowspan="2">I</td><td rowspan="2">0 to 5V</td><td rowspan="2"> 
</td><td rowspan="2">These pins determine the Pin 6 output level.
See Pin 6.</td></tr>
<tr><td>11</td><td>PRGLEV</td></tr>
<tr><td>10</td><td>PRGPLS</td><td>I</td><td>L/H
L: 0 to 0.8V
H: 2.2 to 5V</td><td> 
</td><td>This pin determines the Pin 6 output.
See Pin 6.
Set to low or high when using SIDOUT (Pin 6) as a DC output.</td></tr>
<tr><td>12</td><td>BLKLIM</td><td>I</td><td>1 to 5V</td><td> 
</td><td>Output black level (low level side) limit voltage control.
Apply voltage of 1V DC or more.</td></tr>
<tr><td>13</td><td>GAMOFF</td><td>I</td><td>L/H
L: 0 to 0.8V
H: 2.2 to 5V</td><td> 
</td><td>Gamma characteristics ON/OFF setting.
<table>
<tr><th>I²C data input (1bit)</th><th>Pin 13 input</th><th>γ mode</th></tr>
<tr><td rowspan="2">0</td><td>H</td><td>γ ON</td></tr>
<tr><td>L</td><td>γ OFF</td></tr>
<tr><td rowspan="2">1</td><td>H</td><td>γ OFF</td></tr>
<tr><td>L</td><td>γ OFF</td></tr>
</table></td></tr>
<tr><td>14</td><td>BOUT</td><td rowspan="3">O</td><td rowspan="3">1.8 to 3.3V</td><td rowspan="3"> 
</td><td>B channel output.</td></tr>
<tr><td>16</td><td>GOUT</td><td>G channel output.</td></tr>
<tr><td>18</td><td>ROUT</td><td>R channel output.</td></tr>
<tr><td>15</td><td>PGND</td><td></td><td>GND</td><td rowspan="3"></td><td>GND.</td></tr>
<tr><td>17</td><td>PVcc</td><td></td><td>5V</td><td>5V</td></tr>
<tr><td>19</td><td>GND</td><td></td><td>GND</td><td>GND.</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Typical pin voltage</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>20</td><td>CLPPLS</td><td>I</td><td>L/H
L: 0 to 0.8V
H: 2.2 to 5V</td><td> 
</td><td>Input signal clamp pulse input.
Set to low when not using the clamp function.
<table>
<tr><th>Pin input</th><th>Clamp function</th></tr>
<tr><td>H</td><td>ON</td></tr>
<tr><td>L</td><td>OFF</td></tr>
</table></td></tr>
<tr><td>21</td><td>Vcc</td><td></td><td>5V</td><td></td><td>5V</td></tr>
<tr><td>22</td><td>RIN</td><td rowspan="3">I</td><td rowspan="3">1.5 to 3.5V</td><td rowspan="3"> 
</td><td>R channel input.</td></tr>
<tr><td>24</td><td>GIN</td><td>G channel input.</td></tr>
<tr><td>26</td><td>BIN</td><td>B channel input.</td></tr>
<tr><td>23</td><td>ATT</td><td>I</td><td>L/H
L: 0 to 0.8V
H: 2.2 to 5V</td><td> 
</td><td>Input signal gain control.
This pin also supports 2Vp-p input.
<table>
<tr><th>Pin input</th><th>Clamp block gain</th><th>Signal level</th></tr>
<tr><td>H</td><td>0dB</td><td>For 1Vp-p</td></tr>
<tr><td>L</td><td>–6dB</td><td>For 2Vp-p</td></tr>
</table></td></tr>
<tr><td>25</td><td>CLPLEV</td><td>I</td><td>0 to 5V</td><td> 
</td><td>Clamp voltage control during clamp operation.
<table>
<tr><th>Pin input</th><th>Clamp voltage</th></tr>
<tr><td>5V</td><td>2.5V</td></tr>
<tr><td>↓</td><td>↓</td></tr>
<tr><td>2.5V (open)</td><td>2.0V</td></tr>
<tr><td>↓</td><td>↓</td></tr>
<tr><td>0V</td><td>1.5V</td></tr>
</table></td></tr>
<tr><td>27</td><td>AMPRGAIN</td><td rowspan="6">I</td><td rowspan="6">0 to 5V</td><td rowspan="3"> 
</td><td rowspan="3">Amplifier gain control.
Independent control for R, G and B.
Equivalent to 2.5V input when open.</td></tr>
<tr><td>28</td><td>AMPGGAIN</td></tr>
<tr><td>29</td><td>AMPBGAIN</td></tr>
<tr><td>30</td><td>AMPRBIAS</td><td rowspan="3"> 
</td><td rowspan="3">Amplifier bias control.
Independent control for R, G and B.
Equivalent to 2.5V input when open.</td></tr>
<tr><td>31</td><td>AMPGBIAS</td></tr>
<tr><td>32</td><td>AMPBBIAS</td></tr>
</table>

Pin No.	Symbol	I/O	Typical pin voltage	Equivalent circuit	Description
33	GAMR_WHP	I	0 to 5V		Gamma white position control. Independent control for R, G and B. Equivalent to 2.5V input when open.
34	GAMG_WHP				
35	GAMB_WHP				
36	GAMR_B1P				Gamma black 1 position control. Independent control for R, G and B. Equivalent to 2.5V input when open.
37	GAMG_B1P				
38	GAMB_B1P				
39	GAMR_B2P				Gamma black 2 position control. Independent control for R, G and B. Equivalent to 2.5V input when open.
40	GAMG_B2P				
41	GAMB_B2P				
42	GAMR_WHG				Gamma white gain control. Independent control for R, G and B. Equivalent to 2.5V input when open.
43	GAMG_WHG				
44	GAMB_WHG				
45	GAMR_B1G				Gamma black 1 gain control. Independent control for R, G and B. Equivalent to 2.5V input when open.
46	GAMG_B1G				
47	GAMB_B1G				
48	GAMR_B2G				Gamma black 2 gain control. Independent control for R, G and B. Equivalent to 2.5V input when open.
49	GAMG_B2G				
50	GAMB_B2G				
51	SCL	I	L/H (0V/5V)		I^2C bus clock input.
52	SDA	I/O			I^2C bus data input.

I²C Bus Format

Slave address: 0111 0110 (76h)

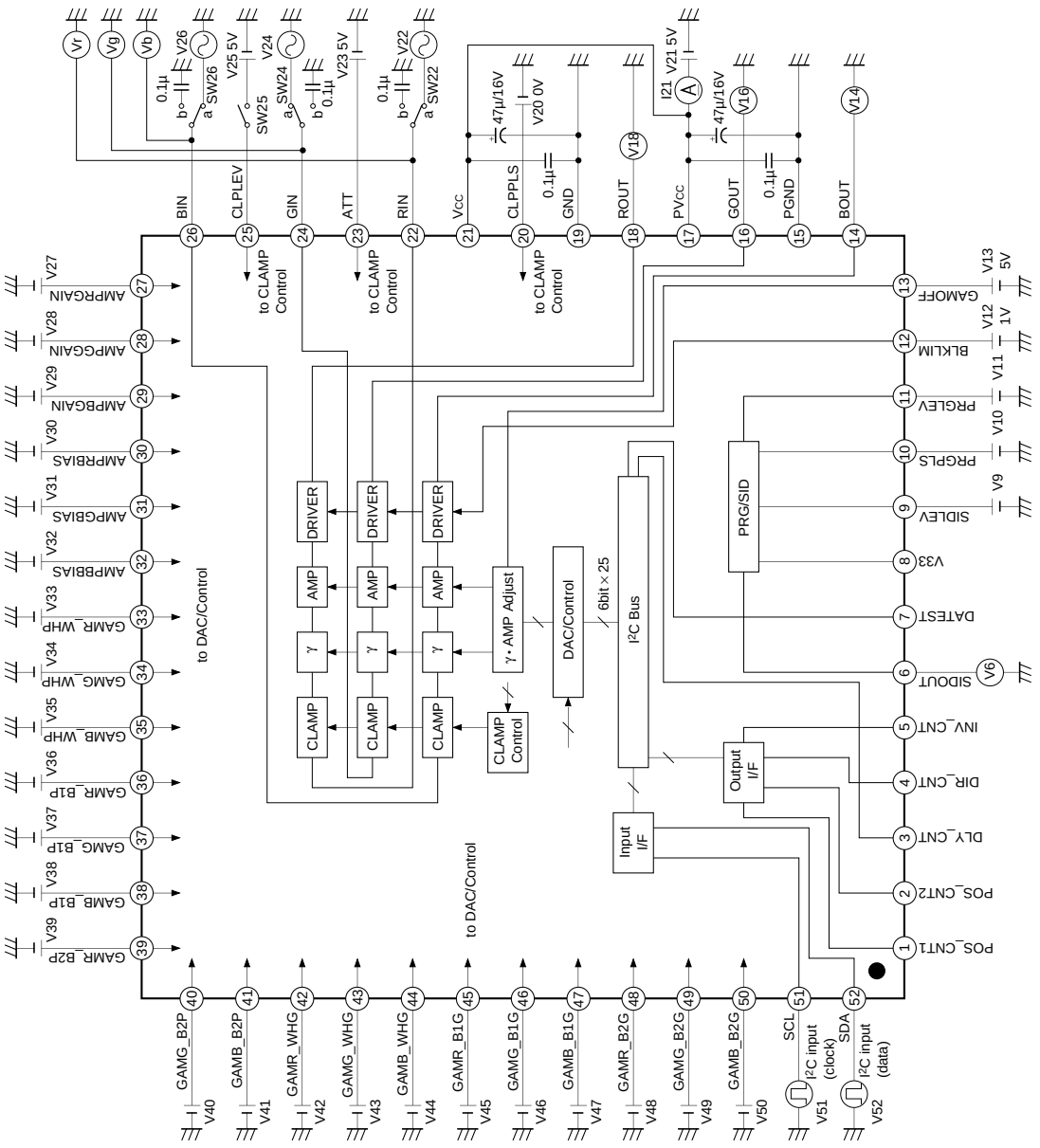
Sub address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
***00000 (00h)	AMPRGAIN							
***00001 (01h)	AMPGGAIN							
***00010 (02h)	AMPBGAIN							
***00011 (03h)	AMPRBIAS							
***00100 (04h)	AMPGBIAS							
***00101 (05h)	AMPBBIAS							
***00110 (06h)	GAMR_WHP							
***00111 (07h)	GAMG_WHP							
***01000 (08h)	GAMB_WHP							
***01001 (09h)	GAMR_B1P							
***01010 (0Ah)	GAMG_B1P							
***01011 (0Bh)	GAMB_B1P							
***01100 (0Ch)	GAMR_B2P							
***01101 (0Dh)	GAMG_B2P							
***01110 (0Eh)	GAMB_B2P							
***01111 (0Fh)	GAMR_WHG							
***10000 (10h)	GAMG_WHG							
***10001 (11h)	GAMB_WHG							
***10010 (12h)	GAMR_B1G							
***10011 (13h)	GAMG_B1G							
***10100 (14h)	GAMB_B1G							
***10101 (15h)	GAMR_B2G						GAMOFF	DATEST
***10110 (16h)	GAMG_B2G						POS_CNT2	
***10111 (17h)	GAMB_B2G						POS_CNT1	
***11000 (18h)	DLY_CNT						DIR_CNT	INV_CNT

Electrical Characteristics (See the Electrical Characteristics Measurement Circuit.) (V_{CC}, PV_{CC} = 5V, Ta = 25°C)

No.	Item	Symbol	Measu-rement point	Measurement conditions and measurement outline	Min.	Typ.	Max.	Unit
1	Current consumption	Icc	I21	[Gamma gain (white, black 1, black 2) = max., amplifier gain = max.] V22, 24, and 26 = 2.5V, V27 to 29 and 42 to 50 = 5V, V30 to 41 = open, Measure the I21 current.	80	135	180	mA
2	Digital input voltage high	Vih		Excluding the I^2C bus pins (Pins 51 and 52).	2.2		Vcc	V
3	Digital input voltage low	Vil		Excluding the I^2C bus pins (Pins 51 and 52).	GND		0.8	V
4	Maximum input voltage amplitude	Vix		Pins 22, 24 and 26 input	2			V
5	Maximum output voltage amplitude	Vox	V14 V16 V18	Pins 14, 16 and 18 output	1.5			V
6	Gamma white gain max.	Ggwx	V14 V16 V18	V27 to 29 and 36 to 44 = 5V, V30 to 35 = open, V45 to 50 = 0V Calculate Vwx/Vo (a) for the maximum Vwx at Vo (e), Vo (f) and Vo (g).	6.0	7.4	9.2	times
7	Gamma black 1 gain max.	Ggb1x	V14 V16 V18	V27 to 29, 39 to 41 and 45 to 47 = 5V, V30 to 32 and 36 to 38 = open, V33 to 35, 42 to 44 and 48 to 50 = 0V. Calculate Vb1x/Vo (i) for the maximum Vb1x at Vo (c), Vo (d) Vo (e) and Vo (f).	8.0	9.5	11.6	times
8	Gamma black 2 gain max.	Ggb2x	V14 V16 V18	V27 to 29, 36 to 38 and 48 to 50 = 5V, V30 to 32 = 3.75V, V33 to 35 and 42 to 47 = 0V, V39 to 41 = 3.3V Calculate Vb2x/Vo (h) for the maximum Vb2x at Vo (a), Vo (b) and Vo (c).	16.0	19.7	26.8	times
9	Amplifier gain max.	Gax	V14 V16 V18	V13 = 0V, V27 to 29 = 0V, V30 to 50 = open Calculate Vo (j)/0.1.	1.65	2.26	3.25	times
10	Amplifier gain min.	Gan	V14 V16 V18	V13 = 0V, V27 to 29 = 5V, V30 to 50 = open Calculate Vo (j)/0.1.	0.28	0.35	0.46	times
11	Amplifier bias output variable range	Vab	V14 V16 V18	V13 = 0V, V22, 24 and 26 = 2.5V, V27 to 29 = 0.75V, V33 to 50 = open V14, 16 and 18 voltages when V30 to 32 = 0V, open and 5V. Calculate Vb (0V) – Vb (open) and Vb (5V) – Vb (open) at Vb (0V), Vb (open) and Vb (5V).	±0.80	±0.96	±1.15	V
12	Gamma white gain I^2C max.	Ggwxi	V14 V16 V18	V27 to 29 and 36 to 44 = 5V, V30 to 35 and 42 to 44 = open, V45 to 50 = 0V, I^2C data = 3Fh Calculate Vwxi/Vo (a) for the maximum Vwxi at Vo (e), Vo (f) and Vo (g).	5.85	7.21	8.65	times
13	Gamma white gain I^2C min.	Ggwni	V14 V16 V18	V27 to 29 and 36 to 44 = 5V, V30 to 35 and 42 to 44 = open, V45 to 50 = 0V, I^2C data = 00h Calculate Vwni/Vo (a) for the maximum Vwni at Vo (e), Vo (f) and Vo (g).	3.80	4.71	5.65	times
14	Gamma black 1 gain I^2C max.	Ggb1xi	V14 V16 V18	V27 to 29, 39 to 41 and 45 to 47 = 5V, V30 to 32, 36 to 38 and 45 to 47 = open, V33 to 35, 42 to 44 and 48 to 50 = 0V, I^2C data = 3Fh Calculate Vb1xi/Vo (i) for the maximum Vb1xi at Vo (c), Vo (d) Vo (e) and Vo (f).	7.6	9.11	10.7	times
15	Gamma black 1 gain I^2C min.	Ggb1ni	V14 V16 V18	V27 to 29, 39 to 41 and 45 to 47 = 5V, V30 to 32, 36 to 38 and 45 to 47 = open, V33 to 35, 42 to 44 and 48 to 50 = 0V, I^2C data = 00h Calculate Vb1ni/Vo (i) for the maximum Vb1ni at Vo (c), Vo (d) Vo (e) and Vo (f).	5.05	6.02	7.00	times
16	Gamma black 2 gain I^2C max.	Ggb2xi	V14 V16 V18	V27 to 29, 36 to 38 and 48 to 50 = 5V, V30 to 32 = 3.75V, V33 to 35 and 42 to 47 = 0V, V39 to 41 = 3.3V, V48 to 50 = open, I^2C data = 3Fh Calculate Vb2xi/Vo (h) for the maximum Vb2xi at Vo (a), Vo (b) and Vo (c).	15.8	19.5	23.2	times

No.	Item	Symbol	Measu-rement point	Measurement conditions and measurement outline	Min.	Typ.	Max.	Unit
17	Gamma black 2 gain I^2C min.	Ggb2ni	V14 V16 V18	V27 to 29, 36 to 38 and 48 to 50 = 5V, V30 to 32 = 3.75V, V33 to 35 and 42 to 47 = 0V, V39 to 41 = 3.3V, V48 to 50 = open, I^2C data = 3Fh Calculate Vb2xi/Vo (h) for the maximum Vb2xi at Vo (a), Vo (b) and Vo (c).	11.3	14.0	16.7	times
18	Amplifier gain I^2C max.	Gaxi	V14 V16 V18	V13 = 0V, V27 to 50 = open, I^2C data = 00h Calculate Vo (j)/0.1.	0.44	0.55	0.67	times
19	Amplifier gain I^2C min.	Gani	V14 V16 V18	V13 = 0V, V27 to 50 = open, I^2C data = 3Fh Calculate Vo (j)/0.1.	0.30	0.39	0.47	times
20	Amplifier bias I^2C output variable range	Vabi	V14 V16 V18	V13 = 0V, V22, 24 and 26 = 2.5V, V27 to 29 = 0.75V, V30 to 50 = open V14, 16 and 18 voltages when I^2C data = 00h, 20h and 3Fh. Calculate Vbi (00h) – Vbi (20h) and Vbi (3Fh) – Vbi (20h) at Vbi (00h), Vbi (20h) and Vbi (3Fh).	±0.34	±0.39	±0.45	V
21	Frequency response	Gf	V14 V16 V18	[Gamma OFF, amplifier gain min., ratio of 100MHz to 20MHz] V13 = 0V, V27 to 29 = 5V, V30 to 50 = open Calculate 20*LOG {Vo (k)/Vo (j)}.	–2.7			dB
22	Clamp voltage min.	Vcn	Vr Vg Vb	SW22, 24, 26 = b, SW25 = ON V20 = 5V, V25 = 0V	1.35	1.45	1.55	V
23	Clamp voltage max.	Vcx	Vr Vg Vb	SW22, 24, 26 = b, SW25 = ON V20 = 5V, V25 = 5V	2.75	2.85	2.95	V
24	Black limiter voltage	Vbl	V14 V16 V18	V12 = 1.3V, V13 = 0V, V22, 24, 26 = 2V, V27 to 29 = 0.75V, V30 to 32 = 0V, V33 to 50 = open	1.00	1.19	1.35	V
25	Output maximum voltage value (white limiter voltage)	Vwl	V14 V16 V18	V13, 27 to 29 = 0V, V22, 24, 26 = 3.1V, V30 to 32 = 5V, V33 to 50 = open	3.50	3.71	4.00	V
26	SIDOUT output min.	Vsn	V6	V9 = V11 = 0.5 V, V10 = 0V or 5V	1.75	1.98	2.15	V
27	SIDOUT output max.	Vsx	V6	V9 = V11 = 4.5 V, V10 = 0V or 5V	3.30	3.48	3.65	V
28	I^2C DAC (6-bit) DLE	Dle		DAC output when DAC data = 00h, 1Fh, 20h and 3Fh. Calculate | {V (20h) – V (1Fh)}/[{V (3Fh) – V (00h}/63] | – 1 at V (00h), V (1Fh), V (20h) and V (3Fh).	–0.9		0.6	LSB
29	Output rise/fall time <Reference data>	Trf	V14 V16 V18	Gamma OFF, gain adjusted so that 1Vp-p pulse input results in 1.5Vp-p output, output 3pF load		4		ns
30	Gamma position max. (white/black 1/black 2) <Reference data>	Pgx		With input DC 2.0 to 3.0V set as 0 to 100 IRE V33 to V41 = 0V	100			IRE
31	Gamma position min. (white/black 1/black 2) <Reference data>	Pgn		With input DC 2.0 to 3.0V set as 0 to 100 IRE V33 to V41 = 5V			0	IRE
32	Gamma position I^2C max. (white) <Reference data>	Pgwxi		With input DC 2.0 to 3.0V set as 0 to 100 IRE V33 to 35 = open, I^2C data = 3Fh		100		IRE
33	Gamma position I^2C min. (white) <Reference data>	Pgwni		With input DC 2.0 to 3.0V set as 0 to 100 IRE V33 to 35 = open, I^2C data = 00h		40		IRE
34	Gamma position I^2C max. (black 1/black 2) <Reference data>	Pgbxi		With input DC 2.0 to 3.0V set as 0 to 100 IRE V36 to 41 = open, I^2C data = 00h		70		IRE
35	Gamma position I^2C min. (black 1/black 2) <Reference data>	Pgbni		With input DC 2.0 to 3.0V set as 0 to 100 IRE V36 to 41 = open, I^2C data = 3Fh		0		IRE

Electrical Characteristics Measurement Circuit



The following sine wave signals are defined as the V22, 24 and 26 inputs.

(a) 2.15Vdc + 0.1Vp-p 20MHz
(b) 2.25Vdc + 0.1Vp-p 20MHz
(c) 2.35Vdc + 0.1Vp-p 20MHz
(d) 2.45Vdc + 0.1Vp-p 20MHz
(e) 2.55Vdc + 0.1Vp-p 20MHz
(f) 2.65Vdc + 0.1Vp-p 20MHz
(g) 2.75Vdc + 0.1Vp-p 20MHz
(h) 2.85Vdc + 0.1Vp-p 20MHz
(i) 2.95Vdc + 0.1Vp-p 20MHz
(j) 2.5Vdc + 0.1Vp-p 20MHz
(k) 2.5Vdc + 0.1Vp-p 100MHz

In addition, the V14, 16 and 18 output levels for the above inputs (x) are labeled Vo (x).

<I²C standard data>

Slave address = 76h

No.	Item	Data
1	AMPRGAIN	00h
2	AMPGGAIN	00h
3	AMPBGAIN	00h
4	AMPRBIAS	20h
5	AMPGBIAS	20h
6	AMPBBIAS	20h
7	GAMR_WHP	00h
8	GAMG_WHP	00h
9	GAMB_WHP	00h
10	GAMR_B1P	00h
11	GAMG_B1P	00h
12	GAMB_B1P	00h
13	GAMR_B2P	00h
14	GAMG_B2P	00h
15	GAMB_B2P	00h
16	GAMR_WHG	00h
17	GAMG_WHG	00h
18	GAMB_WHG	00h
19	GAMR_B1G	00h
20	GAMG_B1G	00h
21	GAMB_B1G	00h
22	GAMR_B2G	00h
23	GAMG_B2G	00h
24	GAMB_B2G	00h
25	DLY_CNT	00h
26	POS_CNT1	00
27	POS_CNT2	00
28	DIR_CNT	0
29	INV_CNT	0
30	GAMOFF	0
31	DATEST	1

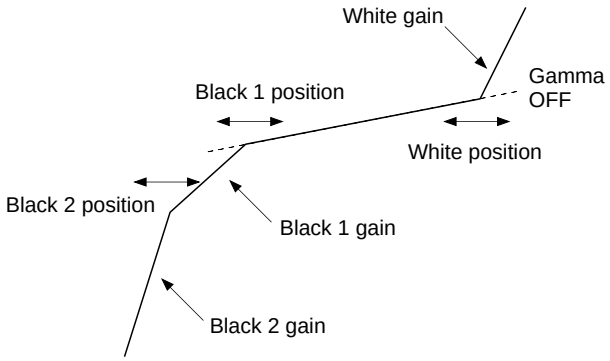
Description of Operation

1. Gamma control

The bend positions and respective gains of one white side point and two black side points can be varied.

Control is performed independently for R, G and B by the I^2C bus or by external DC.

In addition, the gamma function can easily be forced OFF (by Pin 13 or the I^2C bus).



2. Amplifier gain and bias control

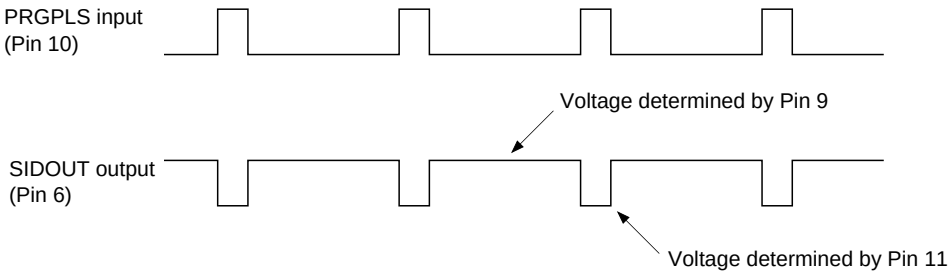
After adjusting the gamma, the signal gain and DC voltage can also be adjusted.

3. SIDOUT

SIDOUT generates the precharge signal.

After the CXA2111R determines the DC level (Pins 9 and 11) and the pulse width (Pin 10), the signal is inverted by the CXA2112R and applied to the LCD panel.

See the Example of Representative Characteristics for the DC level.



Output example

4. I^2C bus

The various gamma and amplifier controls can be performed in accordance with the I^2C Bus Format table.

In addition, the sample-and-hold position and other items can also be controlled by connecting the CXA2112R.

Notes on Operation

1. External DC voltage adjustment, I²C adjustment and variable ranges

(a) When varying the external DC voltage

Setting the I²C data to the standard setting values (listed in the Electrical Characteristics Measurement Circuit) is recommended when performing the various adjustments using the external pins (Pins 27 to 50). Note that setting data that differs from these standard setting values may clip one side of the variable ranges below.

(b) When varying the I²C setting

The variable ranges when the external pins are open or 2.5V are as shown in the table below. The I²C variable range position can be altered by changing the voltage applied to the external pins. However, note that characteristics in excess of the range in (a) above cannot be obtained.

	(a) External voltage adjustment	(b) I²C adjustment (external pins open or 2.5V)
γ white gain	× 7.4 ↕ 5V × 1 0V (I²C standard setting 00h)	× 7.21 ↕ 3Fh × 4.71 00h The variable position can be altered by changing the external voltage.
γ black 1 gain	× 9.5 ↕ 5V × 1 0V (I²C standard setting 00h)	× 9.11 ↕ 3Fh × 6.02 00h
γ black 2 gain	× 19.7 ↕ 5V × 1 0V (I²C standard setting 00h)	× 19.5 ↕ 3Fh × 14.0 00h

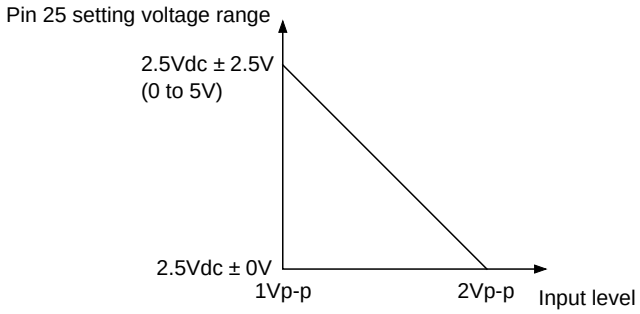
	(a) External voltage adjustment	(b) I^2C adjustment (external pins open or 2.5V)
γ white position	100 IRE ↕ 0V 0 IRE ↕ 5V (I^2C standard setting 00h)	100 IRE ↕ 3Fh 40 IRE ↕ 00h
γ black 1 position	100 IRE ↕ 0V 0 IRE ↕ 5V (I^2C standard setting 00h)	70 IRE ↕ 00h 0 IRE ↕ 3Fh
γ black 2 position	100 IRE ↕ 0V 0 IRE ↕ 5V (I^2C standard setting 00h)	70 IRE ↕ 00h 0 IRE ↕ 3Fh

Note) The 0 to 100 IRE levels here correspond to the following values when ATT (Pin 23) is high.
Clamp OFF: Input 2 to 3V (1Vp-p)
Clamp ON: Input 1Vp-p (however, Pin 25 = open or 2.5V)

	(a) External voltage adjustment	(b) I^2C adjustment (external pins open or 2.5V)
Amplifier gain	× 2.26 ↕ 0V × 0.35 5V (I^2C standard setting 00h)	× 0.55 ↕ 00h × 0.39 3Fh
Amplifier bias (relative variation)	+0.96V ↕ 5V 0V 2.5V –0.96V 0V (I^2C standard setting 20h)	+0.39V ↕ 00h 0V 20h –0.39V 3Fh

2. Input signal level and clamp

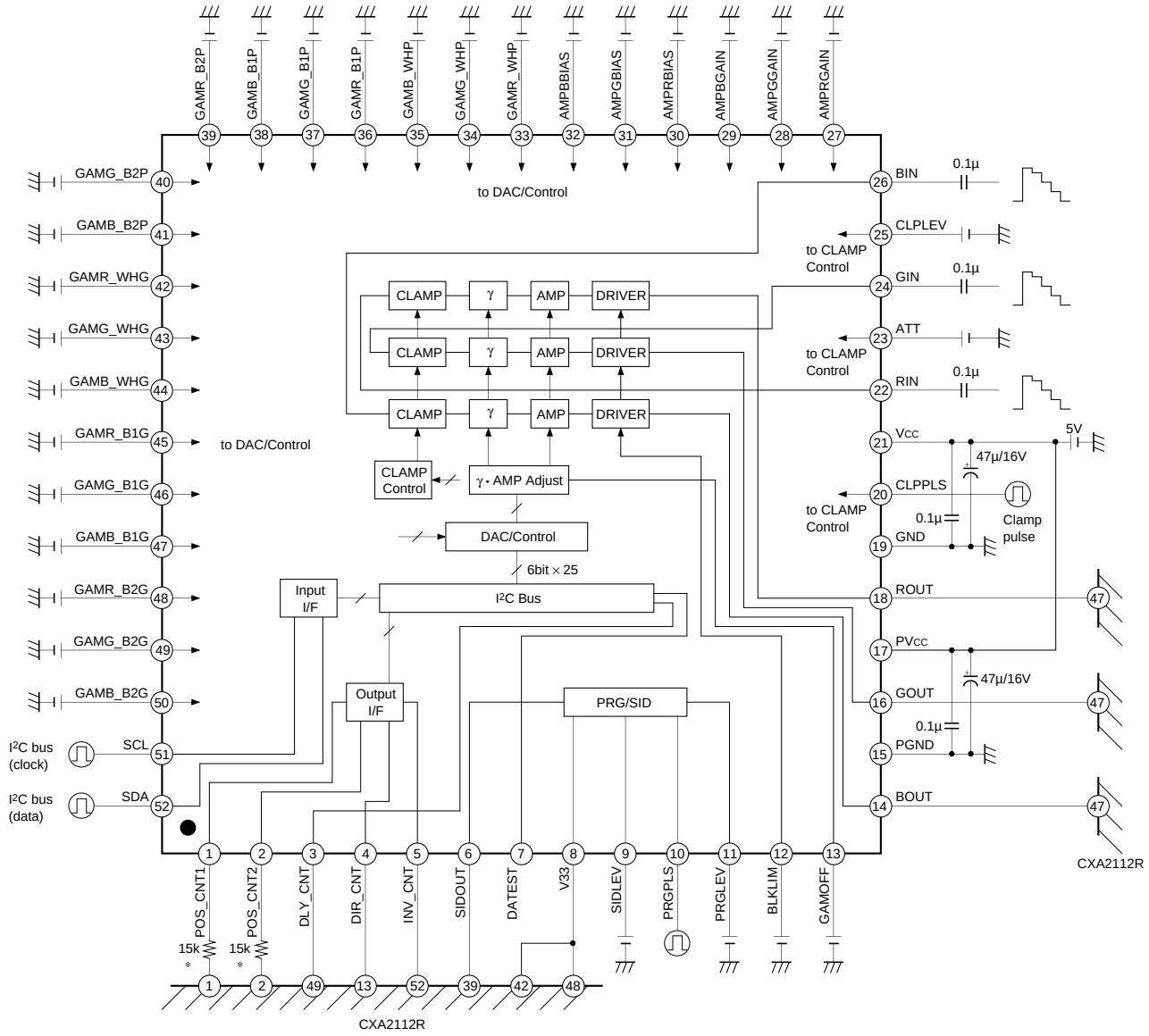
Set Pin 23 (ATT) low when the input amplitude exceeds 1Vp-p (up to 2Vp-p).
In this case, care should be taken for the clamp voltage setting (Pin 25) when applying the clamp. See the figure below.
(The input pin voltage should not exceed the range of 1.5V DC to 3.5V DC.)



3. I^2C bus

The CXA2111R requires I^2C bus control.
The initial values must be set after power-on even when using only external DC adjustment.

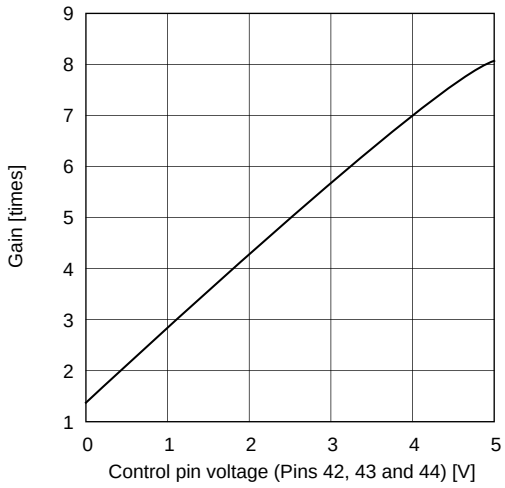
Application Circuit



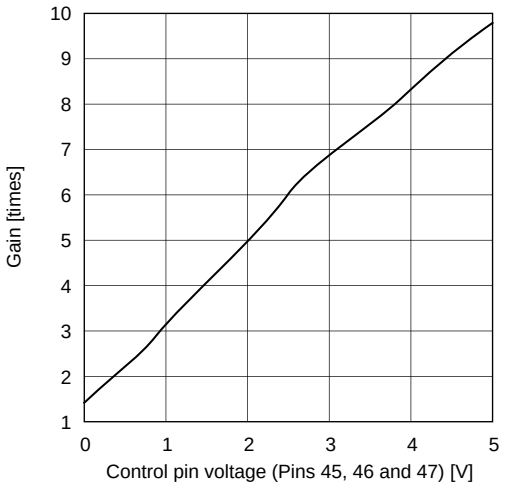
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (Vcc = 5V, Ta = 25°C)

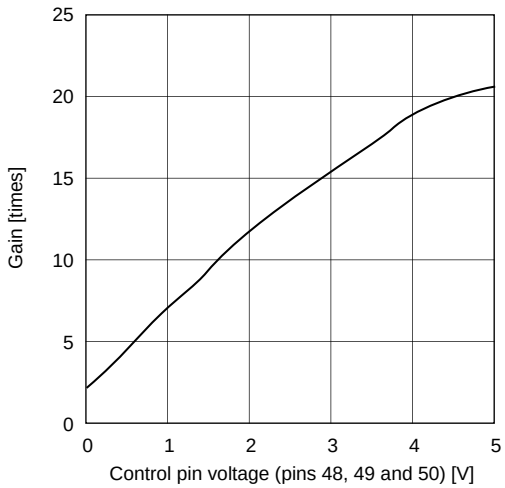
R/G/B gamma white gain
(I²C: standard setting)



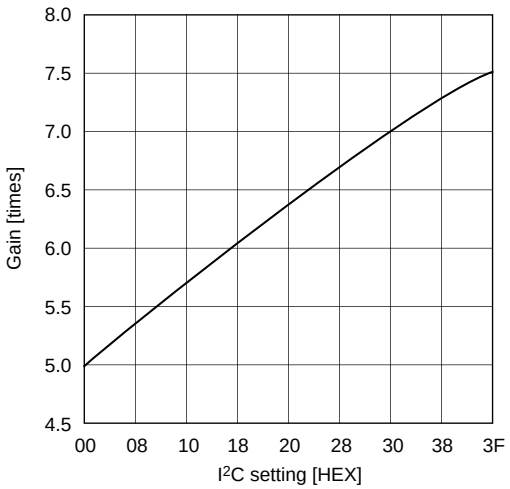
R/G/B gamma black 1 gain
(I²C: standard setting)



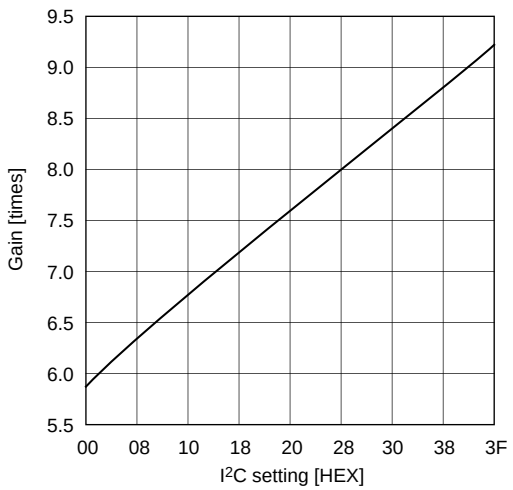
R/G/B gamma black 2 gain
(I²C: standard setting)



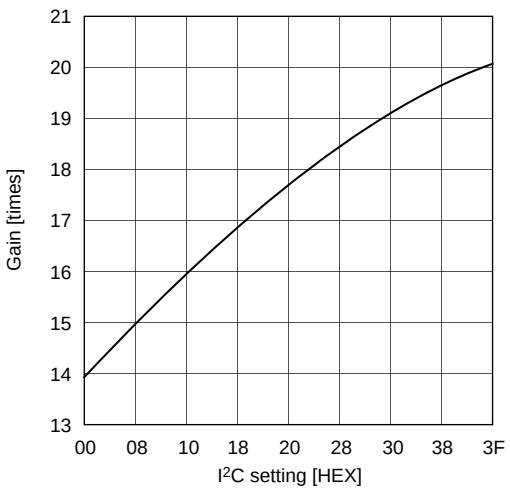
R/G/B gamma white gain I²C characteristics
(Control pins = open)



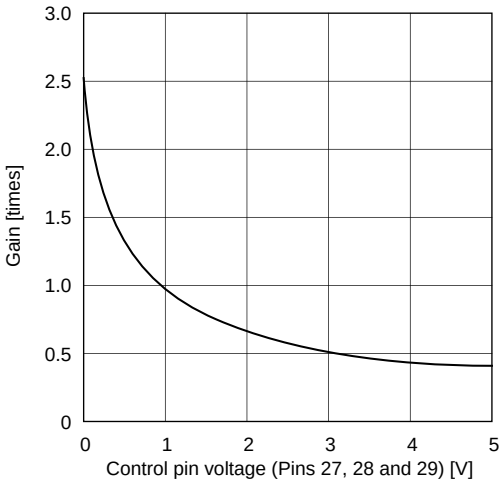
R/G/B gamma black 1 gain I²C characteristics
(Control pins = open)



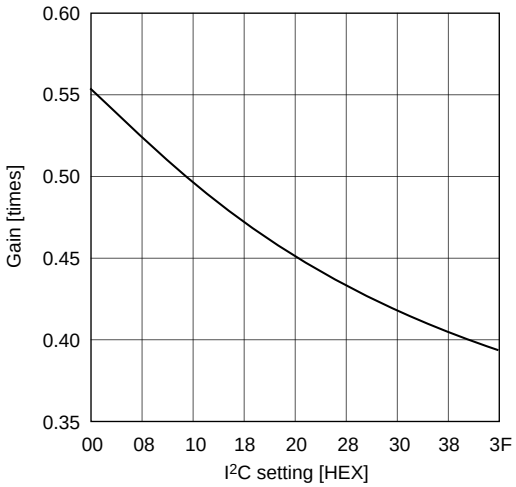
R/G/B gamma black 2 gain I²C characteristics
(Control pins = open)



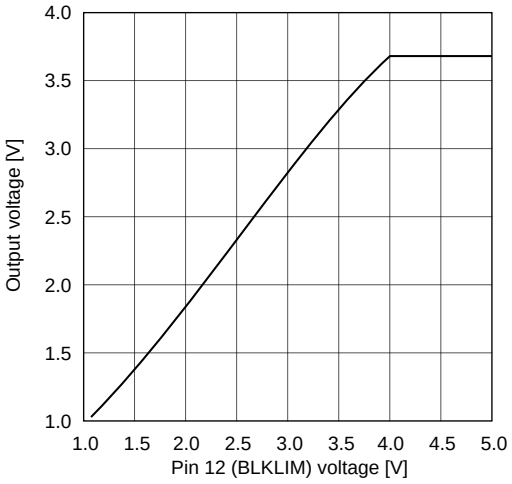
R/G/B amplifier gain
(I²C: Standard setting)



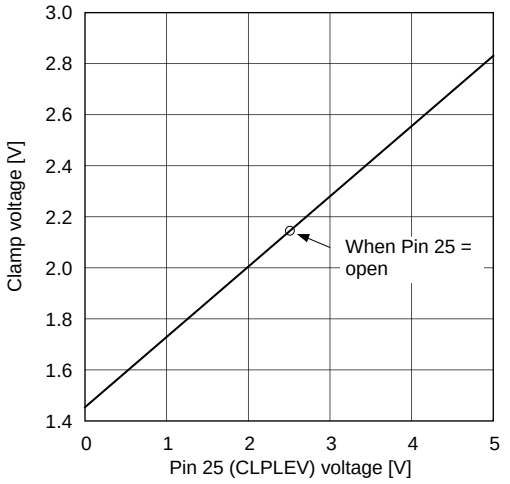
R/G/B amplifier gain I²C characteristics
(Control pins = open)



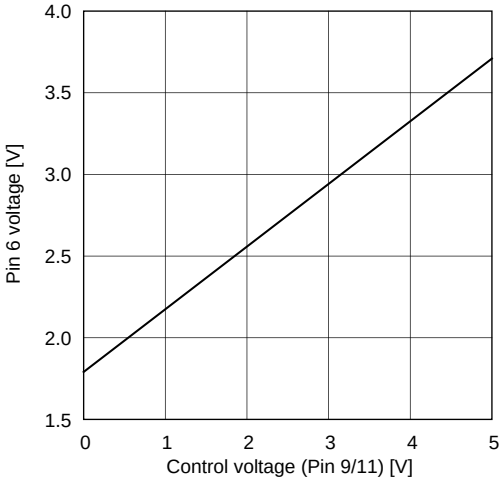
R/G/B output black limiter voltage



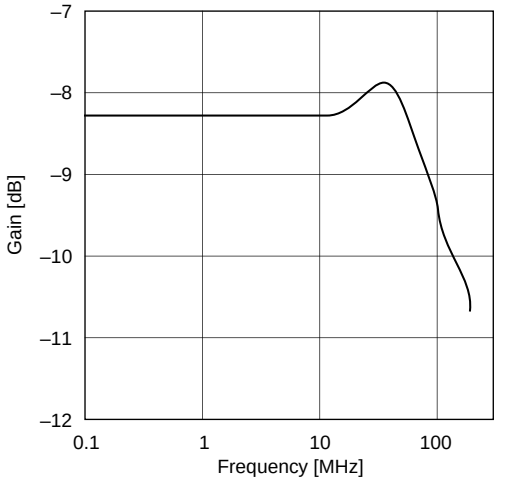
R/G/B input clamp voltage characteristics



Pin 6 (SIDOUT) output

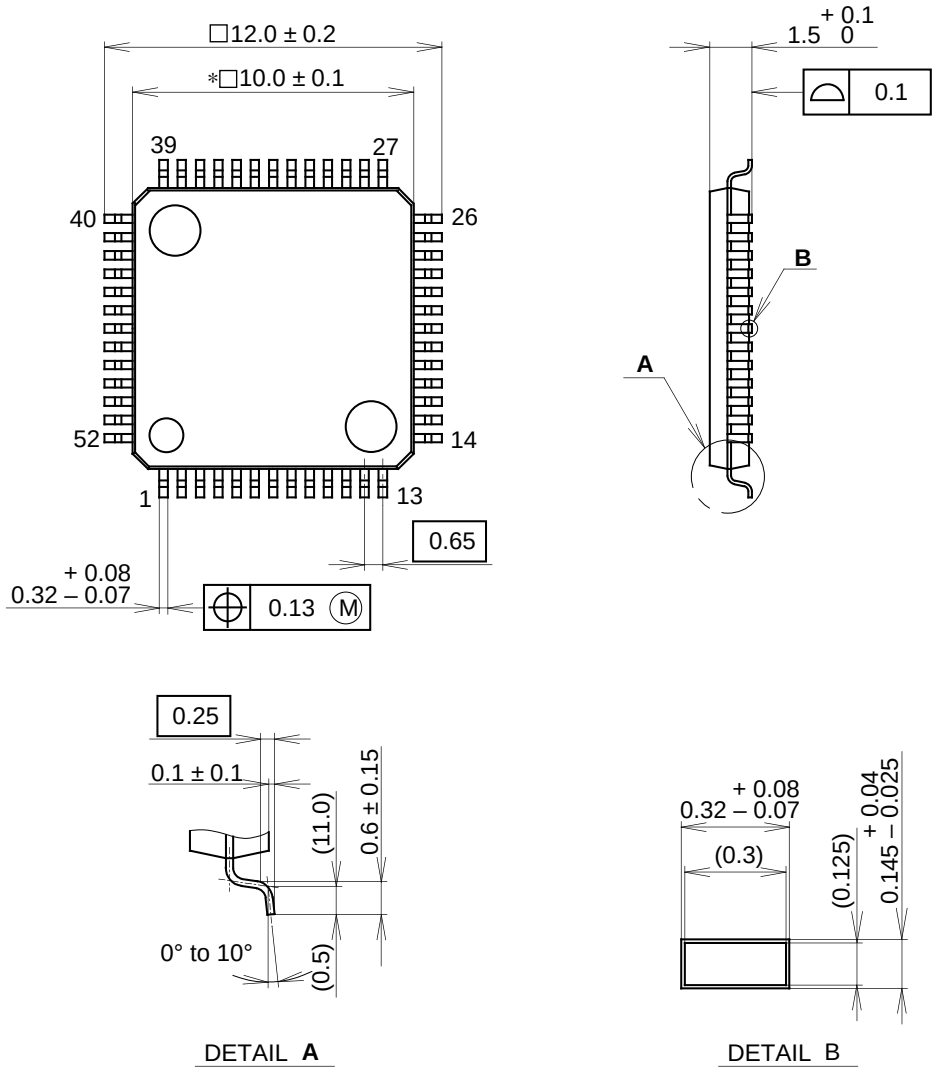


R/G/B frequency response
(Gamma OFF, amplifier gain = min.)



Package Outline Unit: mm

52PIN LQFP(PLASTIC)



DETAIL **A** DETAIL B

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-52P-L01
EIAJ CODE	LQFP052-P-1010
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g