SONY

# CXA2570N

## RF Matrix Amplifier

### Description

The CXA2570N is an IC developed for the RF signal processing of compact disc players.

### Features

- Wide band RF signal processing
- RF system VCA circuit
- RF system equalizer (supports CAV mode)
- Supports pickups with built-in RF summing amplifier
- Low power consumption mode (EQ Pass mode)
- RW/ROM switching mode

### Functions

- RFAC summing amplifier, equalizer, VCA
- RFDC summing amplifier
- Focus error amplifier
- Tracking error amplifier
- Automatic power control
- VC buffer amplifier

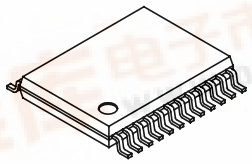
### Applications

CD-ROM/RW compatible systems

### Structure

Bipolar silicon monolithic IC

24 pin SSOP (Plastic)



### Absolute Maximum ratings

| | | | |
|---|---|---|---|
| • Supply voltage | Vcc | 7 | V |
| • Operating temperature | Topr | –20 to +75 | °C |
| • Storage temperature | Tstg | –65 to +150 | °C |
| • Allowable power dissipation | $P_D$ | 620 | mW |

### Operating Conditions

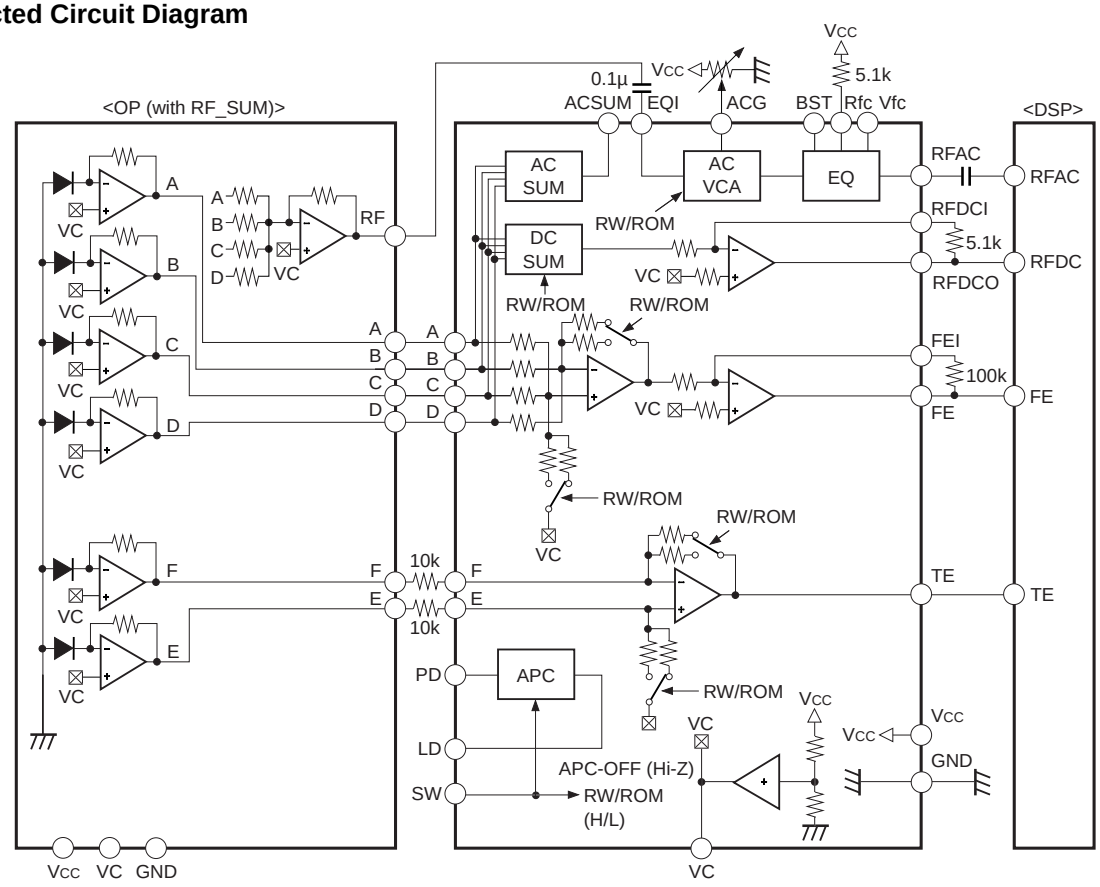
| | | | |
|---|---|---|---|
| • Supply voltage | Vcc – GND | 3.0 to 5.5 | V |
| • Operating temperature | Topr | –20 to +75 | °C |

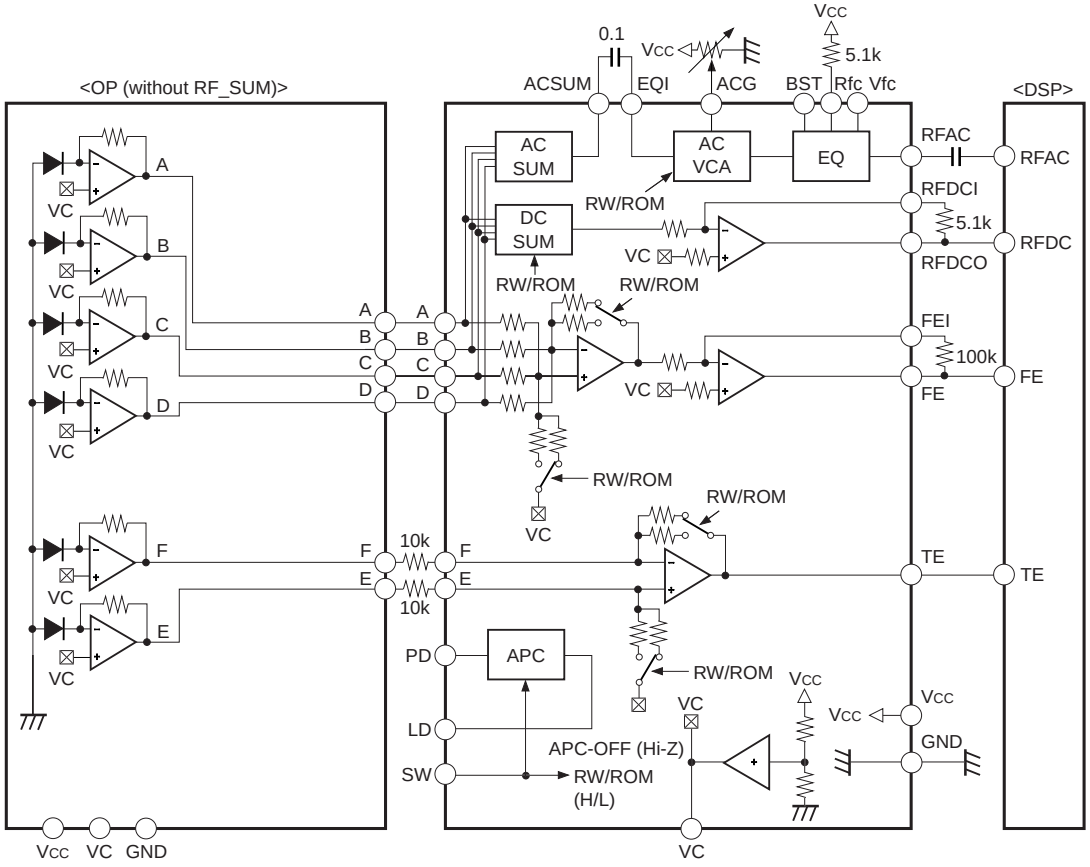




E98259A98-PS

## Connected Circuit Diagram

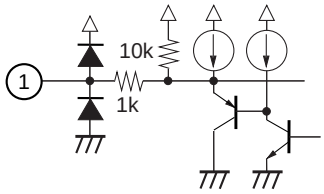
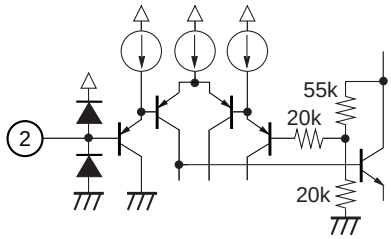
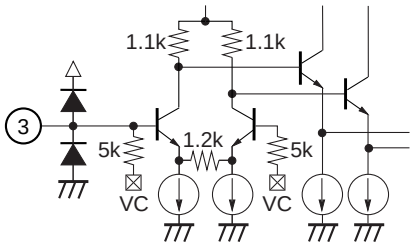
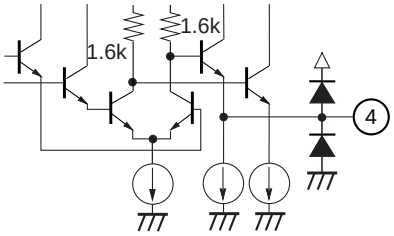


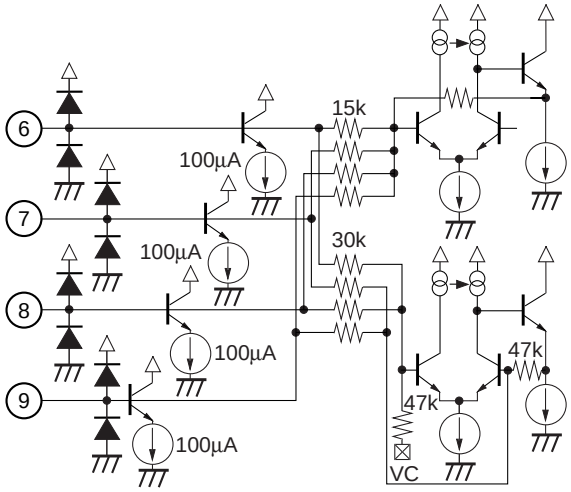
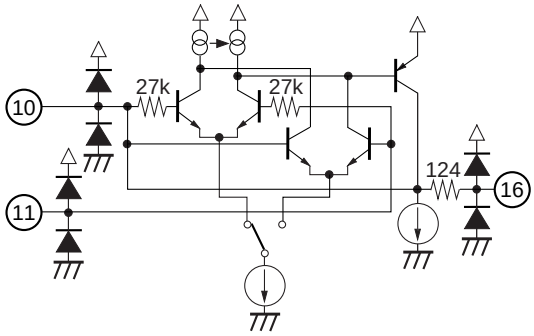
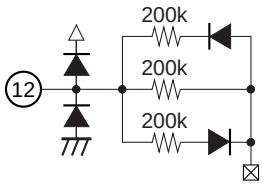
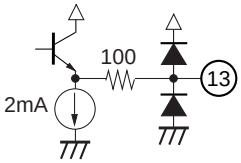
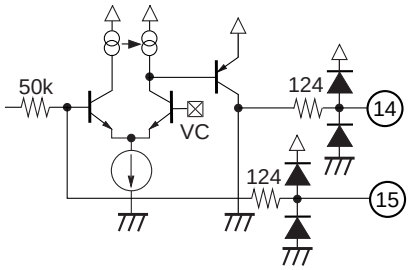



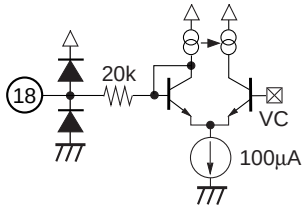
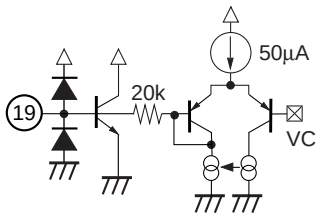
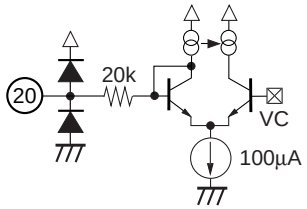
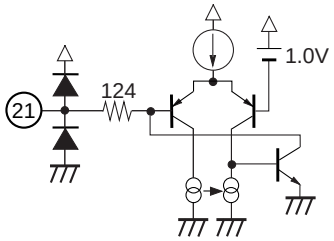
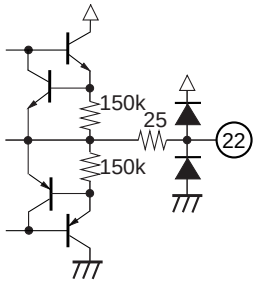
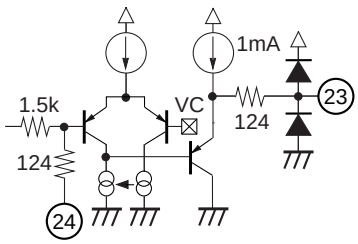
**Pin Description**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | LD | Out | APC amplifier output. |
| 2 | PD | In | APC amplifier input. |
| 3 | EQ_IN | In | RFAC system VCA block and EQ block input. |
| 4 | AC_SUM | Out | RFAC system RF SUM output. |
| 5 | GND | In | Ground. |
| 6 | A | In | A signal input. |
| 7 | B | In | B signal input. |
| 8 | C | In | C signal input. |
| 9 | D | In | D signal input. |
| 10 | E | In | E signal input. |
| 11 | F | In | F signal input. |
| 12 | SW | In | Mode switching signal input. |
| 13 | RFAC | Out | RFAC signal output. |
| 14 | FE | Out | Focus error signal output. |
| 15 | FEI | — | FE amplifier virtual ground. |
| 16 | TE | Out | Tracking error signal output. |
| 17 | $V_{CC}$ | In | $V_{CC}$. |
| 18 | RFG | In | RFAC system VCA block low-frequency gain adjustment. |
| 19 | BST | In | EQ boost amount adjustment range. |
| 20 | VFC | In | EQ cut-off frequency adjustment. |
| 21 | RFC | In | EQ cut-off frequency adjustment. |
| 22 | VC | Out | VC voltage output. |
| 23 | RFDCO | Out | RFDC signal output. |
| 24 | RFDCI | — | RFDC amplifier virtual ground. |

**Pin Description and Equivalent Circuit**

| Pin No. | Symbol | I/O | Equivalent circuit | Description |
|---|---|---|---|---|
| 1 | LD | O |  | APC amplifier output. |
| 2 | PD | I |  | APC amplifier input. |
| 3 | EQ_IN | I |  | Equalizer circuit input. |
| 4 | AC_SUM | O |  | RFAC summing amplifier output. |
| 5 | GND | — | — | Ground. |

| Pin No. | Symbol | I/O | Equivalent circuit | Description |
|---|---|---|---|---|
| 6 | A | I |  | RF summing amplifier and focus error amplifier input. |
| 7 | B | I | | |
| 8 | C | I | | |
| 9 | D | I | | |
| 10 | E | I |  | Tracking error amplifier input. |
| 11 | F | I | | |
| 16 | TE | O | | Tracking error amplifier output. |
| 12 | SW | I |  | CD-ROM/RW switching input. RW when connected to $V_{CC}$, ROM when connected to GND. |
| 13 | RFAC | O |  | RFAC amplifier output. |
| 14 | FE | O |  | Focus error amplifier output. |
| 15 | FEI | I | | Focus error amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 14. |

| Pin No. | Symbol | I/O | Equivalent circuit | Description |
|---|---|---|---|---|
| 17 | $V_{CC}$ | — | — | Power supply. |
| 18 | RFG | I |  | Sets the RFAC low-frequency gain. |
| 19 | BST | I |  | Input for adjusting the equalizer circuit boost amount. |
| 20 | VFC | I |  | Input for adjusting the equalizer circuit boost frequency with the control voltage. |
| 21 | RFC | I |  | Input for adjusting the equalizer circuit boost frequency with external resistance. |
| 22 | VC | O |  | ($V_{CC}$ + GND)/2 voltage output. |
| 23 | RFDC | O |  | RFDC amplifier output. This pin serves as the eye pattern check point. |
| 24 | RFDCI | I | | RFDC amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 23. |

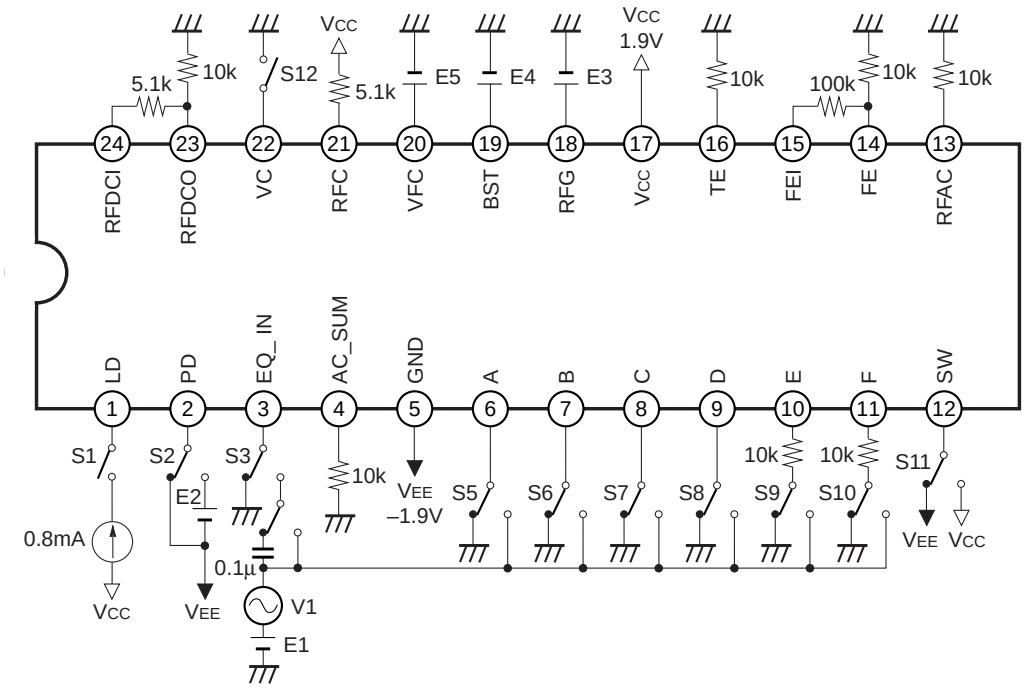
## Electrical Characteristics

($V_{CC}$ = 1.9V, $V_{EE}$ = –1.9V)

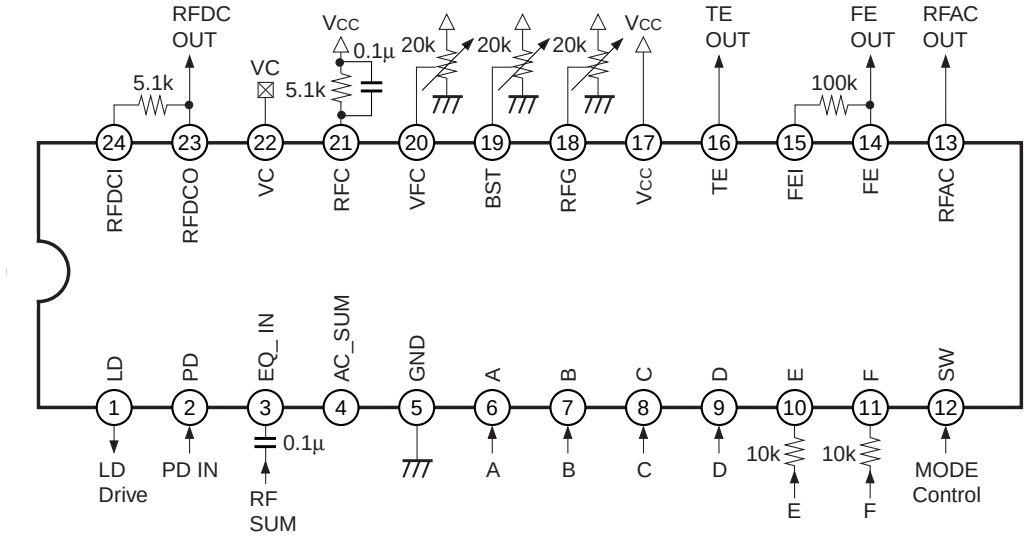
| Measurement No. | Function | Measurement item | Symbol | Switch conditions | | | | | | | | | | | | Bias conditions | | | | | | | Measurement pin | Measurement conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | V1 amplitude | V1 frequency | E1 | E2 | E3 | E4 | E5 | | | | | | |
| 1 | | Current consumption (Active, EQ On) | Icc_Aeqon | | | | | | | | | | | | | | | 0V | 0V | 0V | 0V | 0V | 17 | Pin current | 25 | 45 | 65 | mA |
| 2 | | Current consumption (Active, EQ Off) | Icc_Aeqoff | | | | | | | | | | | | | | | | | | 1.9V | | 17 | Pin current | 10 | 25 | 40 | mA |
| 3 | | Current consumption (Sleep) | Icc_Slp | | | | | | | | | | | Hi-Z | | | | | | | 0V | | 17 | Pin current | 3.0 | 5 | 7.5 | mA |
| 4 | RFAC SUM | SUM offset voltage | ACSUM_Ofst | | | | | | | | | | | | | | | | | | | | 4 | Pin voltage | –1.2 | –0.6 | 0 | V |
| 5 | | SUM frequency gain | Gsum | | | | | O | O | O | O | | | | | 0.1Vp-p | 100kHz | | | | | | 4 | 20 log (Vout/Vin) | 14.0 | 16.0 | 18.0 | dB |
| 6 | | SUM frequency response | Fsum | | | | | O | O | O | O | | | | | 0.1Vp-p | 30MHz | ↓ | | | | | 4 | 20 log (Vout/Vin) – Gsum | –3.0 | –1.5 | 0.3 | dB |
| 7 | | SUM maximum output voltage H | Vsum_H | | | | | O | O | O | O | | | | | | | 0.3V | | | | | 4 | Pin voltage | 0.9 | 1.25 | — | V |
| 8 | | SUM maximum output voltage L | Vsum_L | | | | | O | O | O | O | | | | | | | –0.3V | | | | | 4 | Pin voltage | — | –0.5 | –0.3 | V |
| 9 | RFAC EQ | Offset voltage ROM | AC_OfstROM | | | | | | | | | | | | | | | 0V | | | | | 13 | Pin voltage | –0.3 | 0 | 0.3 | V |
| 10 | | Offset voltage RW | AC_OfstRW | | | | | | | | | | | O | | | | | | ↓ | | | 13 | Pin voltage | –0.3 | 0 | 0.3 | V |
| 11 | | Low-frequency gain ROM_min | Gac_ROM1 | | | O | | | | | | | | | | 1.6Vp-p | 100kHz | | | –1.0V | | | 13 | 20 log (Vout/Vin) – Gac_ROM2 | –11.0 | –8.0 | –5.0 | dB |
| 12 | | Low-frequency gain ROM_cnt | Gac_ROM2 | | | O | | | | | | | | | | 0.8Vp-p | 100kHz | | | 0V | | | 13 | 20 log (Vout/Vin) | –1.0 | 2.0 | 5.0 | dB |
| 13 | | Low-frequency gain ROM_max | Gac_ROM3 | | | O | | | | | | | | | | 0.3Vp-p | 100kHz | | | 1.0V | | | 13 | 20 log (Vout/Vin) – Gac_ROM2 | 5.0 | 8.0 | 11.0 | dB |
| 14 | | Low-frequency gain RW_min | Gac_RW1 | | | O | | | | | | | | O | | 0.4Vp-p | 100kHz | | | –1.0V | | | 13 | 20 log (Vout/Vin) – Gac_RW2 | –11.0 | –8.0 | –5.0 | dB |
| 15 | | Low-frequency gain RW_cnt | Gac_RW2 | | | O | | | | | | | | O | | 0.2Vp-p | 100kHz | | | 0V | | | 13 | 20 log (Vout/Vin) – Gac_ROM2 | 9.0 | 12.0 | 15.0 | dB |
| 16 | | Low-frequency gain RW_max | Gac_RW3 | | | O | | | | | | | | O | | 75mVp-p | 100kHz | | | 1.0V | | | 13 | 20 log (Vout/Vin) – Gac_RW2 | 5.0 | 8.0 | 11.0 | dB |
| 17 | | Low-frequency gain EQ_off | Gac_EQoff | | | O | | | | | | | | | | 0.8Vp-p | 100kHz | | | 0V | | ↓ | 13 | 20 log (Vout/Vin) | –1.0 | 2.0 | 5.0 | dB |
| 18 | | Frequency response Min_L | Fac_MinL | | | O | | | | | | | | | | 0.2Vp-p | 10MHz | | | | | –1.9V | 13 | 20 log (Vout/Vin) – Gac_ROM2 | 3.5 | 6.0 | 8.5 | dB |
| 19 | | Frequency response Min_H | Fac_MinH | | | O | | | | | | | | | | 0.2Vp-p | 30MHz | | | | ↓ | 1.9V | 13 | 20 log (Vout/Vin) – Gac_ROM2 | 3.5 | 6.0 | 8.5 | dB |
| 20 | | Frequency response EQ_OFF | Fac_ECoff | | | O | | | | | | | | | | 0.8Vp-p | 30MHz | ↓ | | | 1.9V | 0V | 13 | 20 log (Vout/Vin) – Gac_EQoff | –2.0 | –1.0 | –0.5 | dB |
| 21 | | Maximum output voltage H | Vac_H | | | O | O | | | | | | | | | | | 2V | | | 0V | | 13 | Pin voltage – AC_OfstROM | 0.6 | 0.8 | — | V |
| 22 | | Maximum output voltage L | Vac_L | | | O | O | | | | | | | | | | | –2V | | | | | 13 | Pin voltage – AC_OfstROM | — | –0.8 | –0.6 | V |
| 23 | RFDC | Offset voltage ROM | DC_OfstROM | | | | | | | | | | | | | | | 0V | | | | | 23 | Pin voltage | –150 | 0 | 150 | mV |
| 24 | | Offset voltage RW | DC_OfstRW | | | | | | | | | | | O | | | | | | | | | 23 | Pin voltage | –100 | 0 | 400 | mV |
| 25 | | Low-frequency gain ROM | Gdc_ROM | | | | | O | O | O | O | | | | | 0.1Vp-p | 100kHz | | | | | | 23 | 20 log (Vout/Vin) | 16.5 | 19.5 | 22.5 | dB |
| 26 | | Low-frequency gain RW | Gdc_RW | | | | | O | O | O | O | | | O | | 25mVp-p | 100kHz | | | | | | 23 | 20 log (Vout/Vin) | 29.0 | 32.0 | 35.0 | dB |
| 27 | | Frequency response ROM | Fdc_ROM | | | | | O | O | O | O | | | | | 0.1Vp-p | 10MHz | | | | | | 23 | 20 log (Vout/Vin) – Gdc_ROM | –3.5 | –1.5 | –0.5 | dB |
| 28 | | Frequency response RW | Fdc_RW | | | | | O | O | O | O | | | O | | 25mVp-p | 10MHz | ↓ | | | | | 23 | 20 log (Vout/Vin) – Gdc_RW | –6.0 | –3.0 | –0.5 | dB |
| 29 | | Maximum output voltage H | Vdc_H | | | | | O | O | O | O | | | | | | | 0.25V | | | | | 23 | Pin voltage | 1.3 | 1.6 | — | V |
| 30 | | Maximum output voltage L | Vdc_L | | | | | O | O | O | O | | | | | | | –0.25V | ↓ | ↓ | ↓ | ↓ | 23 | Pin voltage | — | –1.0 | –0.6 | V |

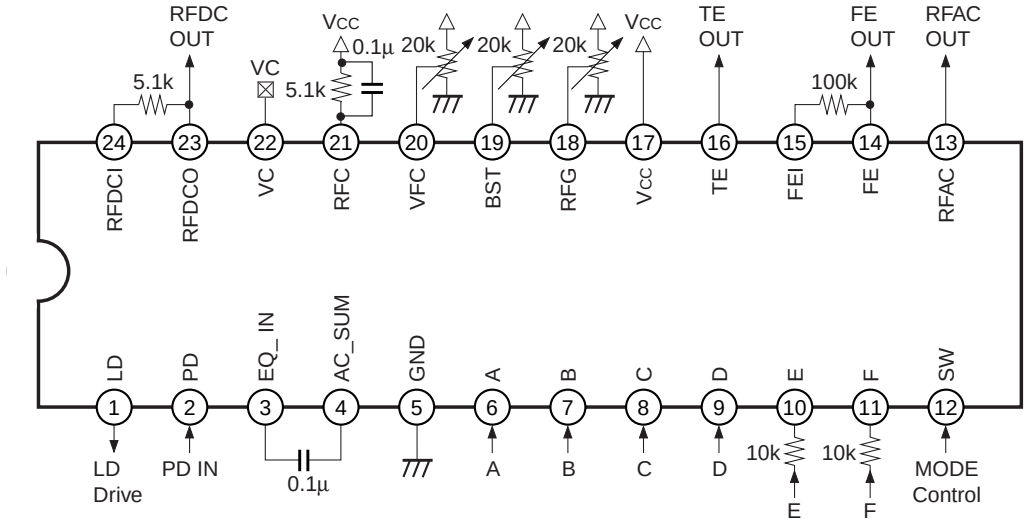
| Measurement No. | Function | Measurement item | Symbol | Switch conditions | | | | | | | | | | | | Bias conditions | | | | | | | | | | Measurement pin | Measurement conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | V1 amplitude | V1 frequency | E1 | | E2 | | E3 | | E4 | | E5 | | | | | | |
| 31 | FE | Offset voltage ROM | FE_OfstROM | | | | | | | | | | | | | | | 0V | | 0V | | 0V | | 0V | | 0V | | 14 | Pin voltage | –150 | 0 | 150 | mV |
| 32 | | Offset voltage RW | FE_OfstRW | | | | | | | | | | | O | | | | | | | | | | | | | | 14 | Pin voltage | –150 | 0 | 150 | mV |
| 33 | | Low-frequency gain ROM1 | Gfe_ROM1 | | | | | O | | O | | | | | | 0.1Vp-p | 10kHz | | | | | | | | | | | 14 | 20 log (Vout/Vin) | 13.0 | 16.0 | 19.0 | dB |
| 34 | | Low-frequency gain ROM2 | Gfe_ROM2 | | | | | | O | | O | | | | | 0.1Vp-p | 10kHz | | | | | | | | | | | 14 | 20 log (Vout/Vin) | 13.0 | 16.0 | 19.0 | dB |
| 35 | | Low-frequency gain RW1 | Gfe_RW1 | | | | | O | | O | | | | O | | 25mVp-p | 10kHz | | | | | | | | | | | 14 | 20 log (Vout/Vin) | 25.0 | 28.0 | 31.0 | dB |
| 36 | | Low-frequency gain RW2 | Gfe_RW2 | | | | | | O | | O | | | O | | 25mVp-p | 10kHz | | | | | | | | | | | 14 | 20 log (Vout/Vin) | 25.0 | 28.0 | 31.0 | dB |
| 37 | | Frequency response ROM1 | Ffe_ROM1 | | | | | O | | O | | | | | | 0.1Vp-p | 100kHz | | | | | | | | | | | 14 | 20 log (Vout/Vin) – Gfe_ROM1 | –3.5 | –0.5 | 0.3 | dB |
| 38 | | Frequency response ROM2 | Ffe_ROM2 | | | | | | O | | O | | | | | 0.1Vp-p | 100kHz | | | | | | | | | | | 14 | 20 log (Vout/Vin) – Gfe_ROM2 | –3.5 | –0.5 | 0.3 | dB |
| 39 | | Frequency response RW1 | Ffe_RW1 | | | | | O | | O | | | | O | | 25mVp-p | 50kHz | | | | | | | | | | | 14 | 20 log (Vout/Vin) – Gfe_RW1 | –3.5 | –0.5 | 0.3 | dB |
| 40 | | Frequency response RW2 | Ffe_RW2 | | | | | | O | | O | | | O | | 25mVp-p | 50kHz | ↓ | | | | | | | | | | 14 | 20 log (Vout/Vin) – Gfe_RW2 | –3.5 | –0.5 | 0.3 | dB |
| 41 | | Maximum output voltage H | Vfe_H | | | | | | O | | O | | | | | | | 0.3V | | | | | | | | | | 14 | Pin voltage | 1.2 | 1.7 | — | V |
| 42 | | Maximum output voltage L | Vfe_L | | | | | O | | O | | | | | | | | –0.3V | | | | | | | | | | 14 | Pin voltage | — | –1.5 | –1.1 | V |
| 43 | TE | Offset voltage ROM | TE_OfstROM | | | | | | | | | | | | | | | 0V | | | | | | | | | | 16 | Pin voltage | –150 | 0 | 150 | mV |
| 44 | | Offset voltage RW | TE_OfstRW | | | | | | | | | | | O | | | | | | | | | | | | | | 16 | Pin voltage | –150 | 0 | 150 | mV |
| 45 | | Low-frequency gain ROM1 | Gte_ROM1 | | | | | | | | | O | | | | 0.1Vp-p | 10kHz | | | | | | | | | | | 16 | 20 log (Vout/Vin) | 17.0 | 20.0 | 23.0 | dB |
| 46 | | Low-frequency gain ROM2 | Gte_ROM2 | | | | | | | | | | O | | | 0.1Vp-p | 10kHz | | | | | | | | | | | 16 | 20 log (Vout/Vin) | 17.0 | 20.0 | 23.0 | dB |
| 47 | | Low-frequency gain RW1 | Gte_RW1 | | | | | | | | | O | | O | | 25mVp-p | 10kHz | | | | | | | | | | | 16 | 20 log (Vout/Vin) | 29.0 | 32.0 | 35.0 | dB |
| 48 | | Low-frequency gain RW2 | Gte_RW2 | | | | | | | | | | O | O | | 25mVp-p | 10kHz | | | | | | | | | | | 16 | 20 log (Vout/Vin) | 29.0 | 32.0 | 35.0 | dB |
| 49 | | Frequency response ROM1 | Fte_ROM1 | | | | | | | | | O | | | | 0.1Vp-p | 200kHz | | | | | | | | | | | 16 | 20 log (Vout/Vin) – Gte_ROM1 | –1.5 | 0 | 1.5 | dB |
| 50 | | Frequency response ROM2 | Fte_ROM2 | | | | | | | | | | O | | | 0.1Vp-p | 200kHz | | | | | | | | | | | 16 | 20 log (Vout/Vin) – Gte_ROM2 | –1.5 | 0 | 1.5 | dB |
| 51 | | Frequency response RW1 | Fte_RW1 | | | | | | | | | O | | O | | 25mVp-p | 200kHz | | | | | | | | | | | 16 | 20 log (Vout/Vin) – Gte_RW1 | –4.5 | –2.0 | –0.2 | dB |
| 52 | | Frequency response RW2 | Fte_RW2 | | | | | | | | | | O | O | | 25mVp-p | 200kHz | ↓ | | | | | | | | | | 16 | 20 log (Vout/Vin) – Gte_RW2 | –4.5 | –2.0 | –0.2 | dB |
| 53 | | Maximum output voltage H | Vte_H | | | | | | | | | | O | | | | | 0.3V | | | | | | | | | | 16 | Pin voltage | 1.2 | 1.7 | — | V |
| 54 | | Maximum output voltage L | Vte_L | | | | | | | | | O | | | | | | –0.3V | | | | | | | | | | 16 | Pin voltage | — | –1.5 | –1.1 | V |
| 55 | APC | Output voltage 1 | Vapc1 | | O | | | | | | | | | | | | | 0V | | ↓ | | | | | | | | 1 | Input where output voltage = 0V | 85 | 135 | 185 | mV |
| 56 | | Output voltage 2 | Vapc2 | | O | | | | | | | | | | | | | | | –30mV | | | | | | | | 1 | Pin voltage | 0.45 | 0.7 | 0.95 | V |
| 57 | | Output voltage 3 | Vapc3 | | O | | | | | | | | | | | | | | | 30mV | | | | | | | | 1 | Pin voltage | –0.95 | –0.7 | –0.45 | V |
| 58 | | APC OFF voltage | Vapc_off | | O | | | | | | | | | Hi-Z | | | | | | 0V | | | | | | | | 1 | Pin voltage | 1.4 | 1.6 | – | V |
| 59 | | Maximum output current | Iapc_max | O | O | | | | | | | | | | | | | | | | | | | | | | | 1 | Pin voltage | –0.2 | 0 | 0.6 | V |
| 60 | VC | Output voltage | Vvc | | | | | | | | | | | | O | | | ↓ | | ↓ | | ↓ | | ↓ | | ↓ | | 22 | Pin voltage | –100 | 0 | 100 | mV |

**Electrical Characteristics Measurement Circuit**



## Application Circuits



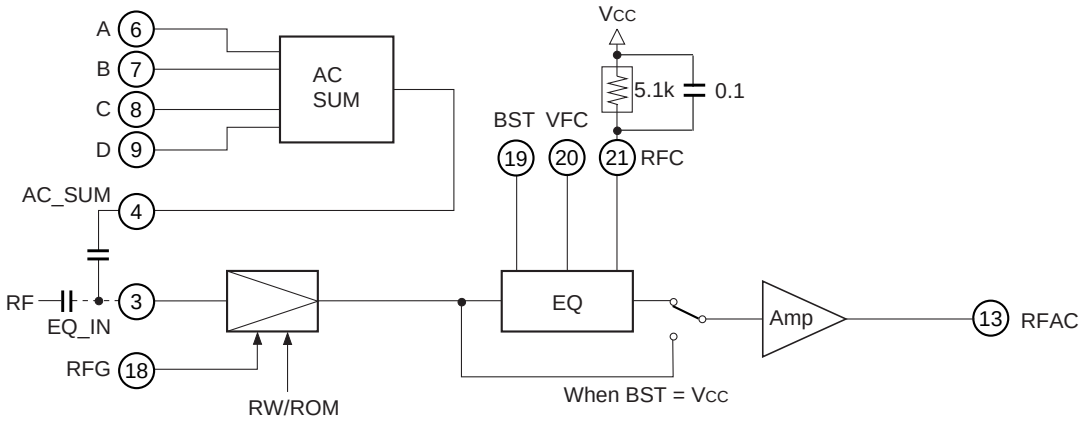




Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Description of Functions**

**• RFAC**

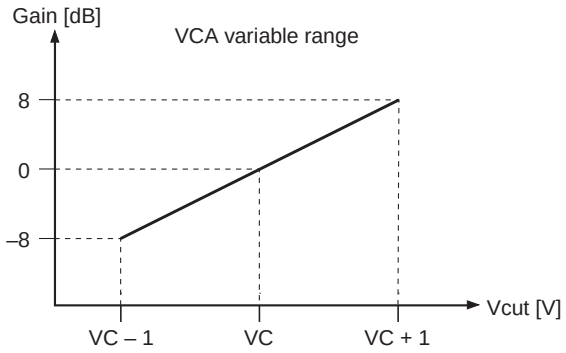
The RF signal input by connecting capacitance to the EQ_IN pin is equalized, arithmetically amplified and then output from the RFAC pin.




Low-frequency gain
AC_SUM: 16dB (both ROM/RW)
VCA to RFAC ROM: 2dB
RW: 14dB

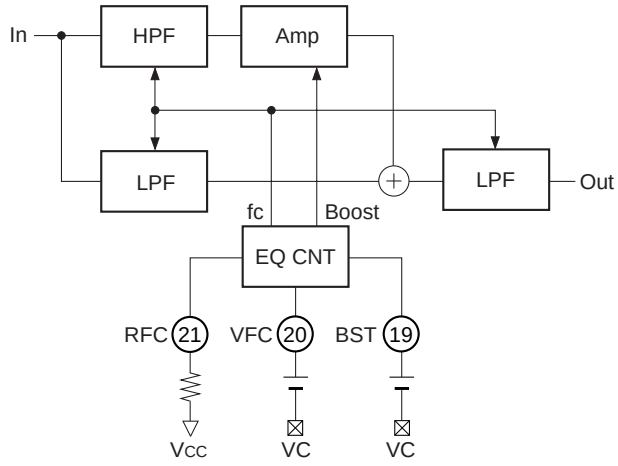
The EQ can be bypassed by connecting the BST control pin (Pin 19) to Vcc. In this case only the EQ block enters sleep mode and the low power consumption mode (slim mode) is activated. The low-frequency gain is the same value as for EQ ON mode.
The RF_SUM input dynamic range is VC ± 300mV (typ.).
If RF (summing signal) is present at the pickup output pin, input the addition output signal to the EQ_IN pin (Pin 3) coupled by capacitance.
When using a pickup without a summing output function, perform addition with the AC SUM block and then input the signal to the EQ_IN pin coupled by capacitance.
RW/ROM switching is done by the VCA block, so either input method can be used without problem.
The RW gain is 12dB higher than the ROM gain.

The VCA low-frequency gain can be adjusted by the RFG pin (Pin 18) voltage.
The control voltage vs. low-frequency gain characteristics are shown in the graph to the right.




The RFAC pin (Pin 13) is an NPN transistor emitter follower output.
The maximum drive current is approximately 2mA.
If the load capacitance distorts the output waveform, increase the drive current.
Connect resistance between Pin 13 and GND.

• **EQ**

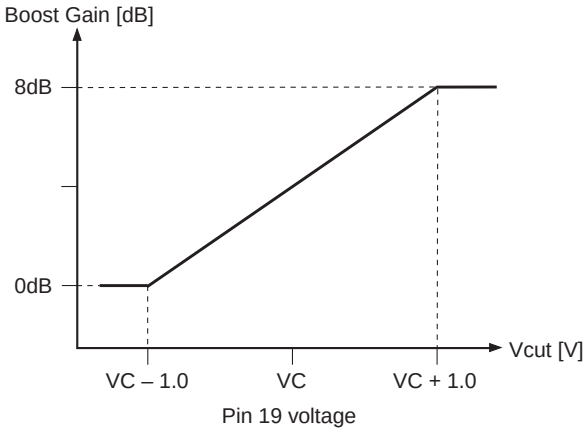



The diagram to the left shows the EQ internal block diagram.
The EQ consists of a combination of HPF and LPF.
The HPF and LPF transmittance is the Bessel function.
The boost gain can be adjusted by adjusting the HPF gain.
The boost frequency is adjusted by the RFC external resistance value and the VFC control voltage value.

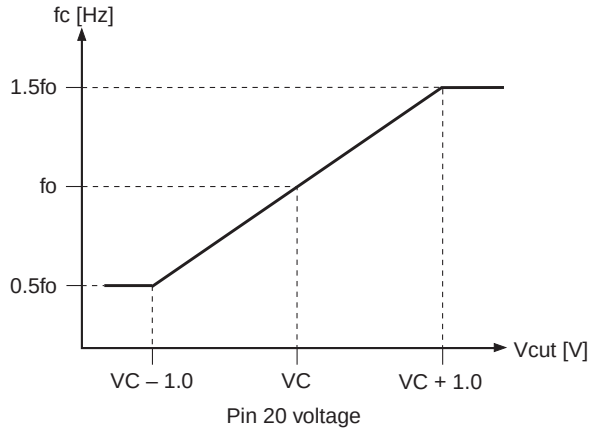
RFC resistance value: The cut-off frequency fo of each filter is adjusted by the Pin 21 external resistance value. The VFC voltage can be varied using this fo as the reference.

VFC voltage: fo can be changed by the voltage applied to Pin 20.

The boost gain can be adjusted by the BST pin control voltage.
The control characteristics are shown in the graph below.

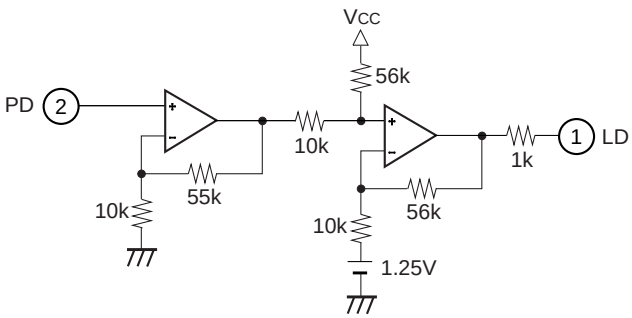



The cut-off frequency control characteristics are shown in the graph below.



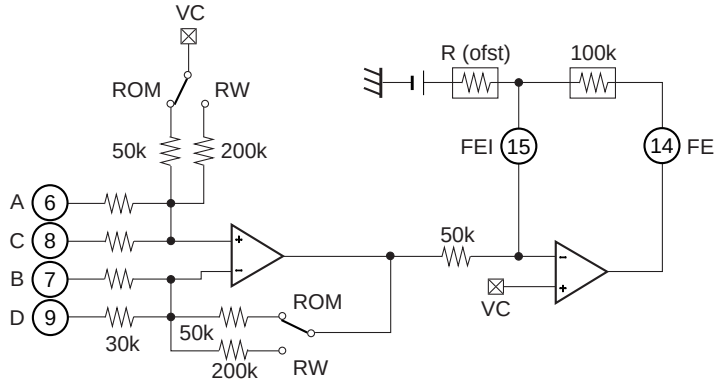

• **APC (Automatic Power Control)**

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics. Therefore, the current must be controlled to maintain the monitor photodiode output at a constant level. This control is performed by the APC function



**• Focus Error**

The signals input to the A and C pins and the B and D pins are arithmetically amplified and the focus error signal is output.
This circuit has RW/ROM switching, low-frequency gain adjustment and offset adjustment (external resistance) functions.

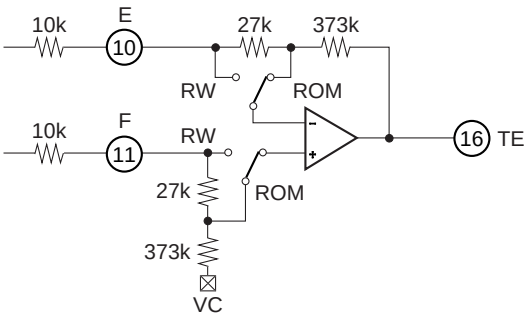



FE = Gain {(B + D) – (A + C)}

| | |
|---|---|
| Low-frequency gain | ROM: 16dB |
| | RW: 28dB |
| Cut-off frequency fc (typ.) | ROM: 400kHz |
| | RW: 300kHz |

**• Tracking Error**

The signals input to the E and F pins are arithmetically amplified and the tracking error signal is output.
This circuit has RW/ROM switching, low-frequency gain adjustment and offset adjustment (external resistance) functions.

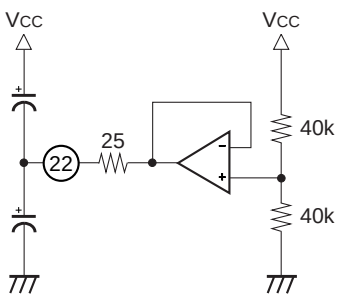



TE = Gain (F – E)

| | |
|---|---|
| Low-frequency gain | ROM: 20dB |
| | RW: 32dB |
| fc (typ.) | ROM: 1MHz |
| | RW: 250kHz |

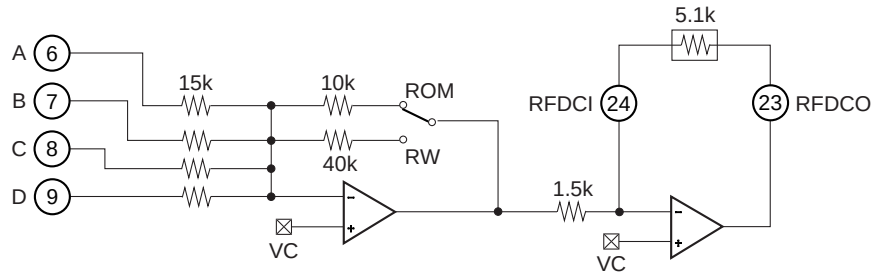
**• VC Buffer**

This outputs the VC ((1/2) $V_{CC}$) voltage.
The maximum output current is approximately ±3mA.



• **RFDC**

The signals input via the A, B, C and D pins are added, amplified and the RFDC signal is output.
RW/ROM switching, low-frequency gain adjustment and offset adjustment are possible.



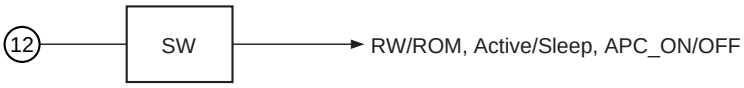

RFDC = Gain (A + B + C + D)

| | |
|---|---|
| Low-frequency gain | ROM: 20dB |
| | RW: 32dB |
| fc (Typ.) | ROM: 12MHz |
| | RW: 5MHz |

The gain can be adjusted by the external resistance connected between Pins 23 and 24.

• **SW**

This controls the laser (APC) on/off, active/sleep mode, and RW/ROM mode switching.
Switching is controlled by the voltage applied to the SW pin (Pin 12).




The VC buffer is kept active even in sleep mode.
In the function block, BGR and MODE_SW are always set to active mode.

| Item / Control voltage | APC | Active/Sleep | RW/ROM |
|---|---|---|---|
| $V_{CC}$ | ON | Active | RW |
| VC or Hi-Z | OFF | Sleep | — |
| GND | ON | Active | ROM |

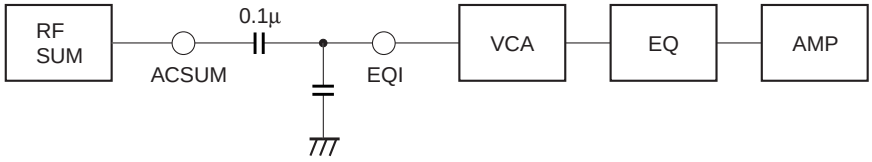
## Notes on Operation

### Stabilizing the RFAC signal

The RFAC system (RFSUM + EQ) is comprised entirely of non-inverted function blocks.
This is in order to support pickups with built-in RFSUM.
Therefore, if the voltage gain of each block is increased, a feedback loop is formed over the entire RFAC system causing the RFAC signal to become unstable (oscillate).
In these cases, it is recommended to lower the EQ frequency response and the boost gain. This has a large effect on the board (power supply, I/O signal cross talk, etc.) loop. The RFAC signal easily becomes unstable if the VCA gain is increased, the EQ boost frequency is set to a high frequency, the EQ boost amount is increased, etc.
The VCA gain is low in ROM mode, so the RFAC signal is stable. Also, when not using RFSUM, the RFAC signal is stabilized because the overall gain is low.
The area where the RFAC signal becomes unstable is thought to vary for each set, as this is greatly affected by the board loop as noted above.

### Proposed stabilization measures

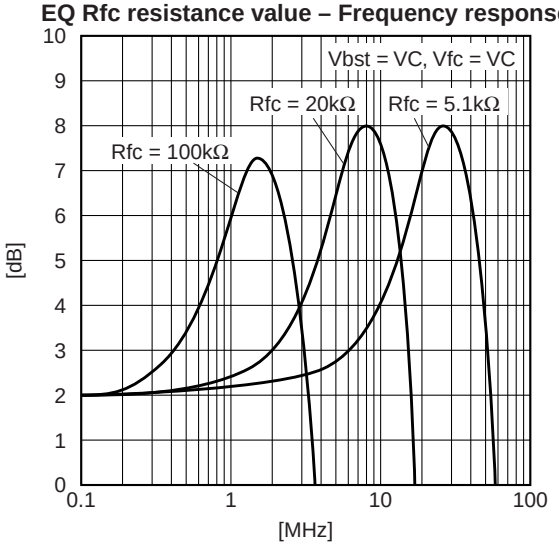
The board and other loop characteristics can be changed by adding external capacitance as noted below.
This has a particularly large effect on the stabilization when using RFSUM.



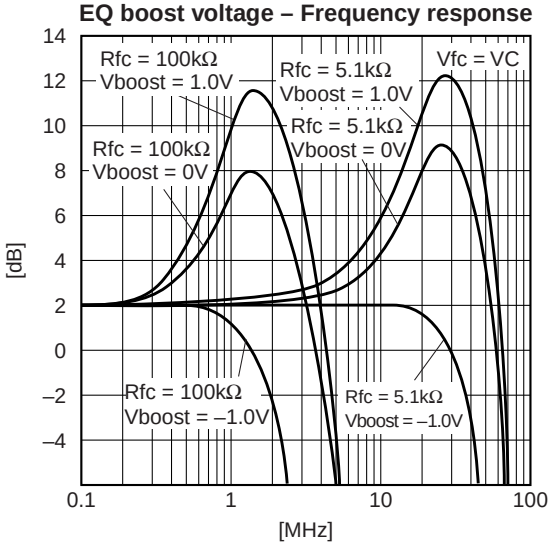

Add capacitance of 10pF to 20pF.

## Example of Representative Characteristics

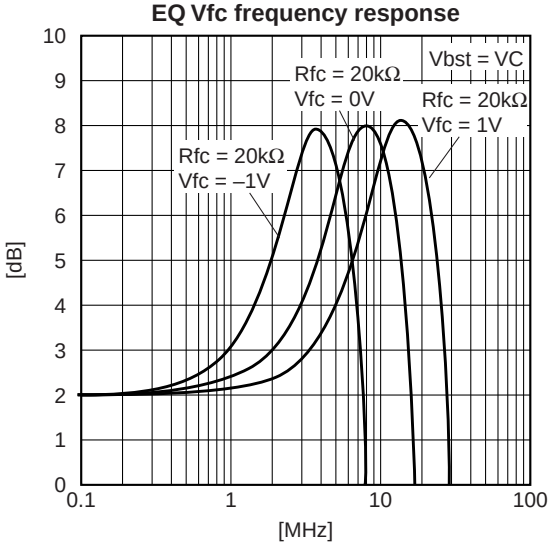
**EQ Rfc resistance value – Frequency response**



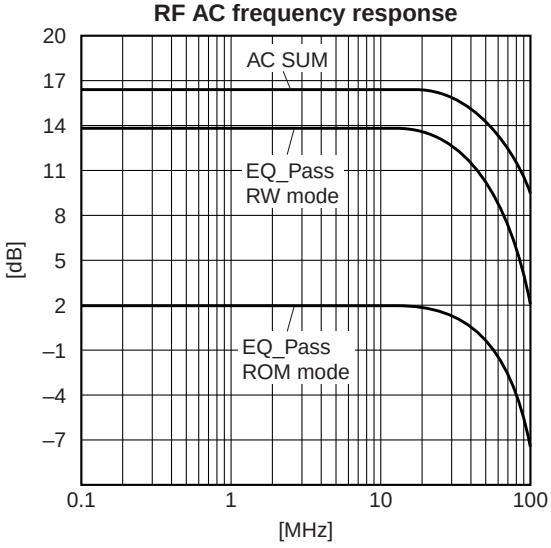

**EQ boost voltage – Frequency response**



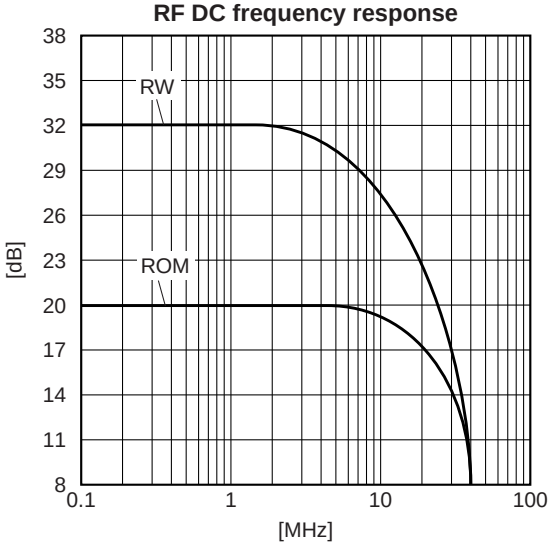

**EQ Vfc frequency response**



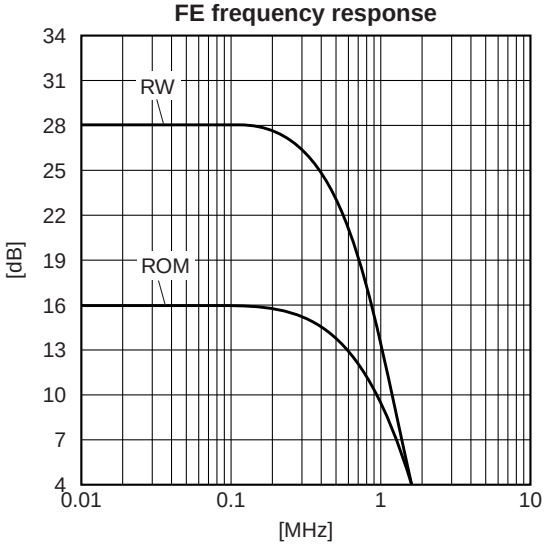

**RF AC frequency response**



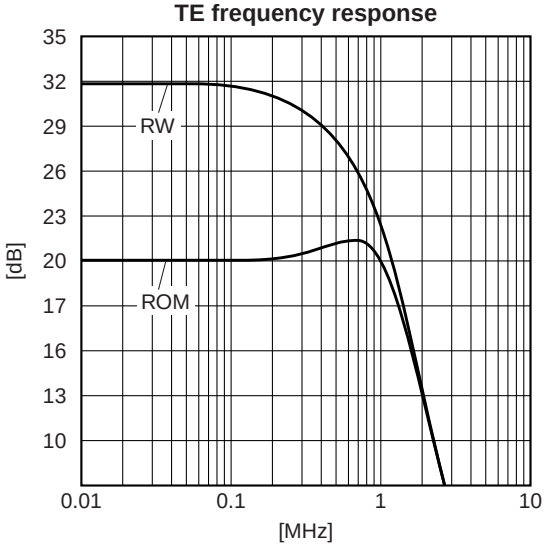

**RF DC frequency response**



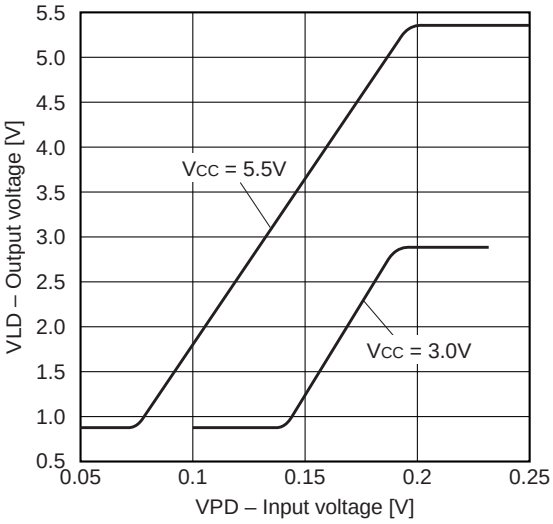

**FE frequency response**



**TE frequency response**

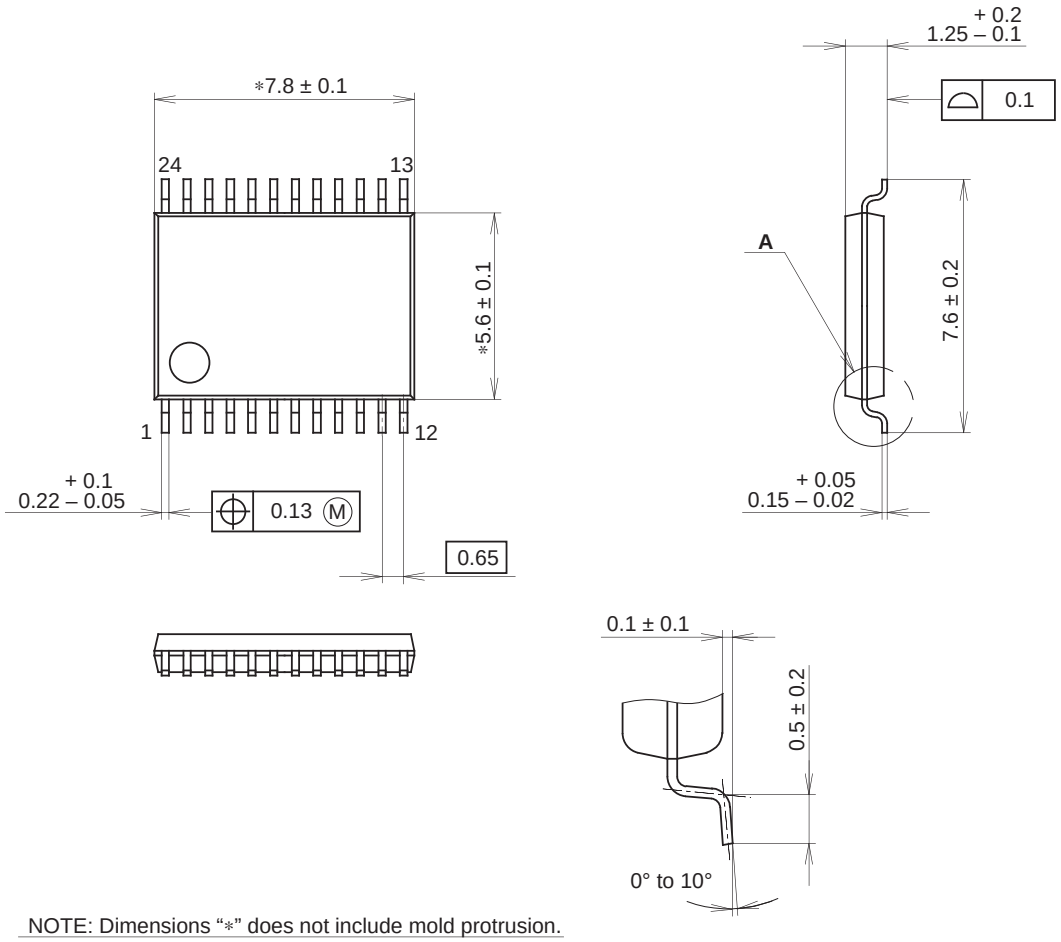



**APC I/O characteristics**



**Package Outline** Unit: mm

24PIN SSOP(PLASTIC)




NOTE: Dimensions "∗" does not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.1g |

| | |
|---|---|
| SONY CODE | SSOP-24P-L01 |
| EIAJ CODE | SSOP024-P-0056 |
| JEDEC CODE | ———— |

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).