SONY

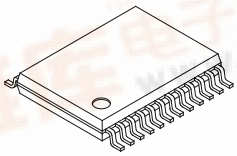
CXA3001N

RX Gain Control Amplifier

Description

CXA3001N is an RX gain control amplifier for CDMA cellular mobile phone.

24 pin SSOP (Plastic)



Features

- Wide gain control range
- Linear gain slope
- Noise figure Typ. 6dB at Gain = 45dB
- Output IP_3 Typ. +2dBm at Gain = 40dB
- 2 input ports
- Power save function included

Absolute Maximum Ratings

• Supply voltage	V_{CC}	6	V
• Operating temperature	Topr	–40 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	420	mW
• Supply voltage range		–0.3 to 6	V
• Logic input voltage		–0.3 to V_{CC} +0.3	V
• Signal input voltage		–0.3 to V_{CC} +0.3	V
• Differential signal input voltage		0 to 2.5	V

Operating Conditions

Supply voltage		3.1 to 3.8	V

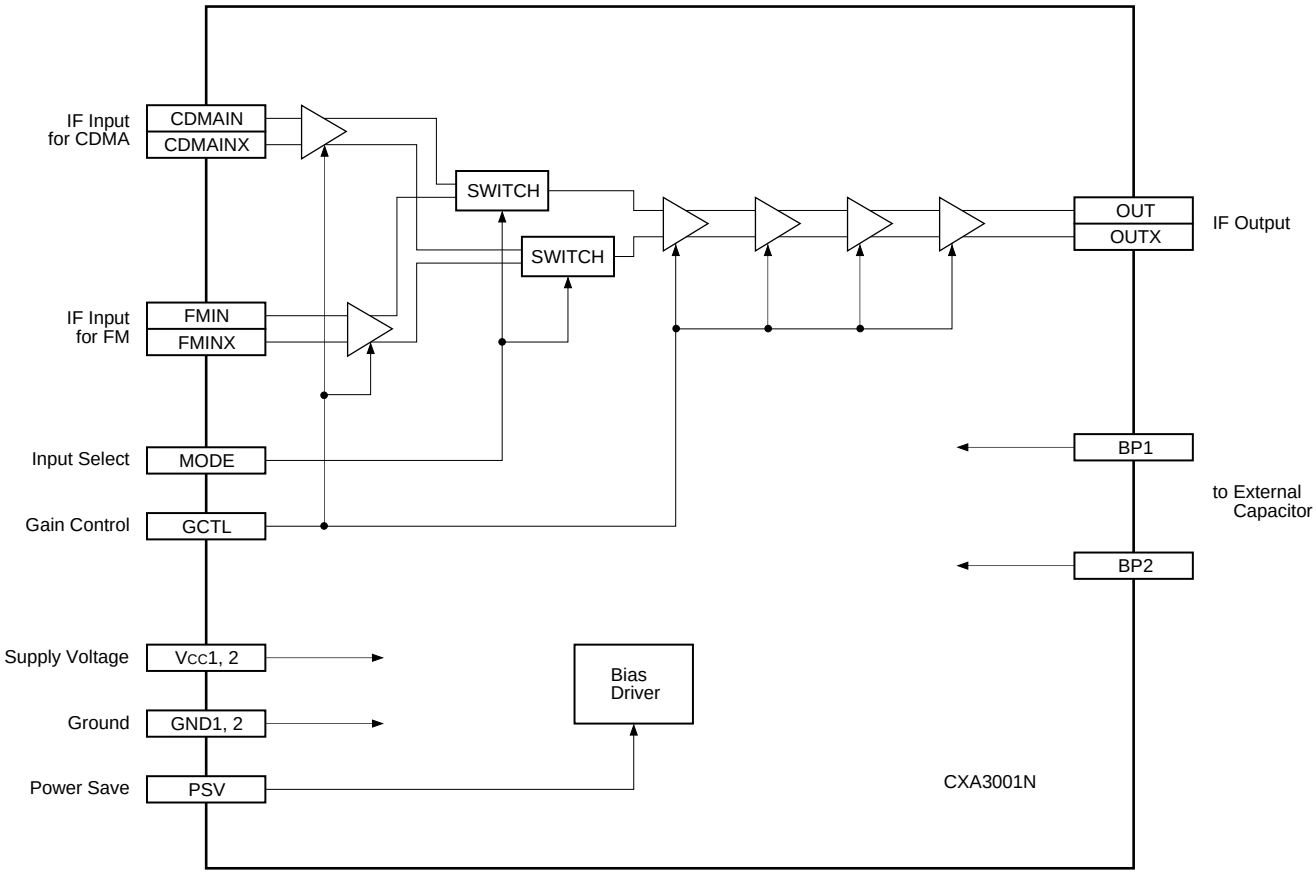
Applications

- CDMA cellular mobile phone
- CDMA & AMPS cellular phone

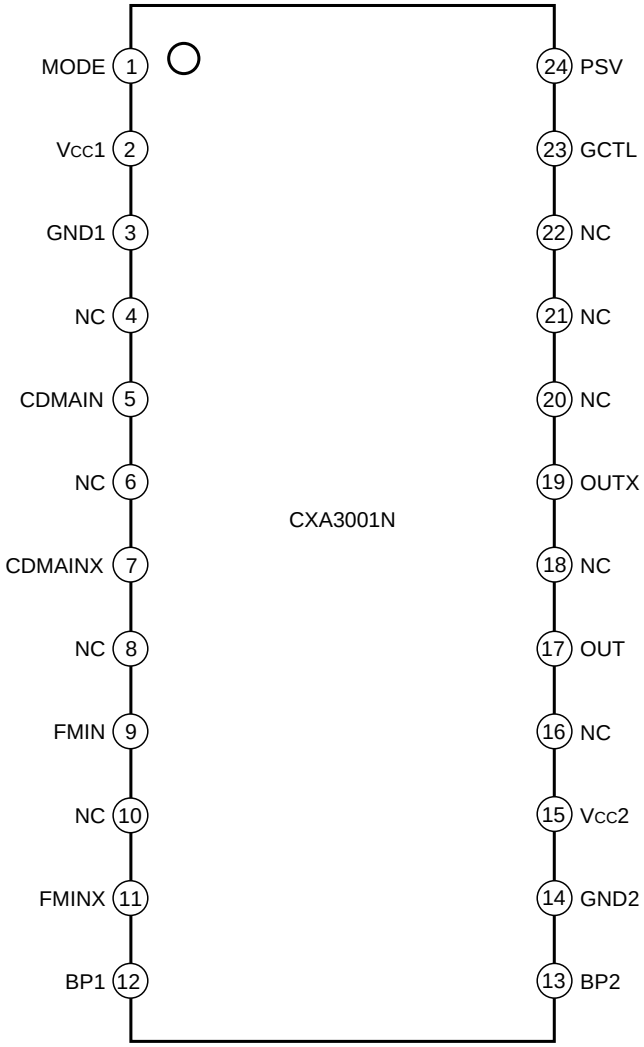
Structure

Bipolar sillicon monolithic IC

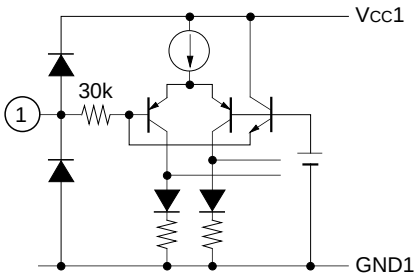
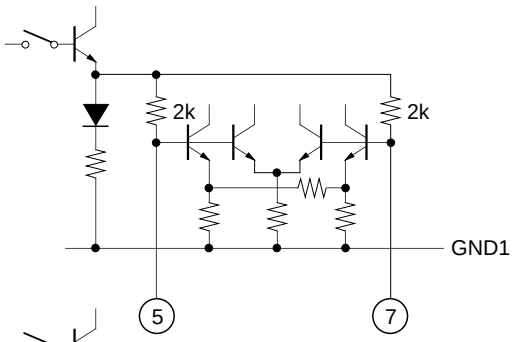
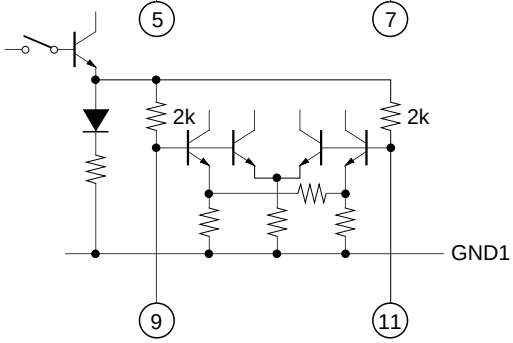
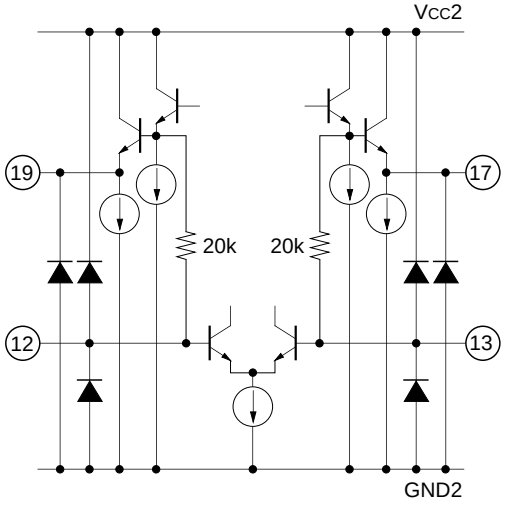
Block Diagram

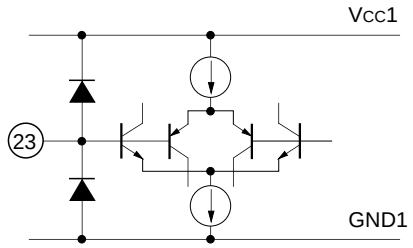
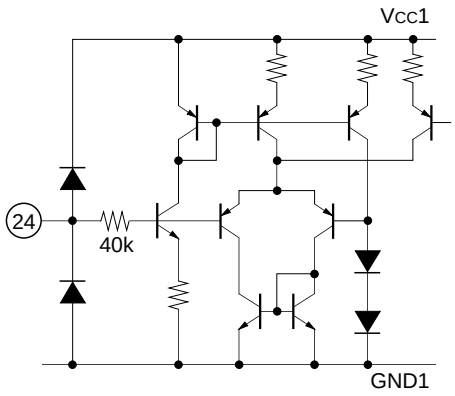


Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage Typ. (V)	Equivalent circuit	Description
1	MODE			Input select pin. CDMAIN for High. FMIN for Low.
2	Vcc1	3.6		Positive power supply.
3	GND1	0		Ground.
4 6 8 10	N.C.			No connection.
5	CDMAIN	1.2		Differential input pins for received CDMA IF signal.
7	CDMAINX	1.2		
9	FMIN	1.2		Differential input pins for received FM IF signal.
11	FMINX	1.2		
12	BP1	2.4		Connected to GND with capacitor 0.01µF.
13	BP2			
14	GND2	0		Ground for output stage.
15	Vcc2	3.6		Positive power supply for output stage.
16	N.C.			No connection.
17	OUT	1.7		Differential output pins for received IF signal.
19	OUTX	1.7		

Pin No.	Symbol	Pin voltage Typ. (V)	Equivalent circuit	Description
18 20 21 22	N.C.			No connection.
23	GCTL			Gain control pin with a ripple filter.
24	PSV			Power save function pin. High: Active Low: Power save

Electrical Characteristics

DC characteristics

(V_{CC} = 3.6V, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	$I_{CC}1$	V_{GCTL} = 1.5V, Pin 2	10	14	19	mA
Current consumption 2	$I_{CC}2$	V_{GCTL} = 1.5V, Pin 15	4.7	6.6	9.0	
Current consumption 3	$I_{CC}3$	V_{PSV} = 0.5V, Pin 2			1	µA
Current consumption 4	$I_{CC}4$	V_{PSV} = 0.5V, Pin 15			1	
Input current pin 1H	$I_{MODE\ H}$	V_{MODE} = 3V			10	
Input current pin 1L	$I_{MODE\ L}$	V_{MODE} = 0.5V	–20			
Input current pin 23H	$I_{GCTL\ H}$	V_{GCTL} = 3V			10	
Input current pin 23L	$I_{GCTL\ L}$	V_{GCTL} = 0.5V	–10			
Input current pin 24H	$I_{PSV\ H}$	V_{PSV} = 3V			10	
Input current pin 24L	$I_{PSV\ L}$	V_{PSV} = 0.5V	–10			
MODE high voltage	V_{MH}	Pin 1	3			V
MODE low voltage	V_{ML}	Pin 1			0.5	
PSV high voltage	V_{PSH}	Pin 24	3			
PSV low voltage	V_{PSL}	Pin 24			0.5	

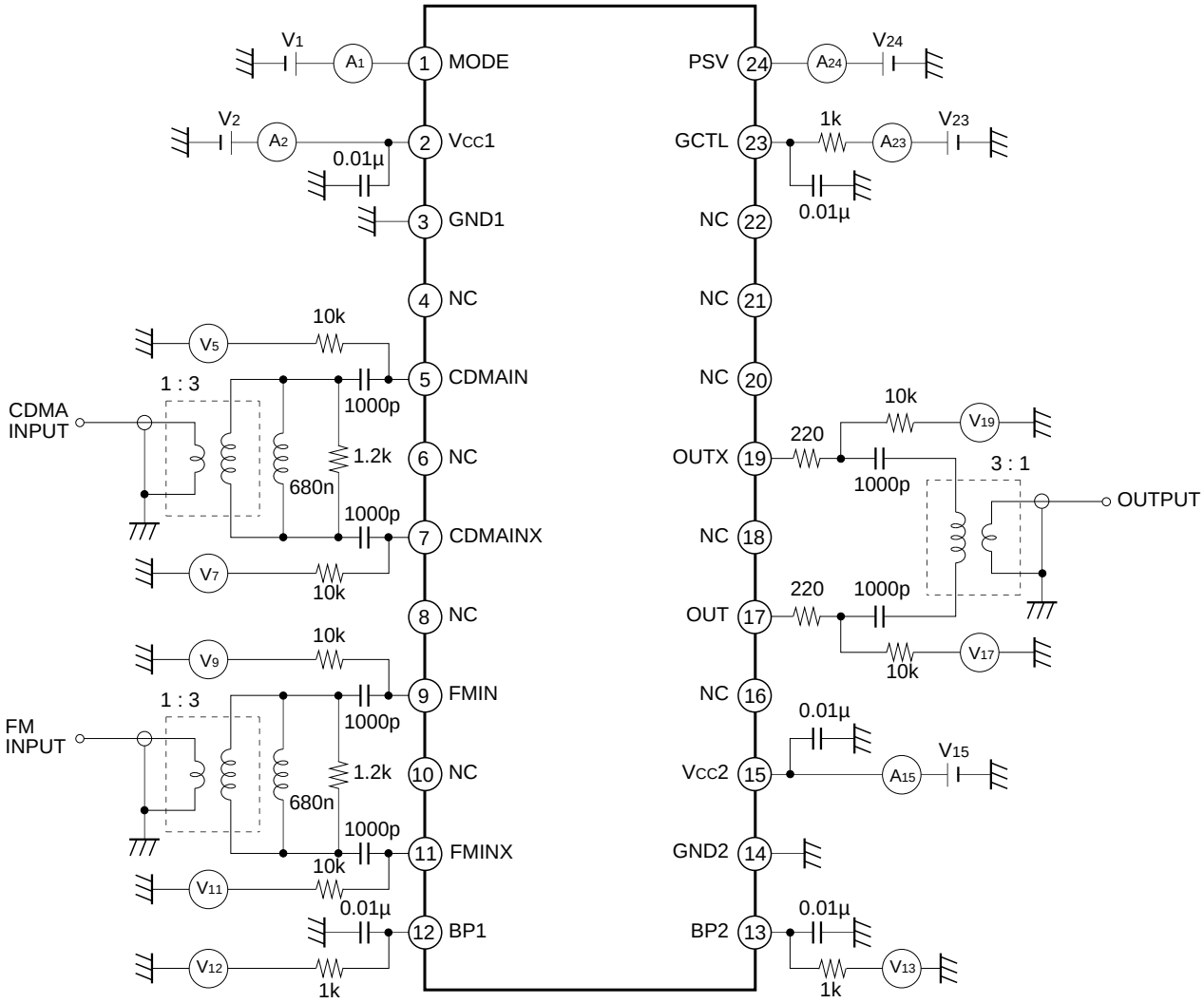
AC characteristics

(V_{CC} = 3.6V, Ta = 25°C)

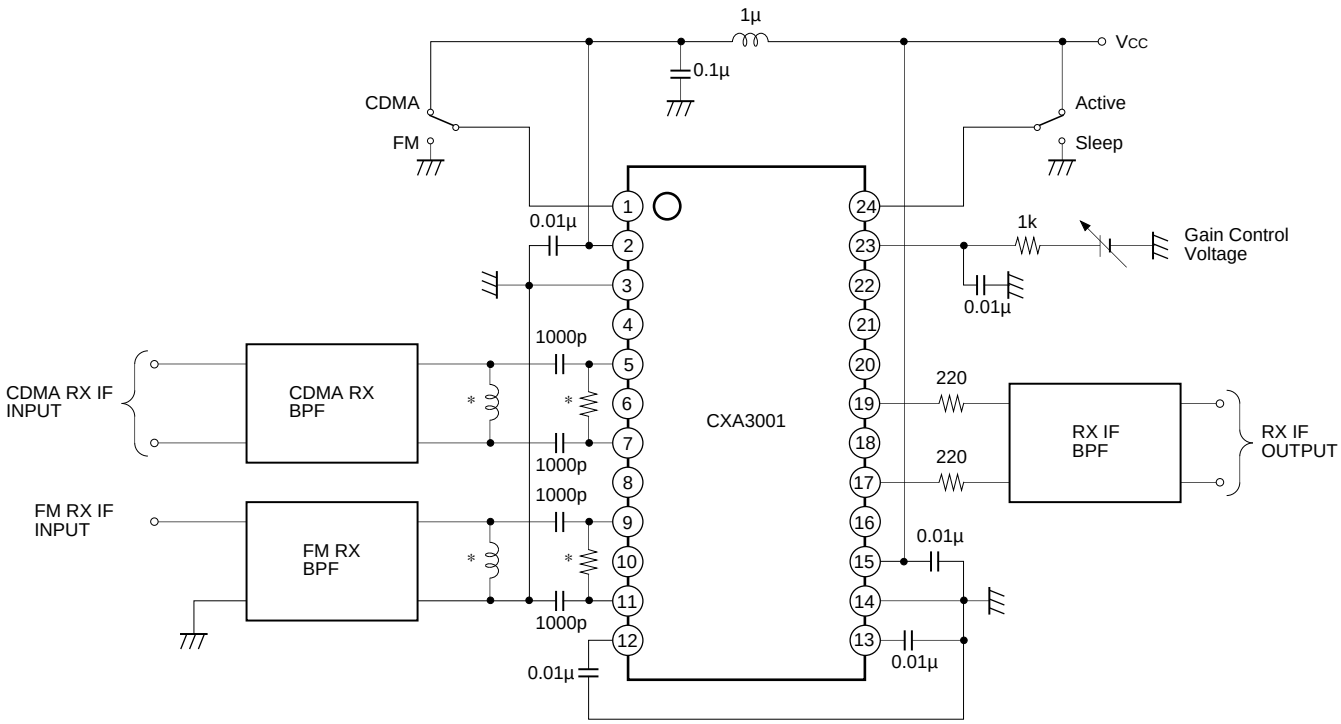
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating frequency range	F_R		10		100	MHz
Gain CDMA2.3	$G_{CDMA2.3}$	V_{MODE} = "H" f = 85.38MHz V_{GCTL} = 2.3V Level = –50dBm	37	41	46	dB
Gain CDMA1.5	$G_{CDMA1.5}$	V_{MODE} = "H" V_{GCTL} = 1.5V Level = –30dBm	–7.5	–3	1.5	
Gain CDMA0.7	$G_{CDMA0.7}$	V_{MODE} = "H" V_{GCTL} = 0.7V Level = –10dBm	–55	–49	–44	
CDMA Gain slope	G_{CLIN}	V_{MODE} = "H" V_{GCTL} = 1 to 2V	57	60	63	dB/V
Gain FM2.3	$G_{FM2.3}$	V_{MODE} = "L" f = 85.38MHz V_{GCTL} = 2.3V Level = –50dBm	37	41	46	dB
Gain FM1.5	$G_{FM1.5}$	V_{MODE} = "L" V_{GCTL} = 1.5V Level = –30dBm	–7.5	–3	1.5	
Gain FM0.7	$G_{FM0.7}$	V_{MODE} = "L" V_{GCTL} = 0.7V Level = –10dBm	–55	–49	–44	
FM Gain slope	G_{FMLIN}	V_{MODE} = "L" V_{GCTL} = 1 to 2V	57	60	63	dB/V
Input level 3rd order intercept point	IIP_3	V_{MODE} = "H" G_{CDMA} = 40dB* F_1 = 86.38MHz F_2 = 87.38MHz Measure of 85.38MHz	–42	–38		dBm
Noise Figure	NF	V_{MODE} = "H" G_{CDMA} = 40dB* Used 1MHz BPF Measure of 85.38MHz		6.5	9.5	dB

* Adjust GCTL voltage, and set the overall gain to 40dB.

Measurement Circuit



Application Circuit



* Must be adjusting values to result a best impedance matching between BPF filter and this IC.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Design Reference Values

Single ended measurement (V_{CC} = 3.6V, Ta = 25°C)

Item	Symbol	Conditions	Typ.	Unit
Input resistance	R_{IN}	f = 85.38MHz, V_{GCTL} = 1.5V	900	Ω
Input capacitance	C_{IN}		9	pF
Output resistance	R_{OUT}		30	Ω

Notes on Operation

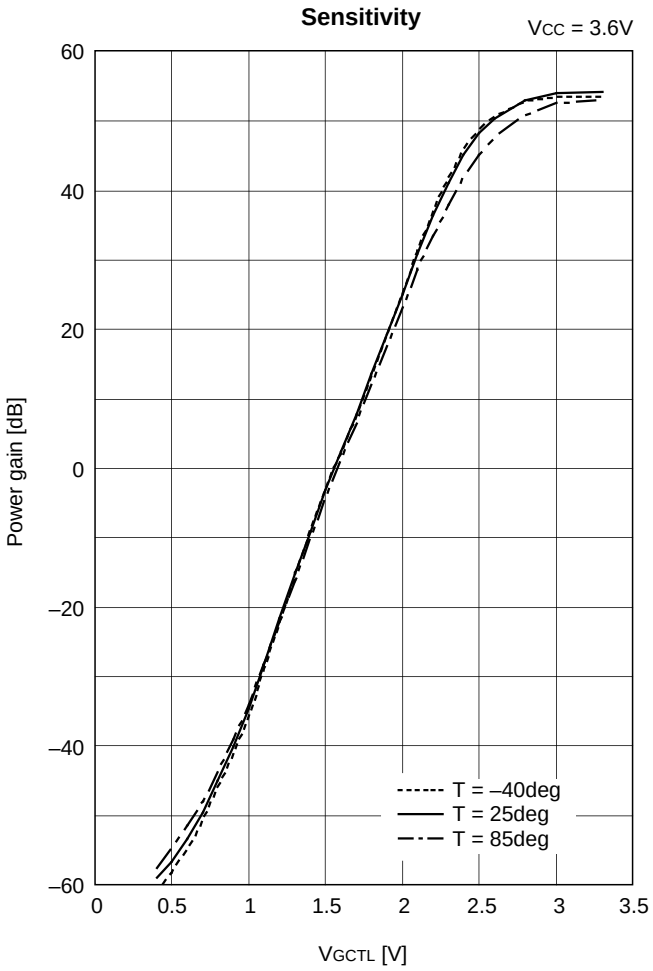
1) This IC is a wideband amplifier with wide gain control range. Separate Pin 3 (GND1) and Pin 14 (GND2) to prevent interference between input and output. Furthermore, the decoupling capacitors between Pins 2 and 3, Pins 14 and 15 should be as close to the IC as possible.

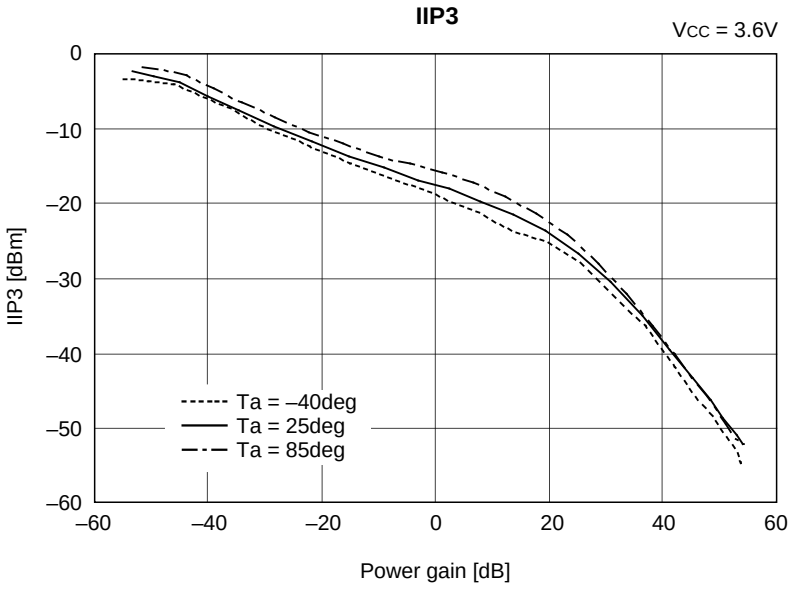
2) The resistors connected to Pins 17 and 19 should be as close to the IC as possible.

3) This IC assumes the excellent characteristics when the differential input impedance between Pins 5 and 7, Pins 9 and 11 is 500Ω. Refer to the Measurement Circuit for the external element settings, etc.

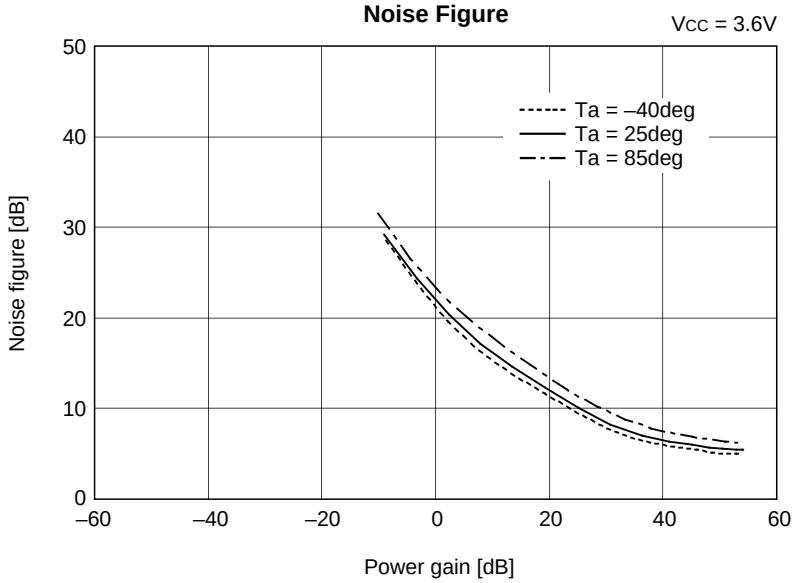
4) Connect the capacitors, which are connected to Pins 12 and 13, to Pin 14 (GND2).

5) Pay attention to handling this IC because its electrostatic discharge strength is weak.

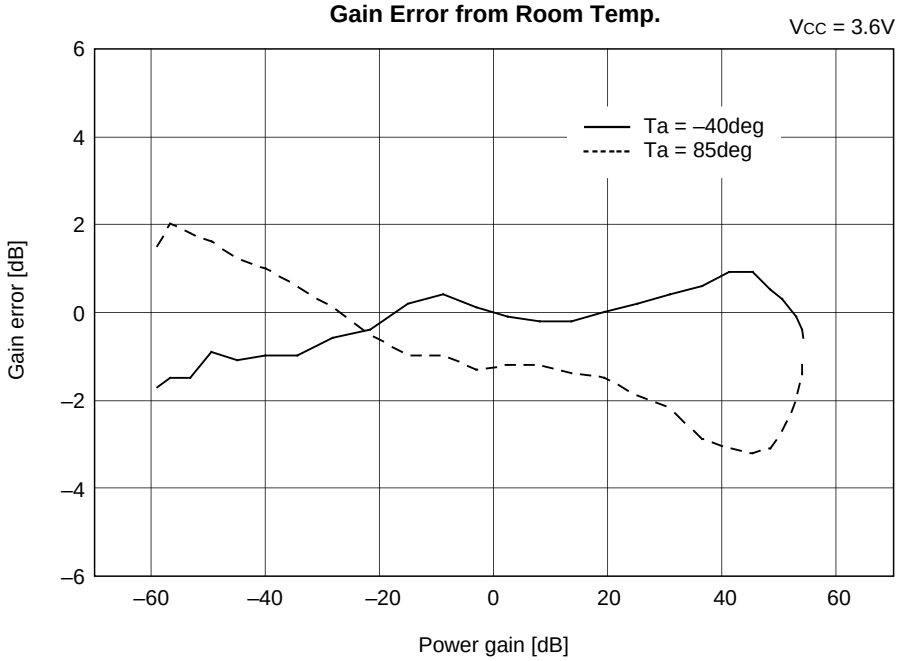

Sensitivity
VCC = 3.6V
60
40
20
0
–20
–40
–60
Power gain [dB]
0
0.5
1
1.5
2
2.5
3
3.5
VGCTL [V]
T = –40deg
T = 25deg
T = 85deg


IIP3
VCC = 3.6V
0
–10
–20
–30
–40
–50
–60
IIP3 [dBm]
–60
–40
–20
0
20
40
60
Power gain [dB]
Ta = –40deg
Ta = 25deg
Ta = 85deg

Noise Figure

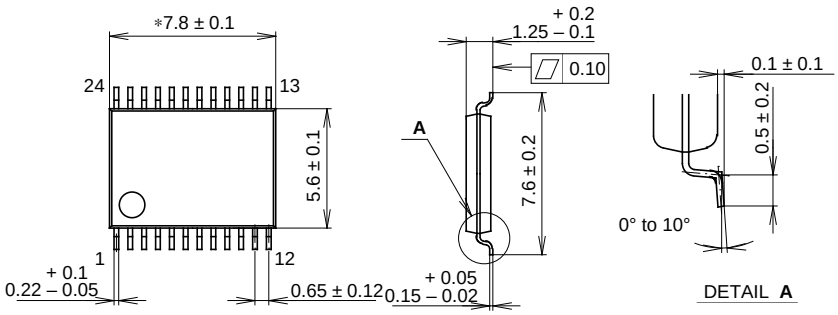


Gain Error from Room Temp.



Package Outline Unit: mm

24PIN SSOP (PLASTIC) 275mil



NOTE : ∗NOT INCLUDE MOLD FINS.

SONY CODE	SSOP-24P-L01
EIAJ CODE	A SIMILAR TO SSOP024-P-0300
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————