SONY

CXA3117N

IF Amplifier for M-ary FSK Pagers

Description

The CXA3117N is a low current consumption FM IF amplifier which employs the newest bipolar process. It is suitable for M-ary FSK pagers.

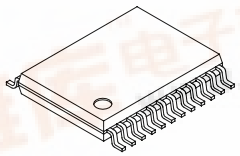
Features

- Low current consumption: 1.1mA (typ. at Vcc = 1.4V)
- Low voltage operation: Vcc = 1.1 to 4.0V
- Small package 24-pin SSOP
- Second mixer and oscillator
- Needless of IF decoupling capacitor
- Reference power supply for operational amplifier and comparator
- Bit rate filter with variable cut-off
- Misoperation prevention function for continuous data
- RSSI function
- IF input, Vcc standard

Applications

- M-ary FSK pagers
- Double conversion pagers

24 pin SSOP (Plastic)



Structure

Bipolar silicon monolithic IC

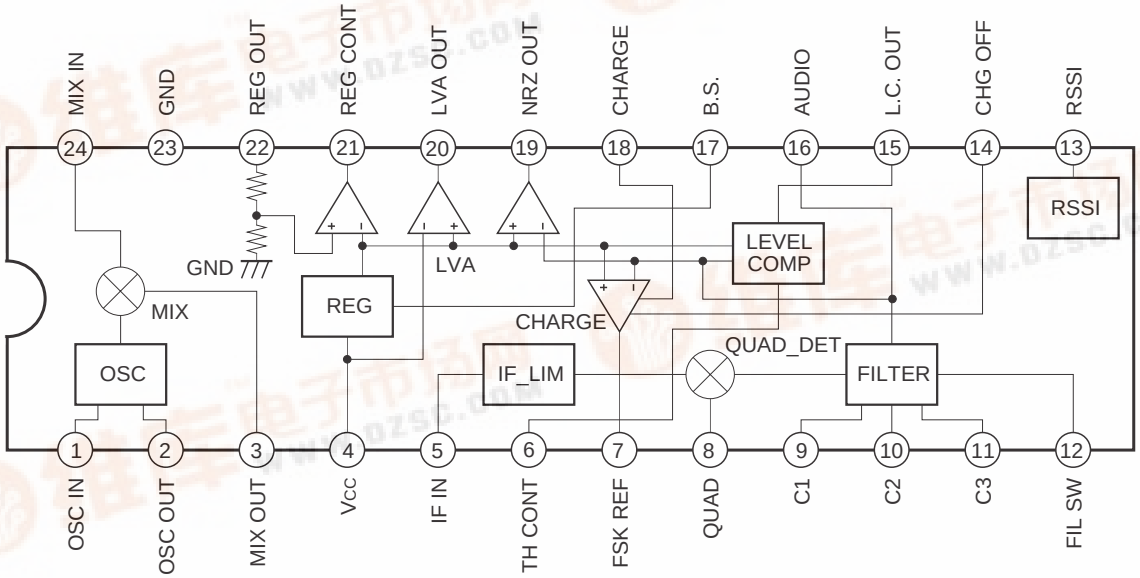
Absolute Maximum Ratings

• Supply voltage	Vcc	7.0	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	PD	417	mW

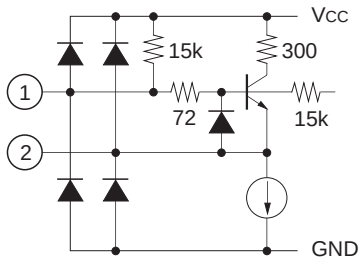
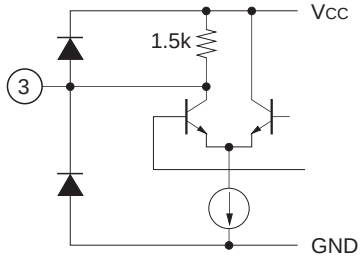
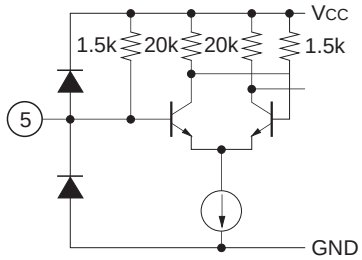
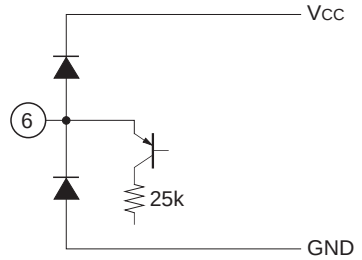
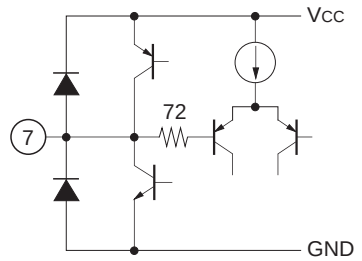
Operating Condition

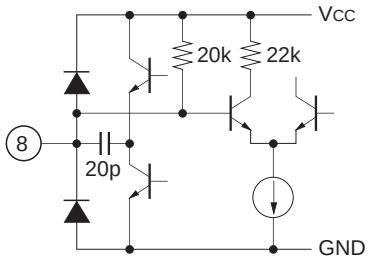
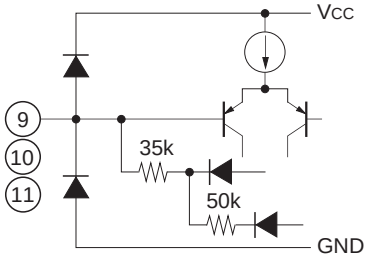
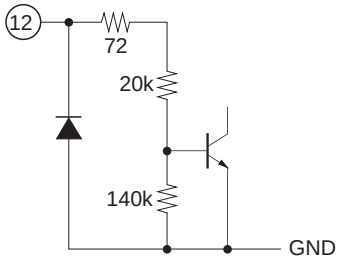
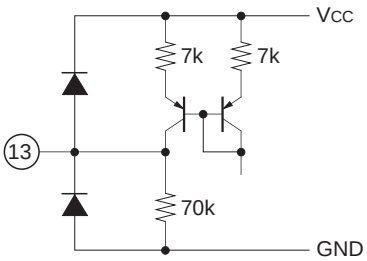
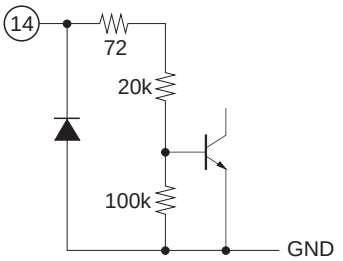
Supply voltage	Vcc	1.1 to 4.0	V

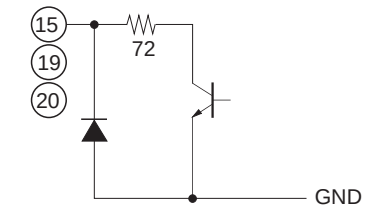
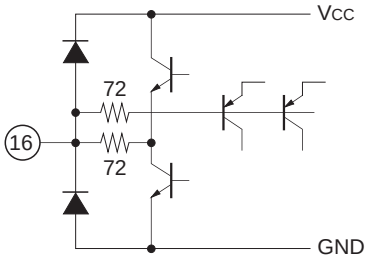
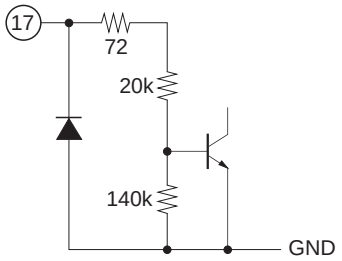
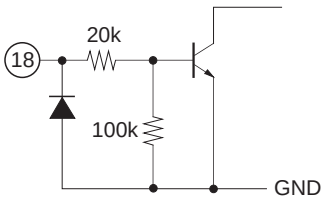
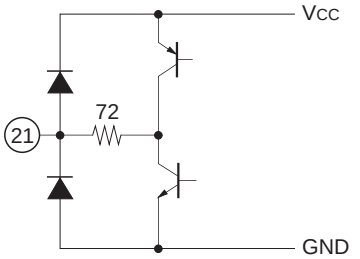
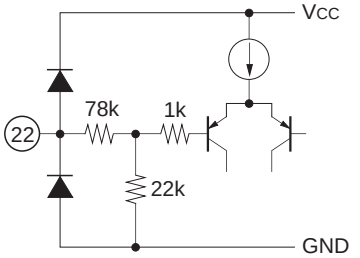
Block Diagram and Pin Configuration

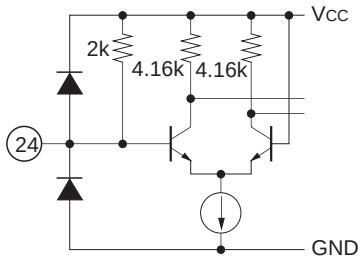


Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	OSC IN	1.4V		Connects the external parts of crystal oscillator circuit. A capacitor and crystal oscillator are connected to these pins and Vcc.
2	OSC OUT	0.7V		
3	MIX OUT	1.3V		Mixer output. Connect a 455kHz ceramic filter between this pin and IF IN.
4	Vcc			Power supply.
5	IF IN	1.4V		IF limiter amplifier input.
6	TH CONT	—		Determines the level comparator threshold value. Threshold value can be adjusted by inserting the resistor between Pin 6 and Vcc. Normally, short to Vcc.
7	FSK REF	0.2V		Connects the capacitor that determines the low cut-off frequency for the entire system.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
8	QUAD	1.4V		Connects the phase shifter of FM detector circuit.
9 10 11	C1 C2 C3	0.2V		Connects the capacitor that determines the LPF cut-off.
12	FIL SW	—		Switches the LPF cut-off. Cut-off is decreased by setting this pin high. (Applied voltage range: –0.5V to +7.0V)
13	RSSI	0.1V		RSSI circuit output.
14	CHG OFF	—		Sets off the quick charge circuit current. The charge current is off by setting Pin 18 low and Pin 14 high.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15 19 20	L.C. OUT NRZ OUT LVA OUT	— — —		Level comparator, NRZ comparator and LVA comparator outputs. They are open collectors. (Applied voltage range: –0.5V to +7.0V)
16	AUDIO	0.2V		Level comparator and NRZ comparator inputs. The filter circuit output is connected.
17	B.S.	—		Controls the battery saving. Setting this pin low suspends the operation of IC. (Applied voltage range: –0.5V to +7.0V)
18	CHARGE	—		Controls the speed of the quick charge circuit. Set this pin high to execute the quick charge. (Applied voltage range: –0.5V to +7.0V)
21	REG CONT	—		Output for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity: 100µA)
22	REG OUT	1.0V		Constant-voltage source output. Controlled to maintain 1.0V.
23	GND	—		Ground

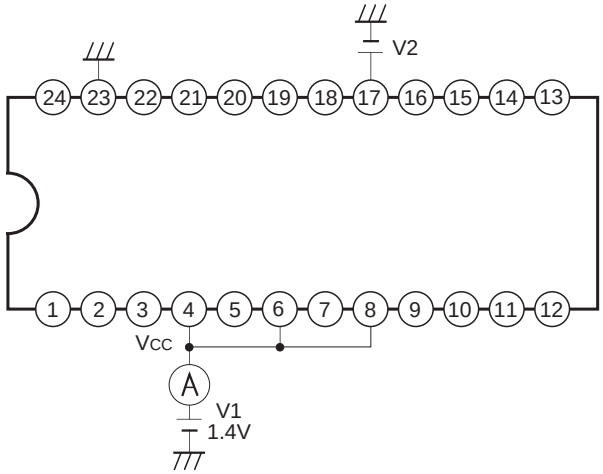
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	MIX IN	1.4V		Mixer input.

Electrical Characteristics

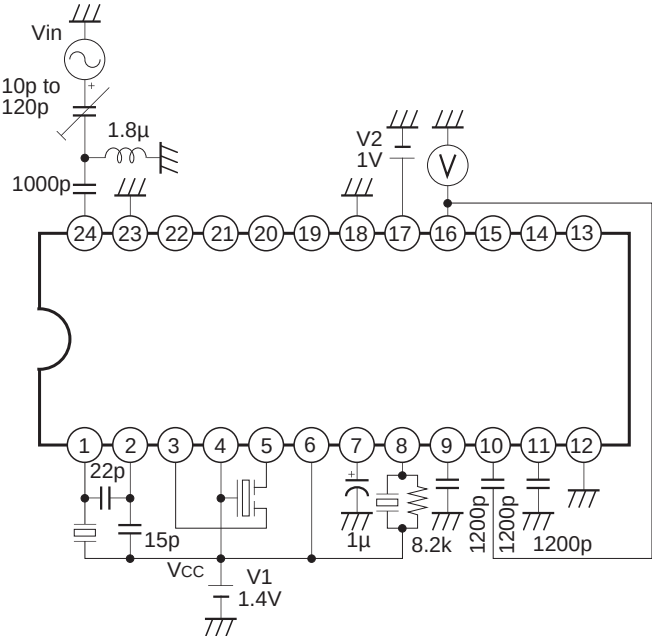
(V_{CC} = 1.4V, Ta = 25°C, Fs = 21.7MHz, F_{MOD} = 1.6kHz, F_{DEV} = 4.8kHz, AM_{MOD} = 30%)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	Measurement circuit 1, V2 = 1.0V	0.7	1.1	1.35	mA
Current consumption	I_{CCS}	Measurement circuit 1, V2 = 0V	—	6	20	µA
AM rejection ratio	AMRR	Measurement circuit 2, 30k LPF	25	—	—	dB
NRZ output saturation voltage	V_{SATNRZ}	Measurement circuit 4, Vin = 0.3V	—	—	0.4	V
NRZ output leak current	I_{LNRZ}	Measurement circuit 3, Vin = 0.1V	—	—	5.0	µA
NRZ hysteresis width	V_{TWNRZ}	Measurement circuit 3, Vin = 0.1 to 0.3V	0	10	20	mV
VB output current	I_{OUT}	Measurement circuit 5	100	—	—	µA
VB output saturation voltage	V_{SATVB}	Measurement circuit 5	—	—	0.4	V
REG OUT voltage	V_{REG}	Output current 0µA	0.92	0.97	1.02	V
LVA operating voltage	V_{LVA}	Measurement circuit 6, V1 = 1.4 to 1.0V	1.00	1.05	1.10	V
LVA output leak current	I_{LLVA}	Measurement circuit 6, V1 = 1.0V	—	—	5.0	µA
LVA output saturation voltage	V_{SATLVA}	Measurement circuit 7	—	—	0.4	V
Detector output voltage	V_{ODET}	Measurement circuit 2	50	63	80	mVrms
Logic input voltage high level	V_{THBSV}	—	0.9	—	—	V
Logic input voltage low level	V_{TLBSV}	—	—	—	0.35	V
Limiting sensitivity	$V_{IN\ (LIM)}$	Measurement circuit 2, Data filter fc = 2.4kHz	—	–108	—	dBm
Detector output level ratio deviation to level comparator window width	V_{LCWR}	When Pin 6 is shorted to Vcc	–15	0	+15	%
Level comparator output saturation voltage	V_{SATLC}	Measurement circuit 9	—	—	0.4	V
Level comparator output leak current	I_{LLC}	Measurement circuit 8	—	—	5.0	µA
RSSI output offset	V_{ORSSI}	Measurement circuit 10	—	150	300	mV
Mixer input resistance	R_{INLIM}	—	1.6	2.0	2.4	kΩ
Mixer output resistance	R_{OUTMIX}	—	1.2	1.5	1.8	kΩ
IF limiter input resistance	R_{INLIM}	—	1.2	1.5	1.8	kΩ

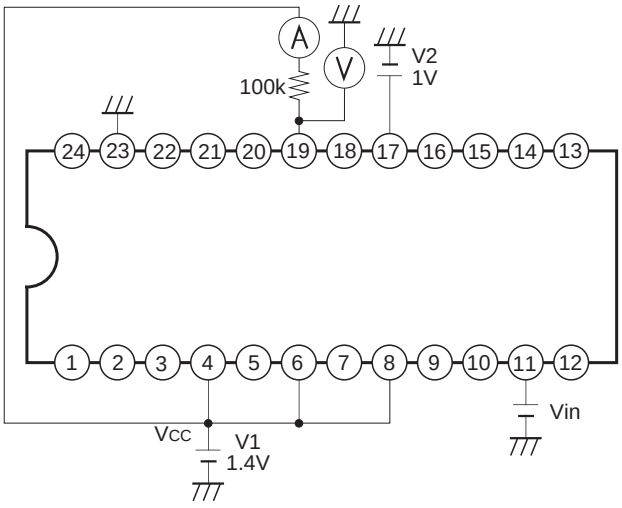
Electrical Characteristics Measurement Circuit



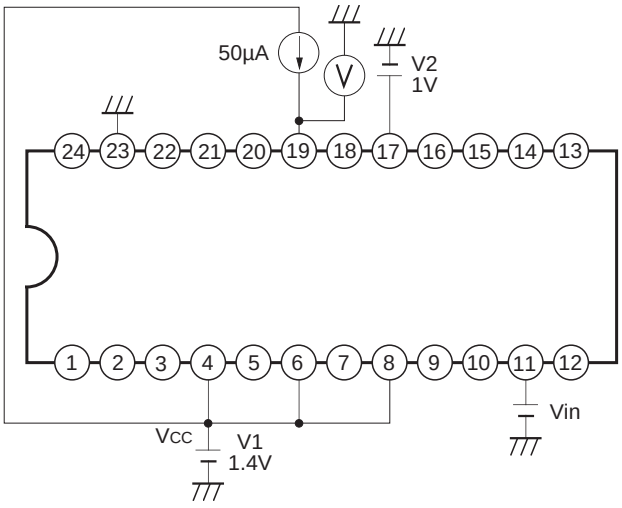
Measurement circuit 1



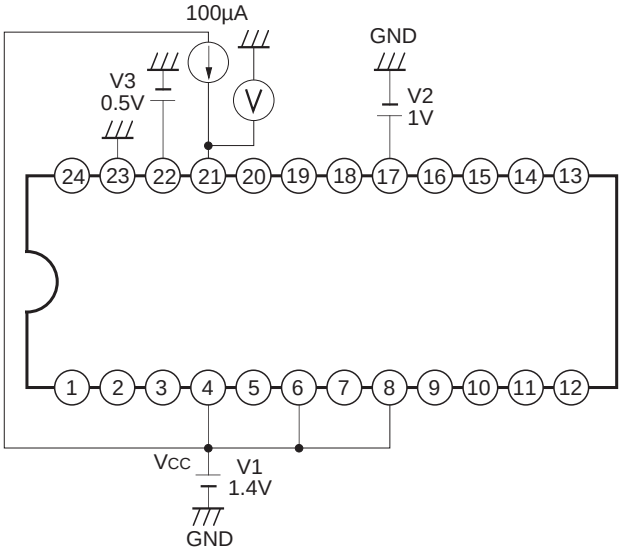
Measurement circuit 2



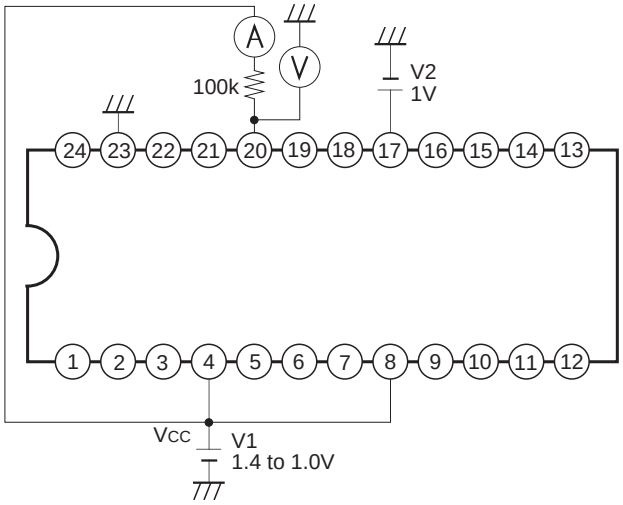
Measurement circuit 3



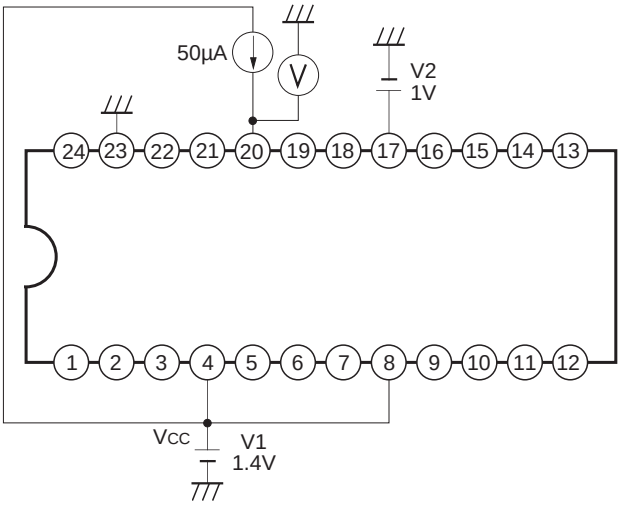
Measurement circuit 4



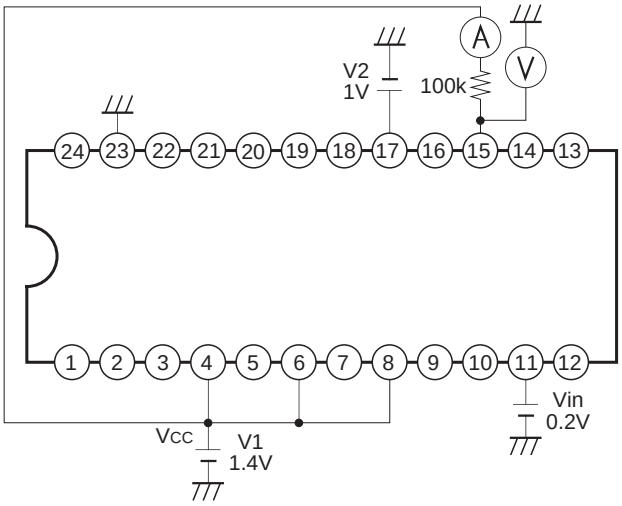
Measurement circuit 5



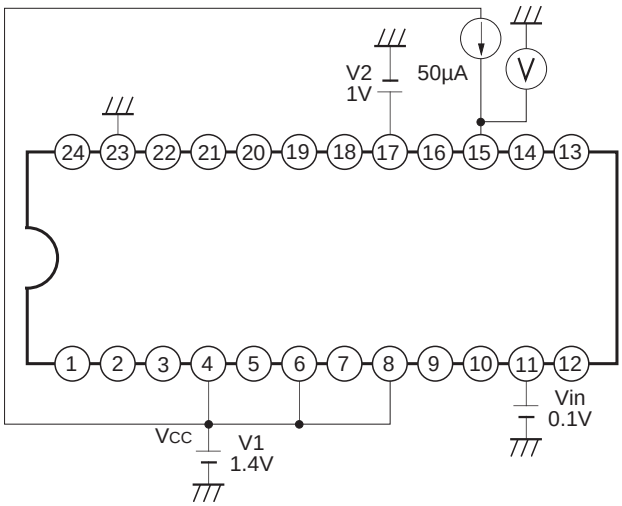
Measurement circuit 6



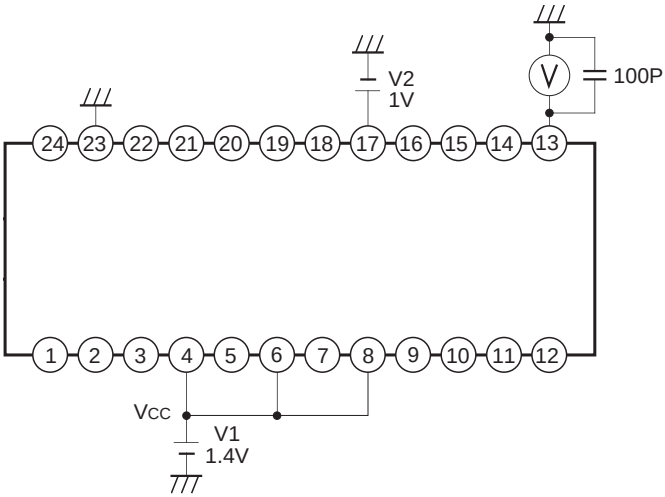
Measurement circuit 7



Measurement circuit 8

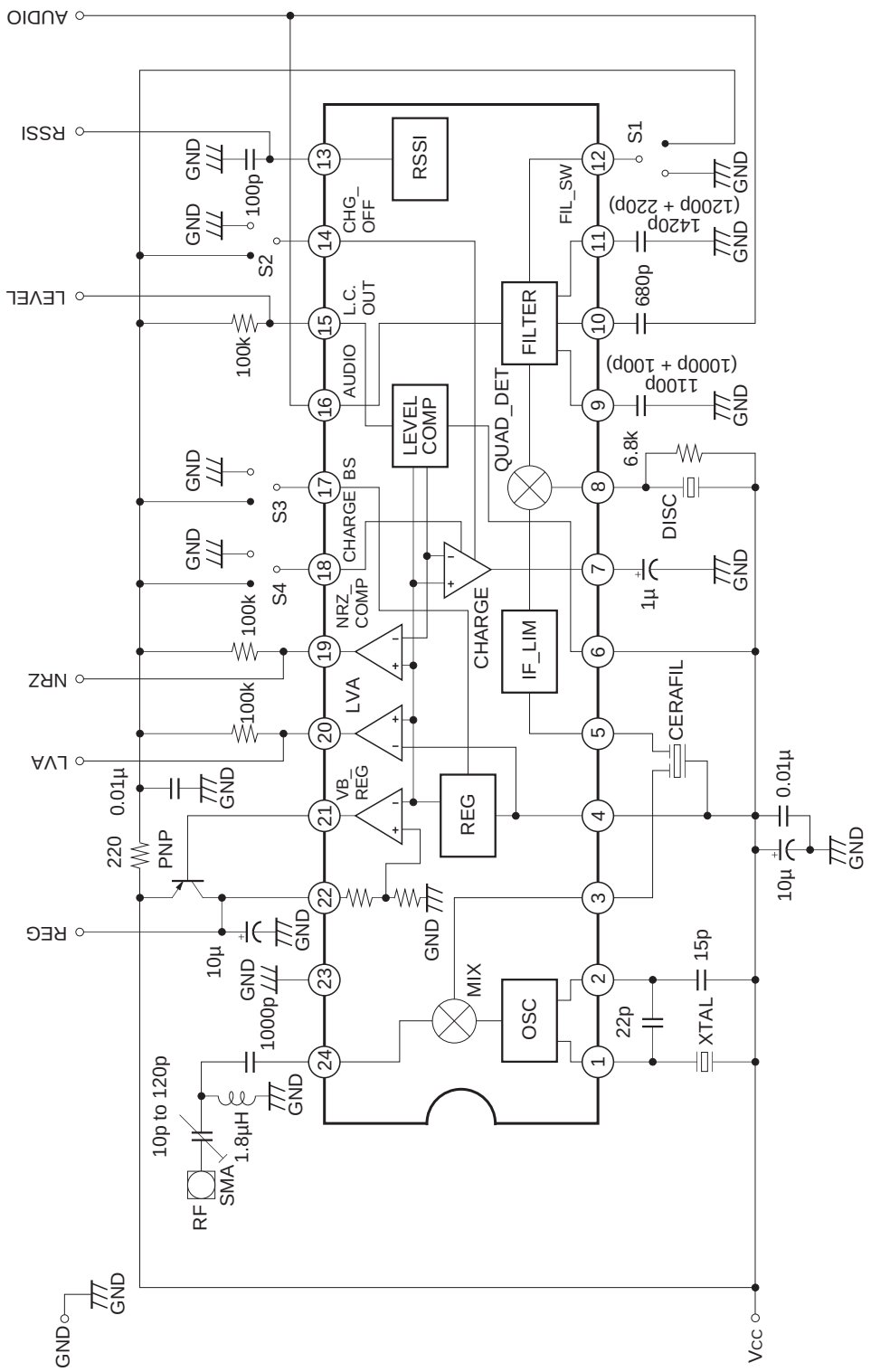


Measurement circuit 9



Measurement circuit 10

Application circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Note

1) Power Supply

The CXA3117N, with the built-in regulator, is designed to permit stable operation at the wide range of supply voltage from 1.1 to 4.0V. Decouple the wiring to VCC (Pin 4) as close to the pin as possible.

2) Oscillator Input

Oscillator input method

a) Using Pins 1 and 2, input self-excited oscillation signal through the composition of a Colpitts type crystal oscillator circuit. Connect the capacitors attached to the crystal and Pin 2 to VCC.

b) Directly input a local oscillation signal to Pin 1.

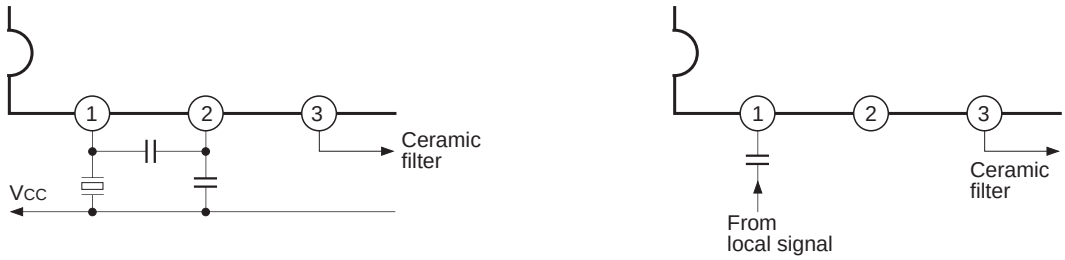


Fig. 1

3) Mixer

The mixer is of double-balance type. Pin 24 is the input pin. Input though a suitable matching circuit. The input impedance is 2.0kΩ.

Pin 3 serves as the output pin for the mixer, and a load resistance of 1.5kΩ is incorporated.

4) IF Filter

The filter to be connected between this mixer output and the IF limiter amplifier input should have the following specifications. Connect the ground pin of the IF filter to VCC.

I/O impedance : 1.5kΩ ±10%

Bandwidth : Changes according to applications.

5) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100dB. Take notice of the following points in making connection to the IF limiter amplifier input pin (Pin 5).

a) Wiring to the IF limiter amplifier input (Pin 5) should be as short as possible.

b) As the IF limiter amplifier output appears at QUAD (Pin 8), wiring to the ceramic discriminator connected to QUAD should be as short as possible to reduce the interference with the mixer output and IF limiter amplifier input.

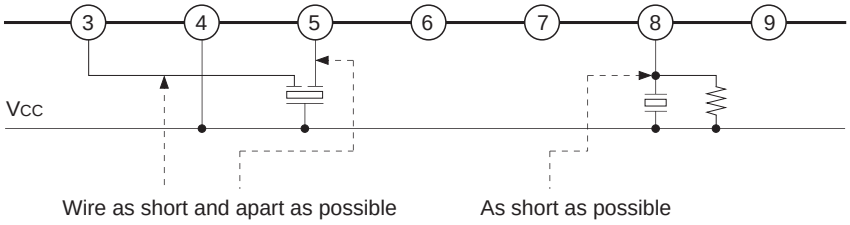


Fig. 2

6) Quick Charge

In order to hasten the rising time from when power is turned on, the CXA3117N features a quick charge circuit. Therefore, the quick charge circuit eliminates the need to insert a capacitor between the detector output and the LPF as is the case with conventional ICs, but a capacitor should be connected to Pin 7 to determine the average signal level during steady-state reception. The capacitance value connected to Pin 7 should be chosen such that the voltage does not vary much due to discharge during battery saving.

Connect a signal for controlling the quick charge circuit to Pin 18. Setting this pin high enables the quick charge mode, and setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time.

Connect Pin 18 to GND when quick charge is not being used.

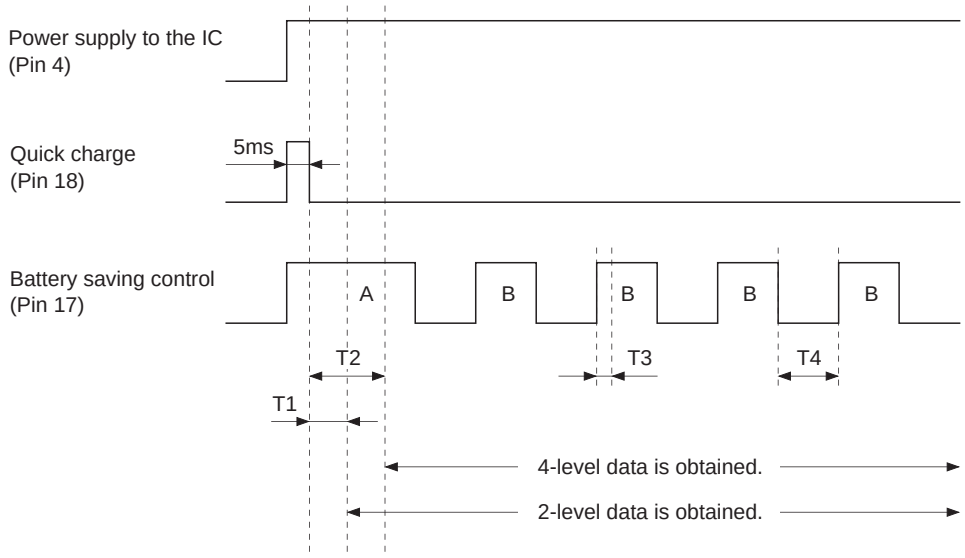


Fig. 3

Example when the Pin 7 REF capacitance value is 1µF

T1 in Fig. 3: 2-level data setting time after quick charge

When the input frequency offset is within ±4.8kHz: 0ms

T2 in Fig. 3: 4-level data setting time after quick charge

When the input frequency offset is within ±1.6kHz or less: 0ms

When the input frequency offset is within ±3kHz or less: 500ms or less

T3 in Fig. 3: 4-level data setting time after battery saving: 2ms or less

T4 in Fig. 3: S curve correction voltage hold time: 5min. or more

7) Detector

The detector is of quadrature type. To perform phase shift, connect a ceramic discriminator to Pin 8.
The phase shifting capacitor for the quadrature detector is incorporated. The FM (FSK) signal demodulated with the detector is output to AUDIO (Pin 16) through the internal primary LPF.
The AUDIO output is the anti-phase output to the NRZ OUT.

The CDBM455C50 (MURATA MFG. CO., LTD.) ceramic discriminator is recommended for the CXA3117N.
For the 2-level system, the CDBM455C28 can also be used.

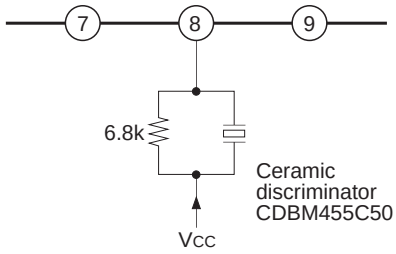


Fig. 4

The detector output level is changed according to the resistance value connected to Pin 8.

8) Filter Buffer, Level Comparator and NRZ Comparator

The LPF circuit is built in this IC.
The LPF output is connected internally to the NRZ comparator, level comparator and quick charge circuit.

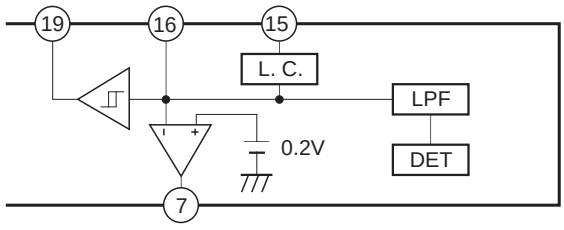


Fig. 5

Using the LPF, remove noise from the demodulated signal and input the signal to the above three circuits.

8)-1. LPF Constant

The data filter cut-off (fc) is expressed with the following equation.

$$fc_1 = \frac{1}{2\pi C_9 R}$$

$$fc_2 = \frac{1}{2\pi}\sqrt{\frac{1}{C_{10}\,C_{11}\,R^2}}\ ,\ Q = \sqrt{\frac{C_{10}}{C_{11}}}$$

C_9 to C_{11}: External capacitance (Pin 9 to Pin 11)
R: IC internal resistance

R is approximately 55kΩ ± 20% when Pin 12 is low. The table below shows the example of constants to data rate.

		Capacitance (pF)	fc (Hz)	Data rate
Pin 12 filter switch	H	6800	—	—
	L		430	512bps (2 levels)
	H	1500	950	1200bps (2 levels)
	L		1900	2400bps (2 levels)
	H	Pin 9 1100 Pin 10 680 Pin 11 1420	1000	1600bps (2 levels)
	L		2000	3200bps (2 levels)
	H	Pin 9 1100 Pin 10 680 Pin 11 1420	1000	3200bps (4 levels)
	L		2000	6400bps (4 levels)

8)-2. Comparator Output

The level comparator and the NRZ comparator shape the waveform of this input signal and output it as a square wave. The comparator output stage is for open collector.

Thus, if the CPU is of CMOS type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

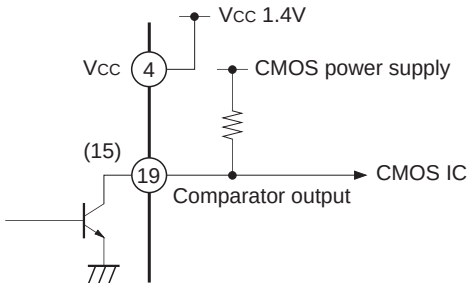
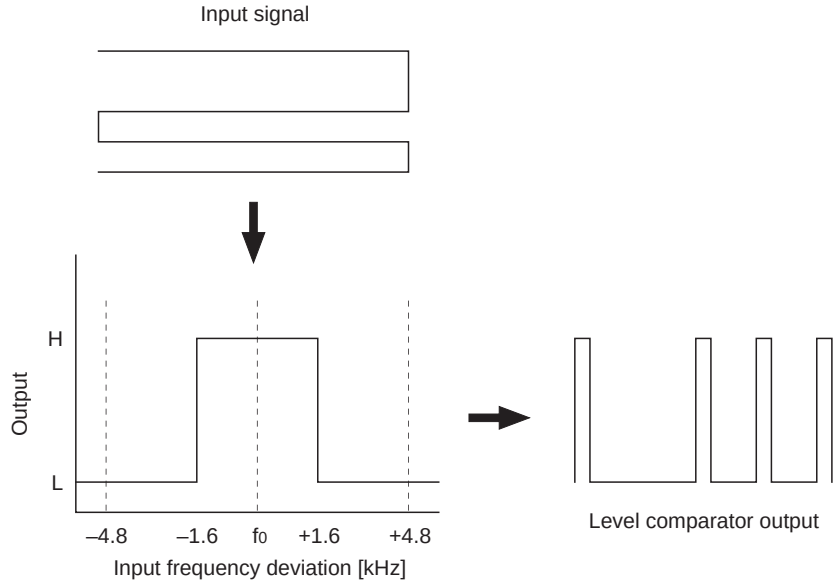


Fig. 6

8)-3. Level Comparator Output

The level comparator characteristics are as shown in the figure below. Therefore, a high signal is output at the bit border even if the input signal is a ±4.8kHz signal. This high output interval varies according to the frequency response of the bit rate filter, and widens as the cut-off frequency becomes lower. The decoder avoids this high interval when processing data.



9) REG CONT

Controls the base bias of the external transistors.

10) LVA OUT

This pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device. The setting voltage of the LVA is 1.05V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 50mV (typ.).

11) B.S.

Operation of the CXA3117N can be halted by setting this pin low. This pin can be connected directly to CMOS device. The current consumption during battery saving is 20µA or less (at 1.4V).

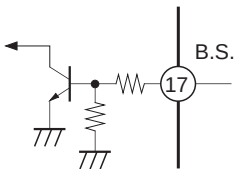


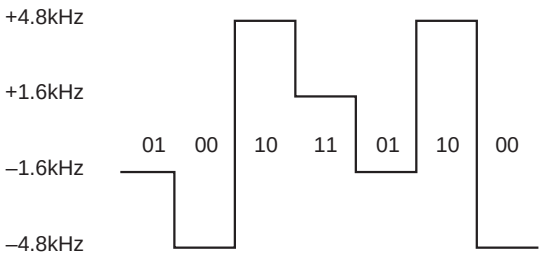
Fig. 7

12) M-ary (M = 2- or 4-level) FSK Demodulation System

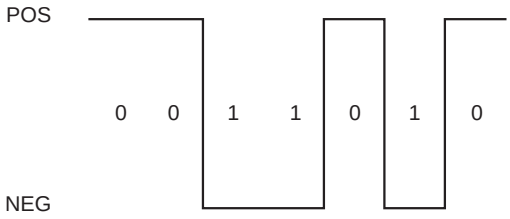
12)-1. Output Waveform

Polarity discrimination output and MSB comparator output are used to demodulate the 4-level waveform shown below.

[4-level FSK demodulating waveform]

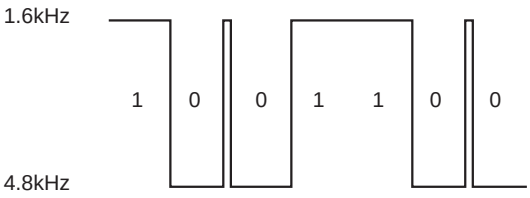


[NRZ OUT] Polarity discrimination output (When the input frequency is higher than the local frequency)



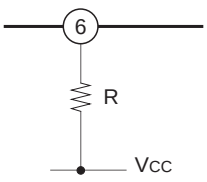
(The polarity can be inverted by setting the local frequency higer than the input frequency.)

[L.C. OUT] MSB comparator output



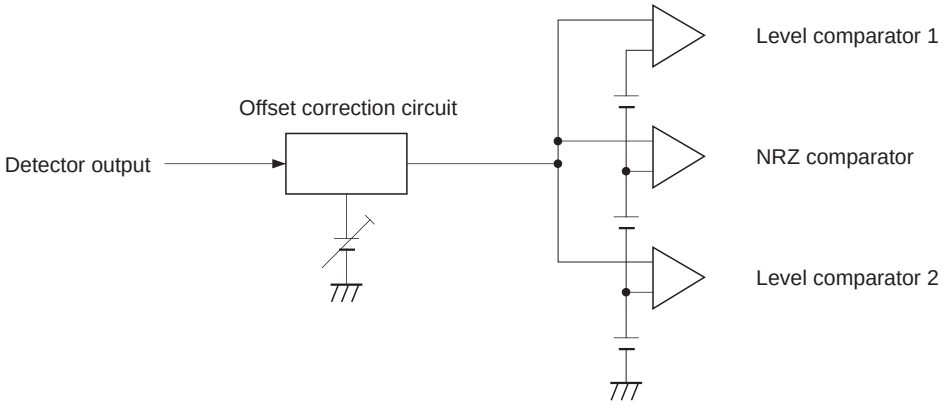
The 4-level FSK demodulating data is divided into an NRZ OUT and L.C. OUT shown above. Here, the NRZ OUT corresponds to a conventional NRZ comparator output. The L.C. OUT is made comparing the demodulated waveform amplitude to the IC internal reference voltage levels. When the threshold value of L.C. OUT is not appropriate to the detector output, the resistance value on Pin 8 should be varied for the detector output level adjustment or the resistor should be inserted between Pin 6 and V_{CC} for the level comparator threshold value adjustment.

For the 2-level FSK demodulation, it corresponds to a conventional NRZ comparator output.



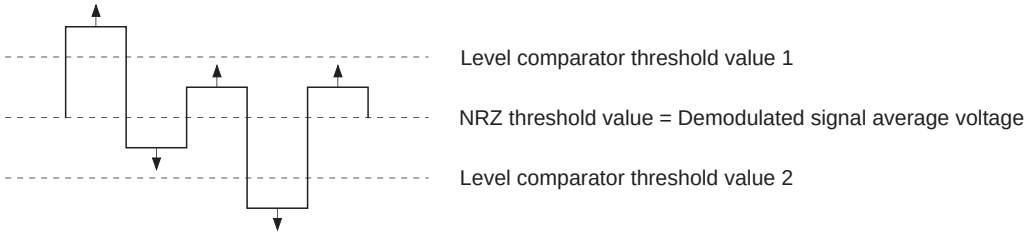
12)-2. 4-level Signal and Threshold Value

For Sony pager ICs, the demodulated signal is optimally matched to the NRZ comparator threshold value by the curve correction operation described in 13) as shown in the figure below. (operation point correction using a feedback loop filter)



Operation point correction (The comparator threshold value is fixed.)

The level comparator threshold value can be adjusted by varying the detector output level, which is achieved by varying the discriminator dumping resistance. (AC gain adjustment)



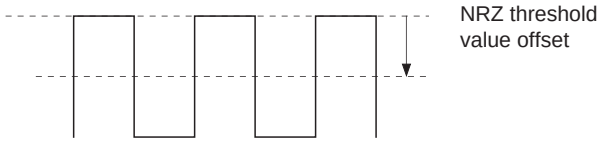
AC gain adjustment

12)-3. Offset Amount and Threshold Value

Immediately after power-on when the REF capacitor is not charged with the correction voltage, if the input frequency has an offset, some time is required to correct this offset. In addition, the times required to obtain 2-level and 4-level data differ according to the offset amount.

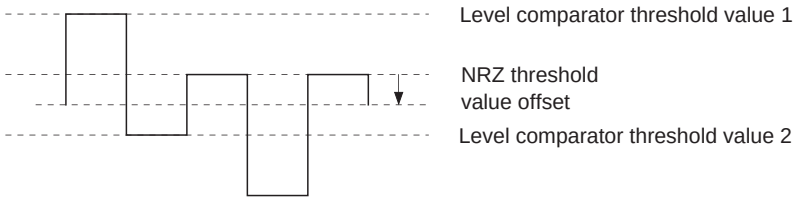
a) 2-level signals

In the case of 2-level signals, correct data is obtained when the offset amount is smaller than the detector output amplitude. This is 75mV or less when the detector output level is 150mVp-p which corresponds to within ±4.8kHz when converted to a frequency by the S curve. Thus, 2-level data is obtained without an operation point correction time lag when the frequency offset is within ±4.8kHz.



b) 4-level signals

In the case of 4-level signals, correct data is obtained when the offset amount is less than 1/3 of the detector output amplitude (during ±4.8kHz DEV). This is 25mV or less when the detector output level is 150mVp-p which corresponds to ±1.6kHz or less when converted to a frequency by the S curve, . Thus, 4-level data is obtained without an operation point correction time lag when the frequency offset is within ±1.6kHz.



As shown above, 4-level signals have an allowable offset range 1/3 that of 2-level signals. When the offset exceeds this allowable range, time is required to determine the operation point and obtain correct data through feedback. Also, even if the offset is within the allowable range, the output pulse duty changes until the offset is 0.

13) Principle of Quick Charge Operation

BUF in Fig. 8 is the detector buffer amplifier and COMP is the level comparator or the NRZ comparator.

The CXA3117N has a feedback loop from the comparator input to the input circuit of the detector output buffer. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set in the feedback loop. Switching the current of the quick charge circuit enables reduction of the rise time.

In this block, CHG is a comparator which compares input voltages and outputs a current based on this comparison. The current on CHG is switched between high and low at Pin 18. When the power is turned on, switch the current to high to increase the charge current at C in Fig. 8 and shorten the time constant. For the short time constant, the FSK REF voltage is charged so that it becomes equal to the reference voltage. During steady-state reception mode, switch the current to low, lengthening the charge time constant and allowing for stable data retrieval. Also, controlling Pin 14 can make the current off. This is effective when the same data are received continuously.

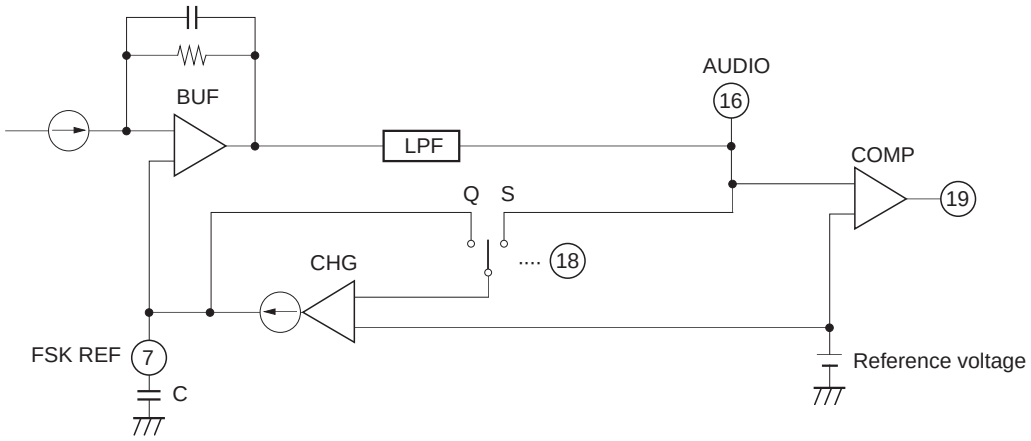


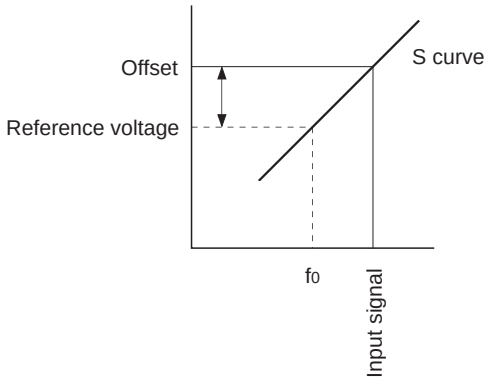
Fig. 8

13)-1. Slow Charge Mode

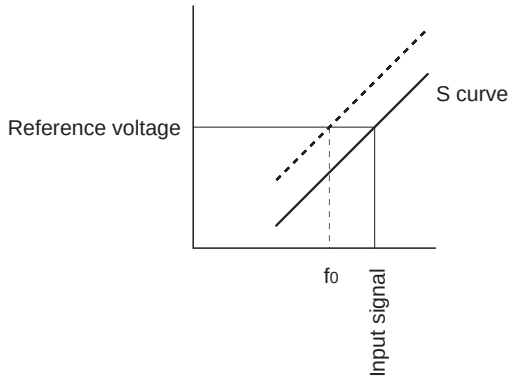
During slow charge mode, if the RF system frequency is deviated, etc., and the demodulated output has an offset voltage, feedback is applied to correct this offset voltage. Here, feedback is applied so that the average value of the audio output voltage matches the internal regulator voltage. This feedback shifts the S curve up and down in a parallel manner.

13)-2. Quick Charge Mode

During quick charge mode, feedback does not operate on the offset voltage of the demodulated output and a non-corrected S curve determined by the IC and discriminator is set.



When the RF system frequency is deviated, there is no correction so an offset occurs.



During slow charge mode, the S curve shifts to correct the offset.

14) S Curve Characteristics

Even if the IF IN input signal frequency is deviated, the feedback is applied to the AUDIO operating point so as to match it to the comparator reference voltage by the quick charge operation shown in Fig. 8. Therefore, this feedback must be halted in order to evaluate the S curve characteristics.

To execute the evaluation, measure the average voltage on Pin 16 first and input this voltage to Pin 7 from the external power supply.

15) Control Pins

The function controls are as shown below.

Pin No.	12	14	17	18
Symbal	FIL SW	CHG OFF	B.S.	CHARGE
Function	Data filter cut-off control	Pin 7 charge current control	Battery saving mode control	Pin 7 charge speed control
Input high	fc: Low	Slow charge off	IC operation*	Quick charge
Input low	fc: High*	Slow charge operation*	Sleep	Slow charge*

Note) Pin 14 control should be performed with Pin 18 low.

When each function is not controlled externally, set it to the state with an asterisk (*).

16) Misoperation Prevention Function for Continuous Data

The offset to the comparator threshold value of the detector output is canceled with the feedback loop indicated in the paragraph 13). This operation assumes that “0” and “1” are in equal numbers in the data. The offset is occurred when the “0” or “1” data are received continuously. In this case, setting Pin 14 high to make the charge current off prevents the offset occurrence.

Without using this function, the stability for the same data continuously received depends on the capacitance value on Pin 7 shown in the paragraph 13). When this capacitance value is increased, the data is demodulated more stably; however, it takes more time for the IC to rise. If this function is not used, be sure to connect Pin 14 to GND.

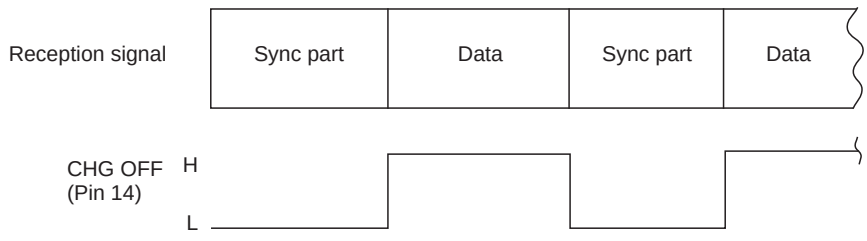


Fig. 9

17) REF Capacitance Value and Charge Time, Hold Time

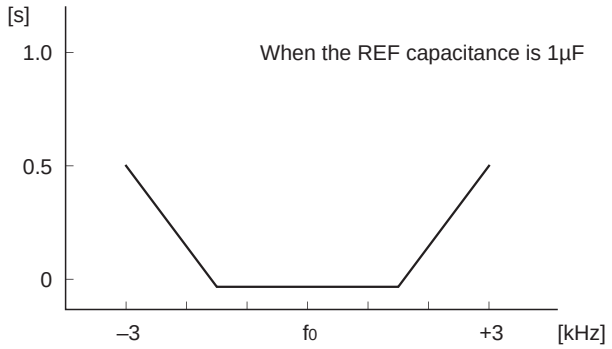
The REF capacitance is the feedback loop time constant of the S curve. This determines the detector output low frequency cut-off, IC rise characteristics and operating voltage hold characteristics during battery saving.

When the REF capacitance is reduced:

1. The detector output low frequency cut-off becomes higher.
2. The IC rise characteristics become faster.
3. The operating voltage hold characteristics during battery saving become shorter.

Of these, 1 has little effect on FSK, so a capacitance value that matches the used system should be selected in consideration of 2 and 3.

17)-1. Example of IC Rise Characteristics Immediately After Power-on



Offset frequency and T2 (after power-on until 4-level data is obtained)

17)-2. Example of Operating Voltage Hold Characteristics

When the REF capacitance is 1µF, the S curve hold voltage variation is a value that has no effect on the rise of the 4-level data after 5 minutes of battery saving as shown below.

Offset voltage after 5 minutes of battery saving: 10mV or less

18) Sensitivity Adjustment Method

The constants shown in the Application Circuit diagram are for the standard external parts. However, adjustment may be necessary depending on the conditions of use, characteristics of external parts, and the RF system circuit and decoder connected to the IF IC, etc. Adjust the sensitivity according to the following procedures.

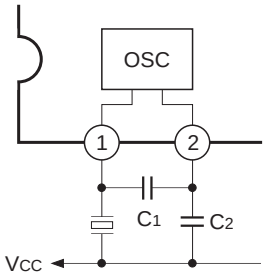
a) MIX IN matching

When using a matching circuit between the RF system circuit and MIX IN of the CXA3117N, adjust the trimmer to obtain the optimal sensitivity while monitoring the AUDIO output.

b) Local input level

The mixer circuit gain is dependent on the local signal input level to OSC IN. The input level to OSC IN should be set as high as possible within the range of –6 to +2dBm as shown in the graph of "Local input level vs. Mixer gain characteristics". However, care should be taken as raising the input level above +2dBm will cause the sensitivity to drop.

When creating the local signal using the internal oscillator circuit, the oscillation level varies according to the external capacitances attached to Pins 1 and 2 and the characteristics of the used crystal. Therefore, be sure to adjust the external capacitance values attached to Pins 1 and 2 according to the crystal characteristics.



C_1 and C_2 have the following range in the figure above.

$C_1 \geq C_2$

$C_1 = C_2$ to $C_1 = 5C_2$

As for the ratio of C_1 to C_2, the oscillation stabilizes as C_1 approaches equality with C_2.

The oscillation level decreases as the C_1 and C_2 values become larger, and increases as the C_1 and C_2 values become smaller.

Use a FET probe to confirm the local input level.

c) LPF constant

The data filter cut-off may need to be changed depending on the characteristics of the connected decoder. Adjust the capacitance values of Pins 9 to 12 while checking the incoming sensitivity including the decoder.

If the capacitance values are too large, the detector output waveform will deviate at high data rates, causing the sensitivity to drop. Conversely, if the capacitance values are too small, the LPF will be easily affected by noise, causing the sensitivity to drop.

Adjust capacitance values of Pins 9 to 12 so that the capacitance value described in "16) LPF Constant" becomes smaller.

d) Detector output level

The NRZ comparator and level comparator threshold values are fixed for the CXA3117N. In the case of 4-level signals, the relationship between the level comparator threshold value and the detector output level affects the sensitivity. The detector output level can be adjusted by the resistance attached to Pin 8. Increasing the resistance value also increases the output level, and vice versa.

The Pin 8 resistance value differs according to the ceramic discriminator attached to Pin 8. When the discriminator is changed to a different type, the resistance value must be adjusted.

Adjust the resistance value while monitoring the level comparator output waveform or the sensitivity including the decoder.

e) Quick charge circuit

The CXA3117N has a feedback circuit that corrects the detector output operation point in order to correct the IF frequency deviation. When the IF frequency deviation amount is large, correction takes time and may lower the sensitivity. Adjust the oscillator frequency of the local oscillator so that the center frequency of the signal input to Pin 5 (IF IN) is as close to 455kHz as possible.

19) CXA3117N Standard Board Description

- Outline

  This board contains the external parts shown in the Application Circuit in order to evaluate CXA3117N operation.

- Features

  The following CXA3117N basic operations can be checked.

  1) Varying the data filter cut-off
  2) Battery saving and other mode switching
  3) NRZ output and level comparator output pins

- Method of use

  1) Input the CXA3117N supply voltage Vcc = 1.4V.
     The CXA3117N operates with a single power supply.
  2) The CXA3117N uses a 21.245kHz crystal. Input the RF signal from the RF pin and use the CXA3117N in the condition where IF = 455kHz.
  3) Set the mode switches.

- Mode switch setting

  Mode switches S1, S2, S3 and S4 are provided in four locations in the board. Each basic operation can be confirmed by switching these mode switches while referring to the board layout. See the table in 15) Control Pins for the mode switching.

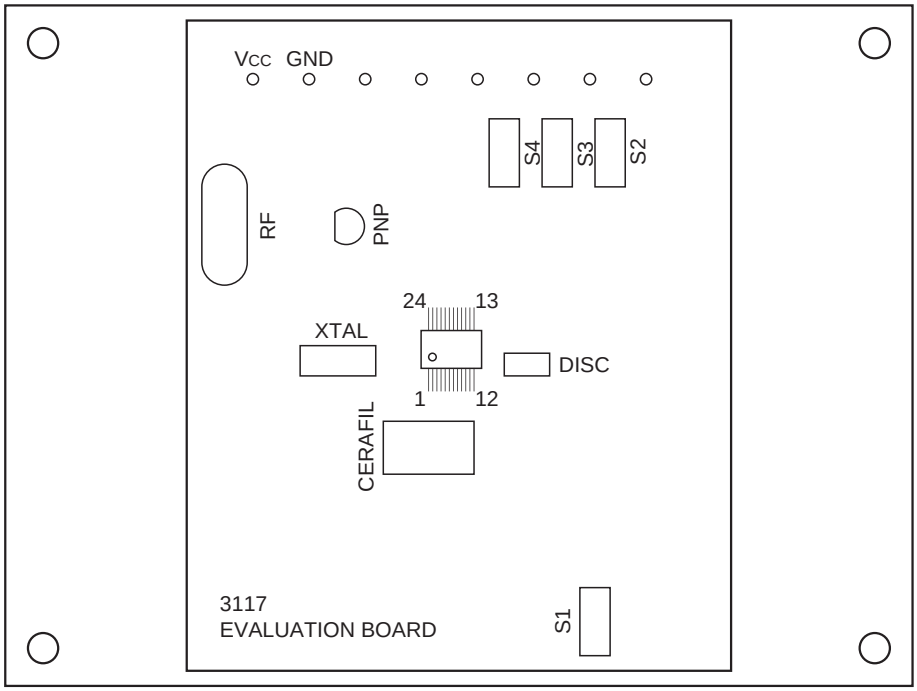
- Device specifications

  See these Specifications for the IC specifications. The ICs for this evaluation board are ES specification.

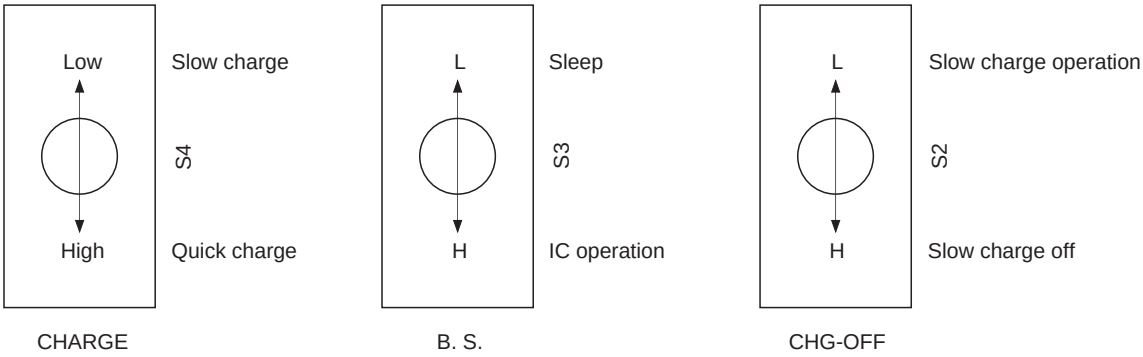
- Circuit diagram

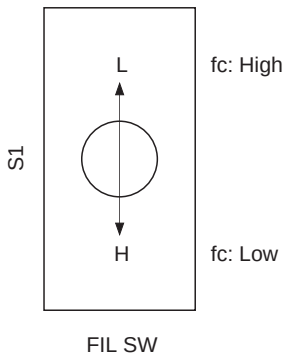
  The circuit diagram is the same as the Application Circuit diagram in these Specifications.

19)-1. Standard Board Layout



19)-2. Mode Switch Description





19)-3. List of Standard Board Parts

VALUE	PART#	REMARKS (MANUFACTURE)	NOTE

Resistor

220	R4	(RIVER)	E12 series 1/8W
8.7k	R7		
100k	R5 R6 R8		

Capacitor

10 to 120p	C1	TZ03P450FR169 (MURATA PRODUCTS)	TRIMMER CAPACITOR
15p	C5	DD100 series temperature characteristics type B (MURATA PRODUCTS)	CERAMIC CAPACITOR E12 series (high dielectric constant type)
22p	C4		
100p	C14		
1000p	C3		
1200p	C11 C12 C13		
0.01µ	C8 C9		
1µ	C10	25V 1µ (SHIN-EI TUSHIN KOGYO CO., LTD.)	ELECTROLYTIC CAPACITOR E6 series
10µ	C6 C7	25V 10µ (SHIN-EI TUSHIN KOGYO CO., LTD.)	

Inductor

1.8µH	L1	EL0405 (TDK Products)	E12 series 2.5mm pitch (Lead Pitch)

Active Component

	PNP	2SA1015 (TOSHIBA CORPORATION)	

Crystal

21.245MHz	XTAL	KSS 2B (KINSEKI, LTD.)	

Ceramic Filter

	CERAFIL	CFWS455D (MURATA PRODUCTS)	455kHz 1.5kΩ

Ceramic Discriminator

	DISC	CDBM455C50 (MURATA PRODUCTS)	455kHz

Switch

	S1, S2, S3, S4	ATE1D-2M3-10 (FUJISOKU CORPORATION)	ON – ON (1 poles)

Connector

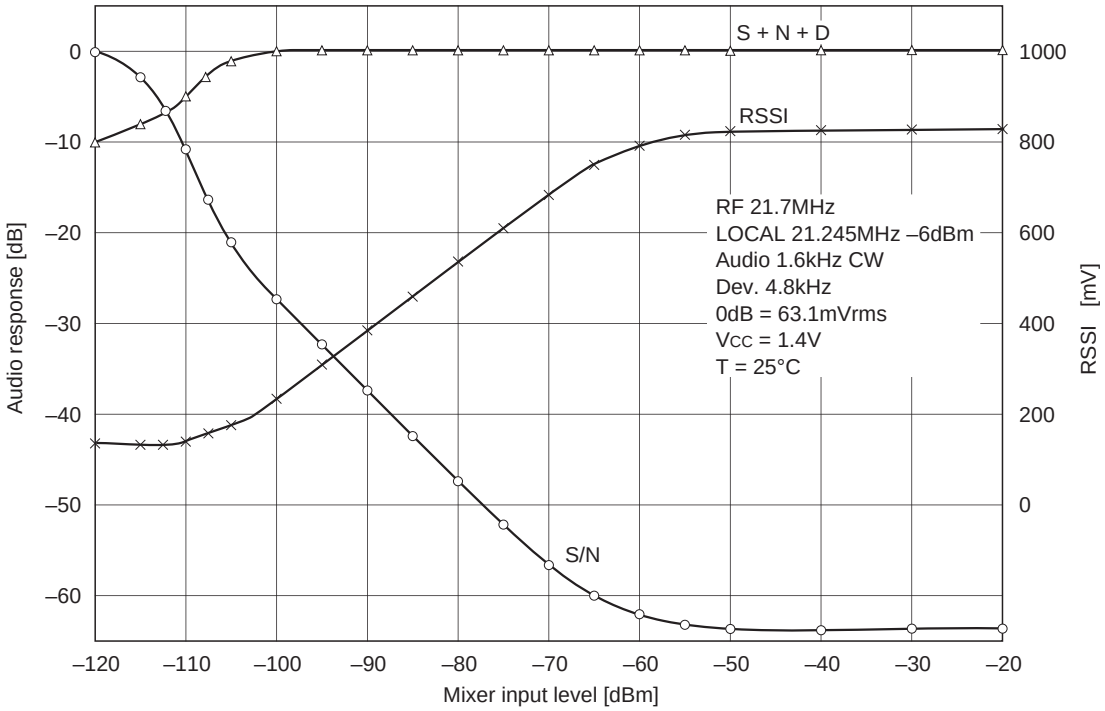
	RF	HRM300-25 (HIROSE ELECTRIC CO., LTD.)	SMA CONNECTOR

Pin

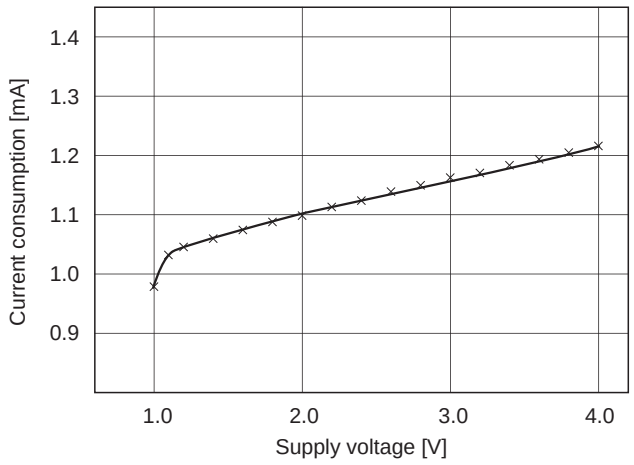
	× 2	Mac 8 test pin ST-1-3 (Mac eight)	L = 10mm 0.8ϕ
	× 6	Mac 8 test pin LC-2-G (Mac eight)	

Example of Representative Characteristics

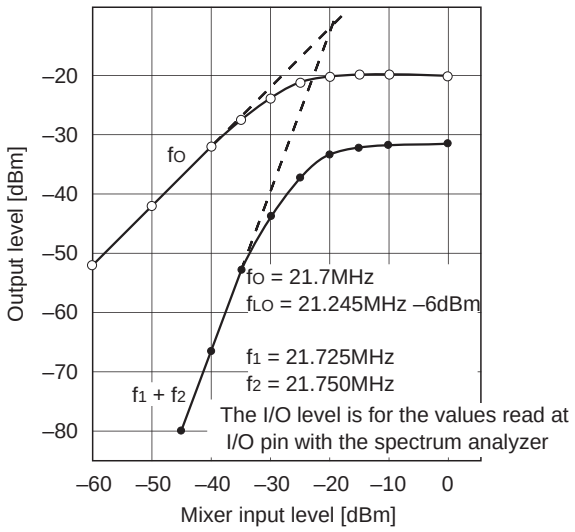
Mixer input audio response and RSSI characteristics



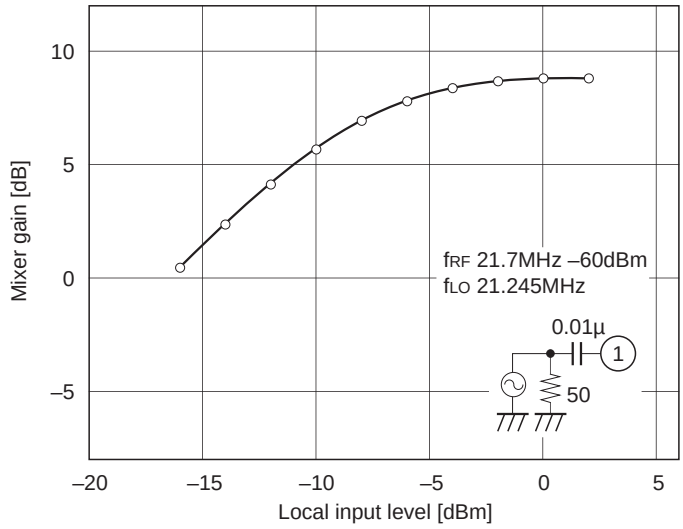
Current consumption characteristics



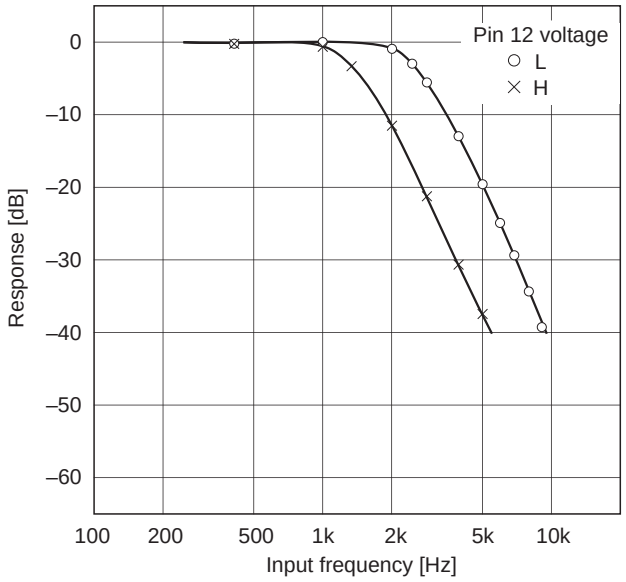
Mixer I/O characteristics and 3rd intercept point



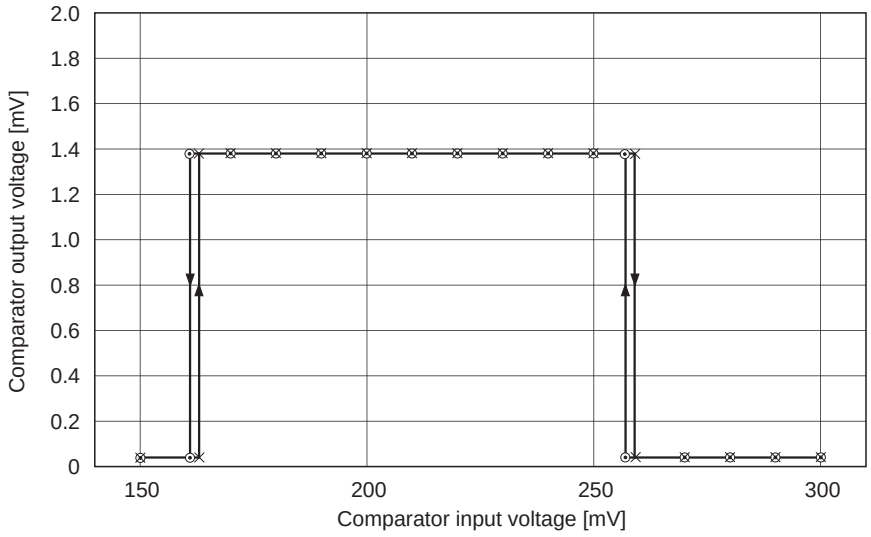
Local input level vs. Mixer gain characteristics



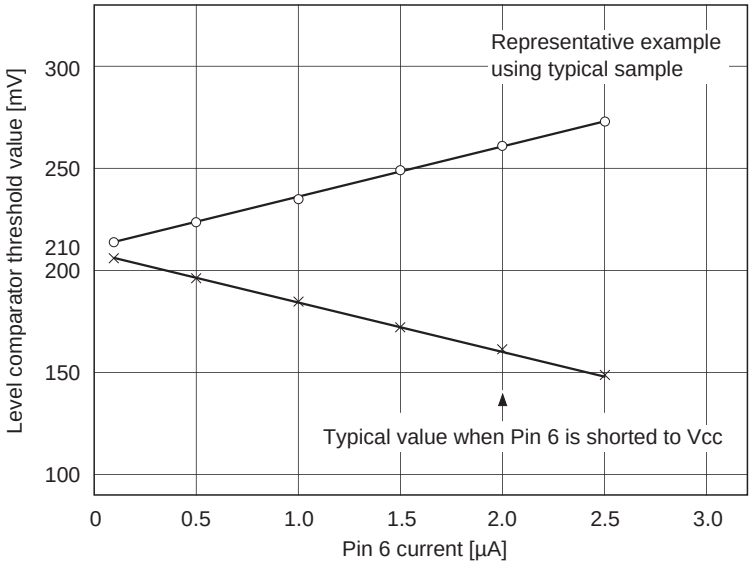
Variable cut-off characteristics of audio filter



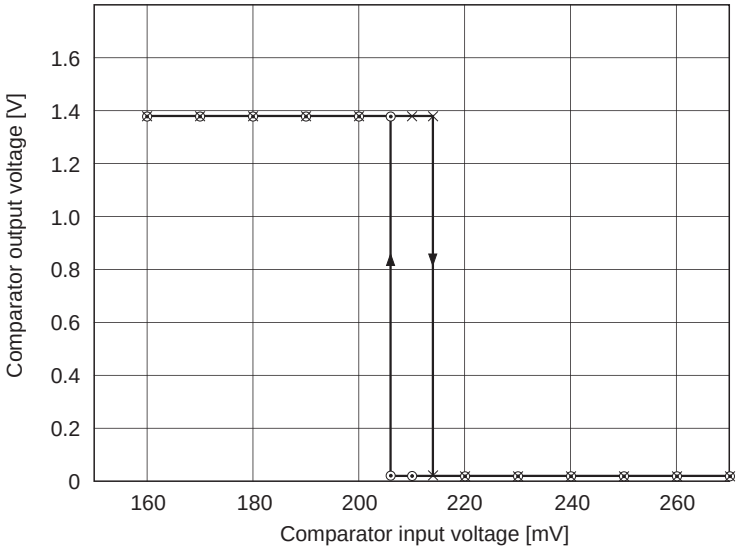
Level comparator characteristics



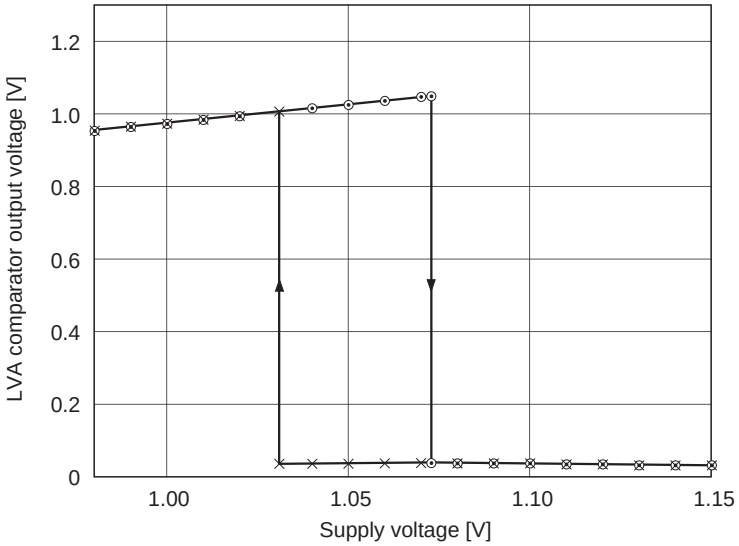
Level comparator threshold value control characteristics (Output low→high switching level)



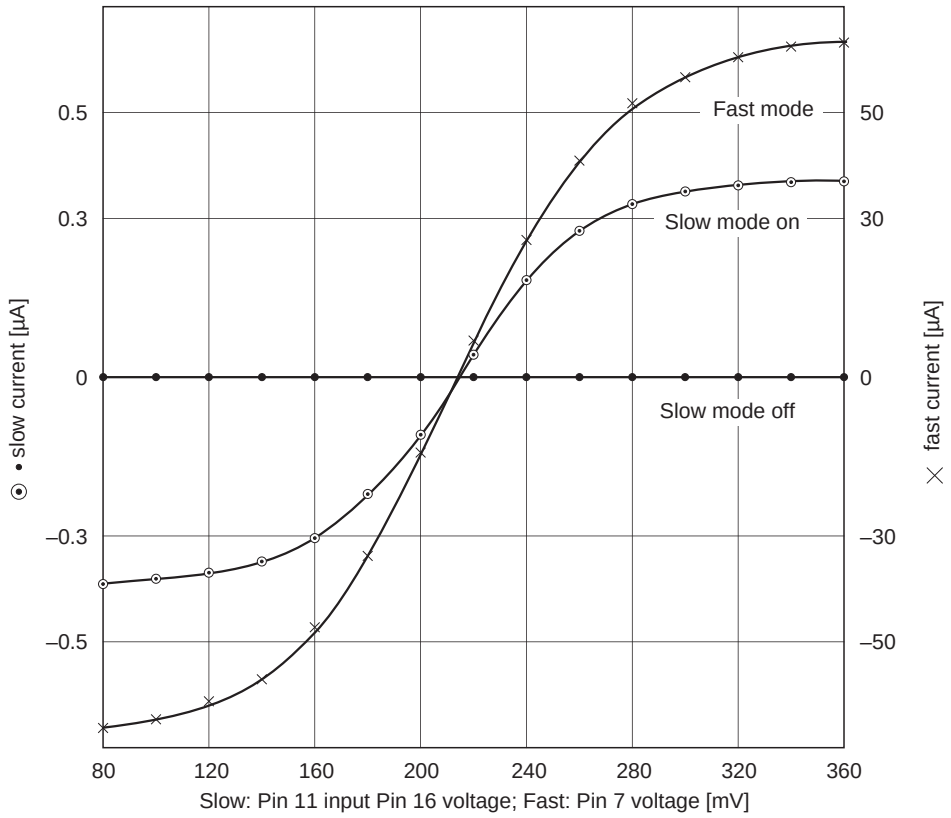
NRZ comparator characteristics



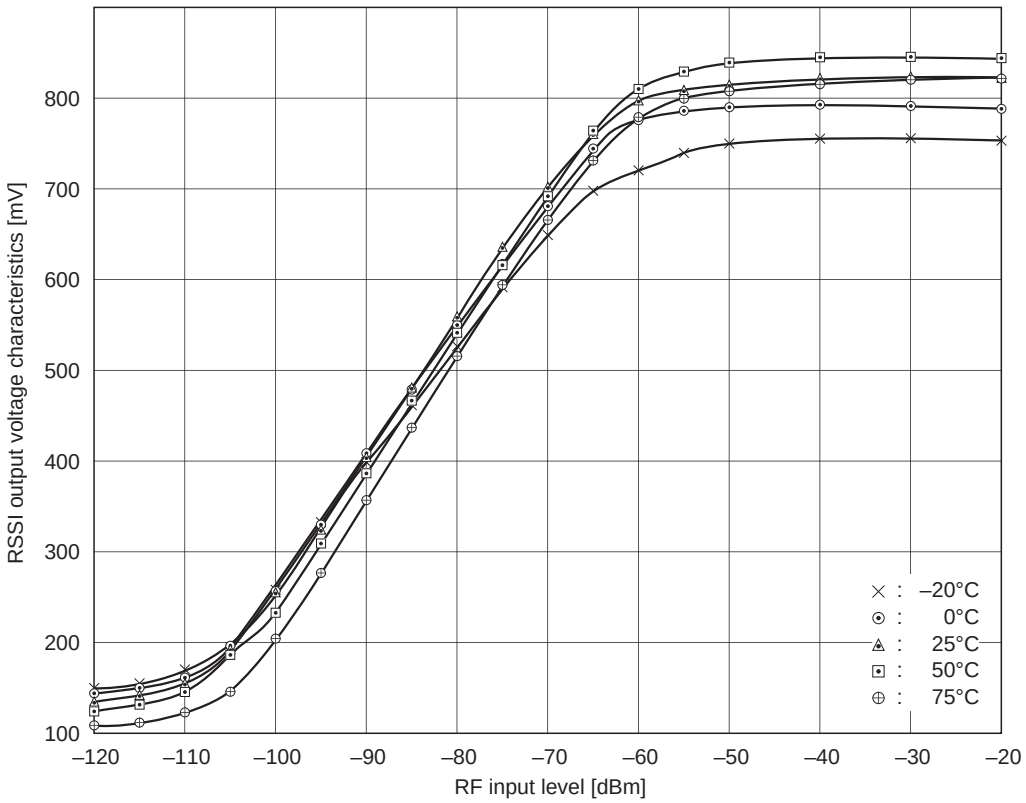
LVA characteristics



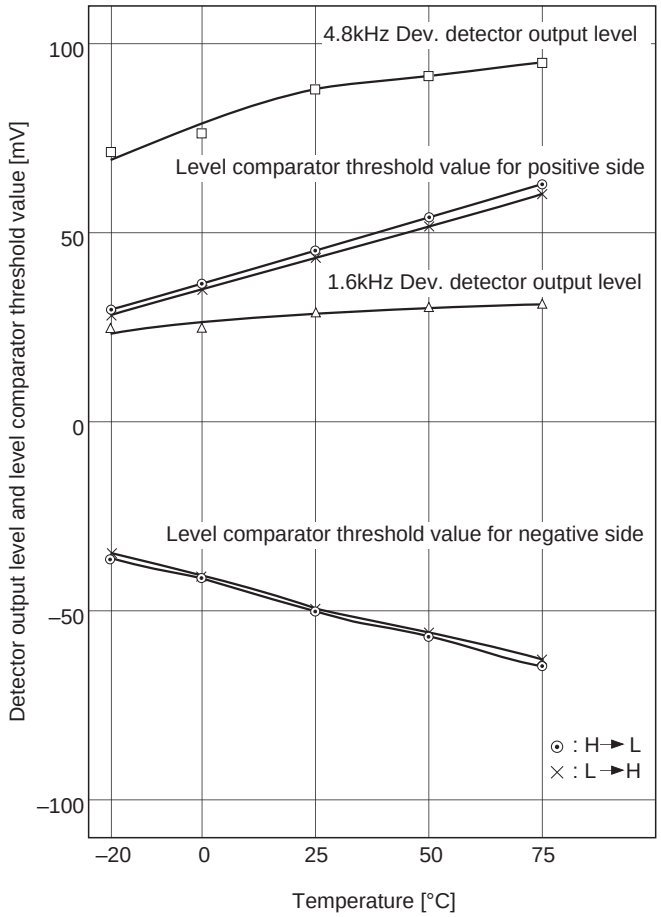
Quick charge circuit output current characteristics



RSSI output voltage temperature characteristics

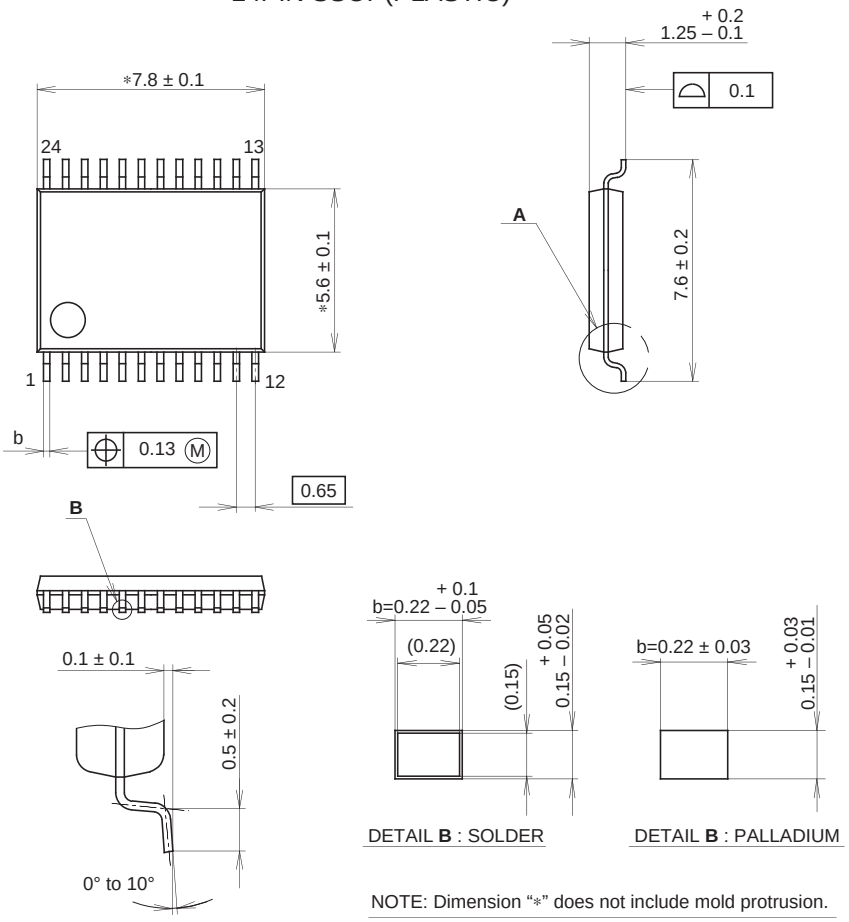


Detector output level and level comparator threshold value vs. Temperature characteristics



Package Outline Unit: mm

24PIN SSOP(PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).