SONY

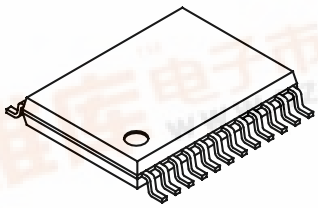
CXA3179N

IF Amplifier for M-ary FSK Pagers (AFC Supported)

Description

The CXA3179N is a low current consumption FM IF amplifier which employs the newest bipolar process. It is suitable for M-ary FSK pagers using AFC.

24 pin SSOP (Plastic)



Features

- Low current consumption : 1.1 mA (typ. at Vcc=1.4 V)
- Low voltage operation : Vcc=1.1 to 4.0 V
- Small package 24-pin SSOP
- Second mixer and oscillator
- Needless of IF decoupling capacitor
- Reference power supply for operational amplifier and comparator
- Bit rate filter with variable cut-off
- AFC current output circuit
- RSSI function
- IF input, Vcc standard
- Maximum input frequency : 30 MHz

Absolute Maximum Ratings

• Supply voltage	Vcc	7.0	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	PD	417	mW

Operating Condition

Supply voltage	Vcc	1.1 to 4.0	V

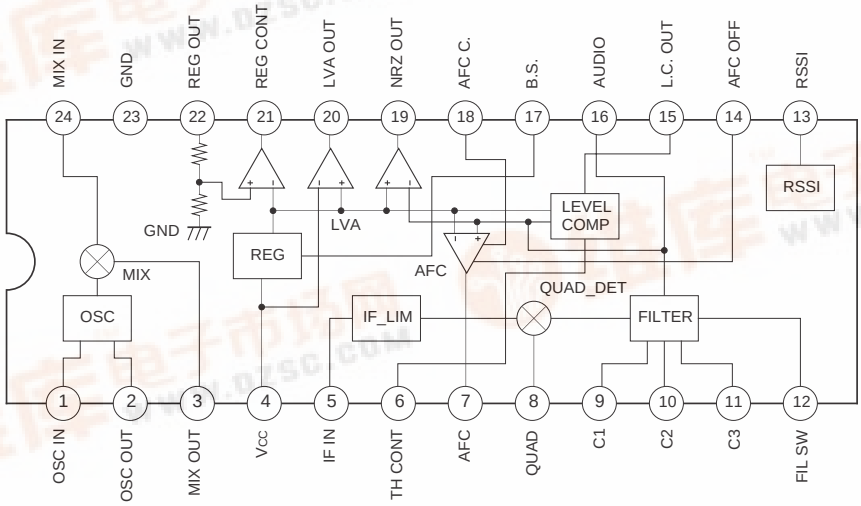
Applications

- M-ary FSK pagers
- Double conversion pagers

Structure

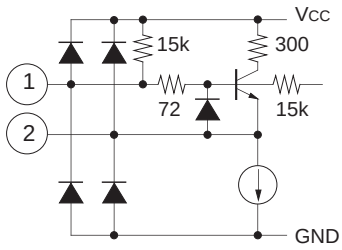
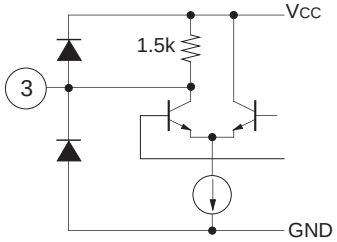
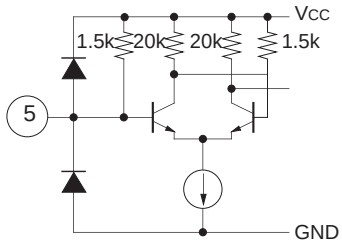
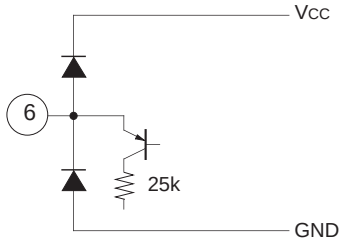
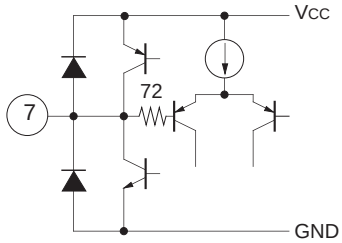
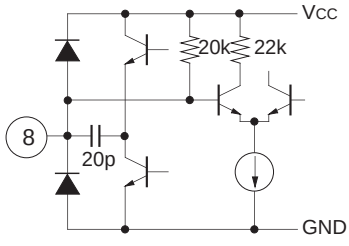
Bipolar silicon monolithic IC

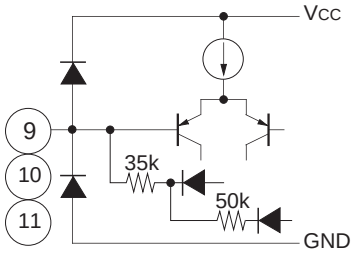
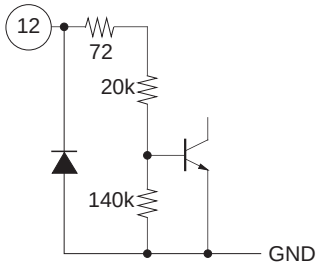
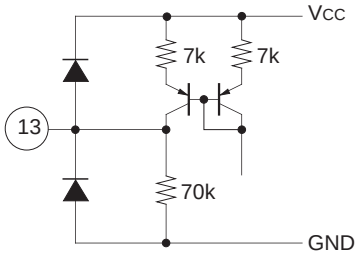
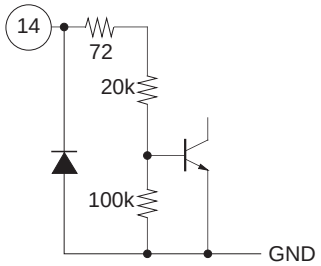
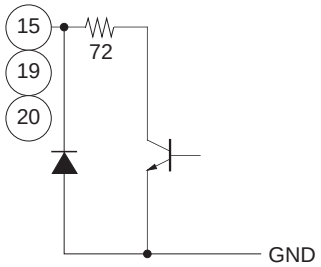
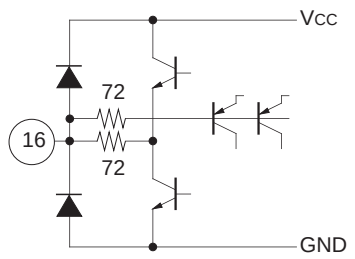
Block Diagram and Pin Configuration

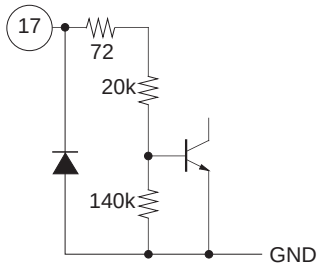
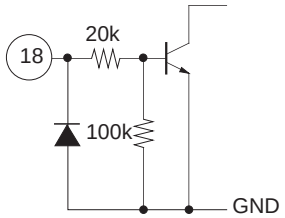
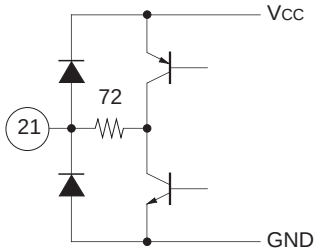
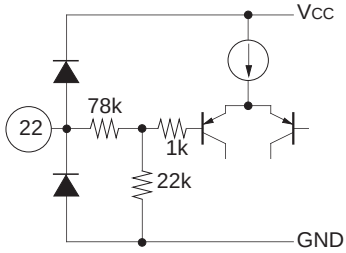
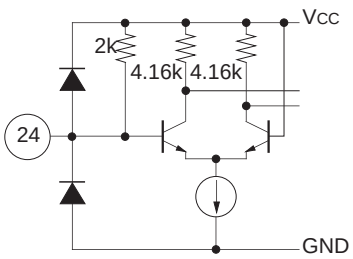


E96Y06A8Z

Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	OSC IN	1.4 V		Connects the external parts of crystal oscillator circuit. A capacitor and crystal oscillator are connected to these pins and Vcc.
2	OSC OUT	0.7 V		
3	MIX OUT	1.3 V		Mixer output. Connect a 455 kHz ceramic filter between this pin and IF IN.
4	Vcc			Power supply.
5	IF IN	1.4 V		IF limiter amplifier input.
6	TH CONT	—		Determines the level comparator threshold value. Threshold value can be adjusted by inserting the resistor between Pin 6 and Vcc. Normally, short to Vcc.
7	AFC	—		AFC current output.
8	QUAD	1.4 V		Connects the phase shifter of FM detector circuit.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9 10 11	C1 C2 C3	0.2 V		Connects the capacitor that determines the LPF cut-off.
12	FIL SW	—		Switches the LPF cut-off. Cut-off is decreased by setting this pin high. (Applied voltage range : –0.5 V to +7.0 V)
13	RSSI	0.1 V		RSSI circuit output.
14	AFC OFF	—		Sets off the AFC circuit current. The AFC current is off by setting Pin 18 low and Pin 14 high.
15 19 20	L.C. OUT NRZ OUT LVA OUT	— — —		Level comparator, NRZ comparator and LVA comparator outputs. They are open collectors. (Applied voltage range : –0.5 V to +7.0 V)
16	AUDIO	0.2 V		Level comparator and NRZ comparator inputs. The filter circuit output is connected.

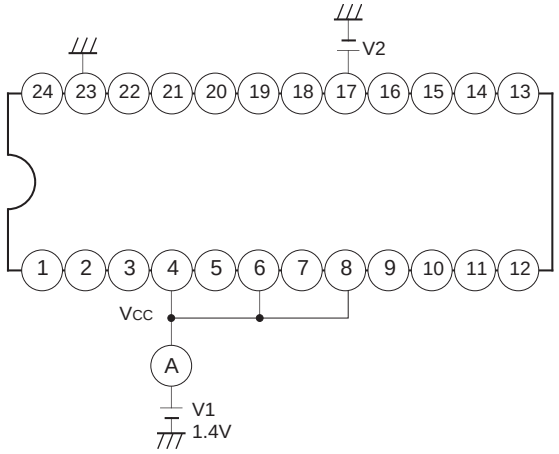
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
17	B.S.	—		Controls the battery saving. Setting this pin low suspends the operation of IC. (Applied voltage range : –0.5 V to +7.0 V)
18	AFC C.	—		Controls the time constant of the AFC circuit. Set this pin high to make the short time constant. (Applied voltage range : –0.5 V to +7.0 V)
21	REG CONT	—		Output for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity : 100 µA)
22	REG OUT	1.0 V		Constant-voltage source output. Controlled to maintain 1.0 V.
23	GND	—		Ground
24	MIX IN	1.4 V		Mixer input.

Electrical Characteristics

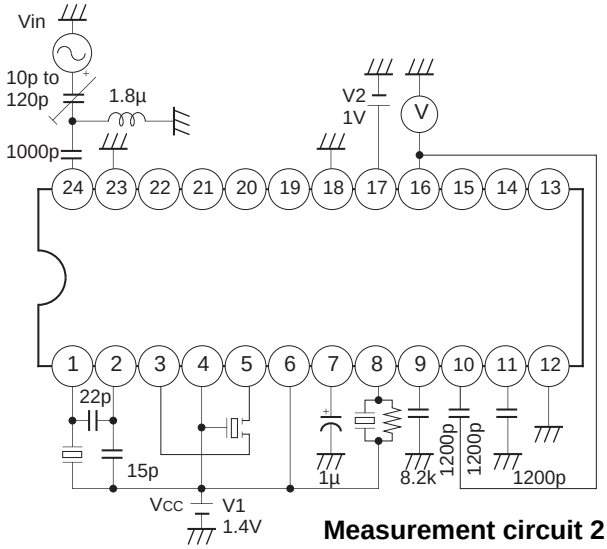
(V_{CC}=1.4 V, Ta=25 °C, F_S=21.7 MHz, F_{MOD}=1.6 kHz, F_{DEV}=4.8 kHz, AM_{MOD}=30 %)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	Measurement circuit 1, V2=1.0 V	0.7	1.1	1.35	mA
Current consumption	I_{CCS}	Measurement circuit 1, V2=0 V	—	6	10	µA
AM rejection ratio	AMRR	Measurement circuit 2, 30 k LPF	25	—	—	dB
NRZ output saturation voltage	V_{SATNRZ}	Measurement circuit 4, Vin=0.3 V	—	—	0.4	V
NRZ output leak current	I_{LNRZ}	Measurement circuit 3, Vin=0.1 V	—	—	5.0	µA
NRZ hysteresis width	V_{TWNRZ}	Measurement circuit 3, Vin=0.1 to 0.3 V	0	10	20	mV
VB output current	I_{OUT}	Measurement circuit 5	100	—	—	µA
VB output saturation voltage	V_{SATVB}	Measurement circuit 5	—	—	0.4	V
REG OUT voltage	V_{REG}	Output current 0 µA	0.95	1.00	1.05	V
LVA operating voltage	V_{LVA}	Measurement circuit 6, V1=1.4 to 1.0 V	1.00	1.05	1.10	V
LVA output leak current	I_{LLVA}	Measurement circuit 6, V1=1.0 V	—	—	2.0	µA
LVA output saturation voltage	V_{SATLVA}	Measurement circuit 7	—	—	0.4	V
Detector output voltage	V_{ODET}	Measurement circuit 2	50	63	80	mVrms
Logic input voltage high level	V_{THBSV}	—	0.9	—	—	V
Logic input voltage low level	V_{TLBSV}	—	—	—	0.35	V
Limiting sensitivity	$V_{IN\ (LIM)}$	Measurement circuit 2, Data filter fc=2.4 kHz	—	–108	—	dBm
Detector output level ratio deviation to level comparator window width	V_{LCWR}	When Pin 6 is shorted to V_{CC}	–15	0	+15	%
Level comparator output saturation voltage	V_{SATLC}	Measurement circuit 9	—	—	0.4	V
Level comparator output leak current	I_{LLC}	Measurement circuit 8	—	—	2.0	µA
RSSI output offset	V_{ORSSI}	Measurement circuit 10	—	150	300	mV
Mixer input resistance	R_{INLIM}	—	1.6	2.0	2.4	kΩ
Mixer output resistance	R_{OUTMIX}	—	1.2	1.5	1.8	kΩ
IF limiter input resistance	R_{INLIM}	—	1.2	1.5	1.8	kΩ

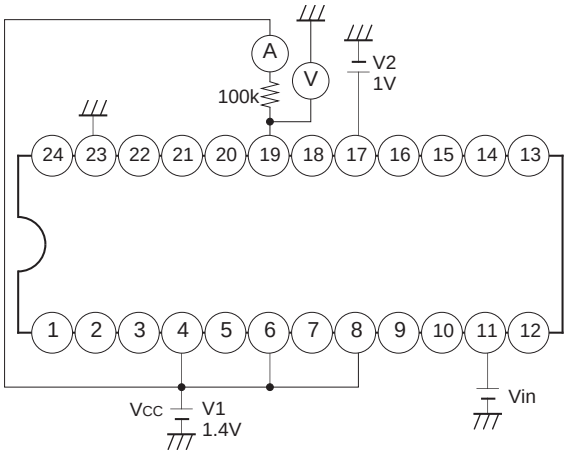
Electrical Characteristics Measurement Circuit



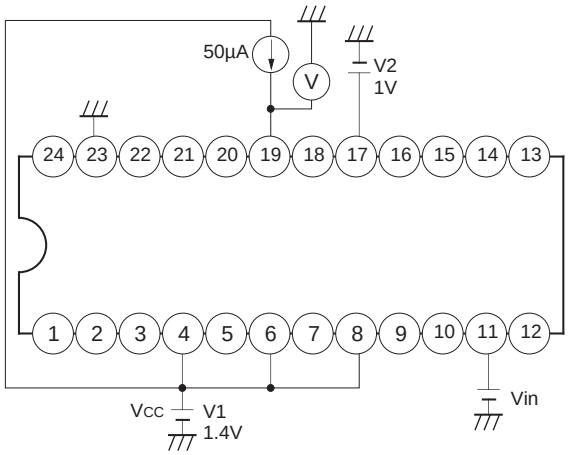
Measurement circuit 1



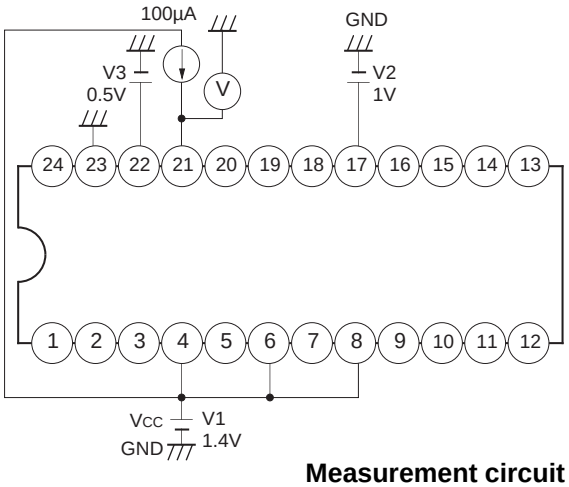
Measurement circuit 2



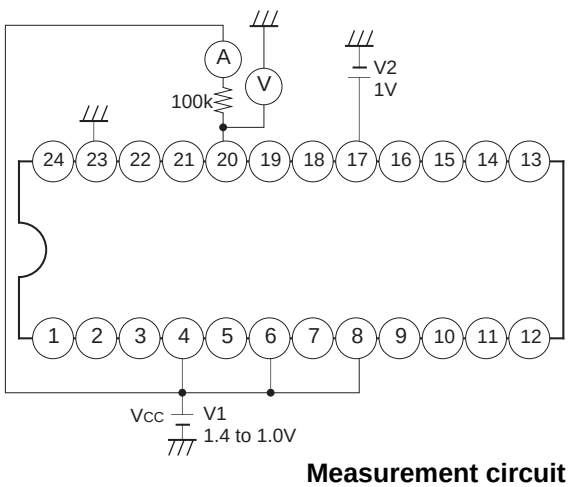
Measurement circuit 3



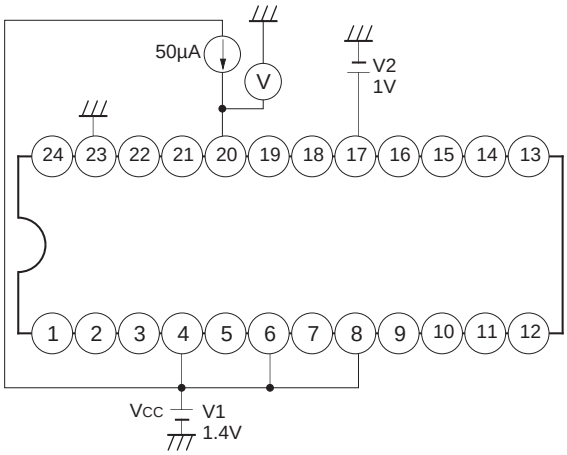
Measurement circuit 4



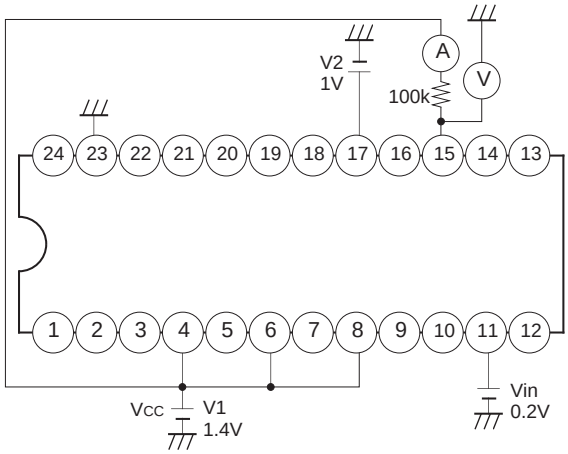
Measurement circuit 5



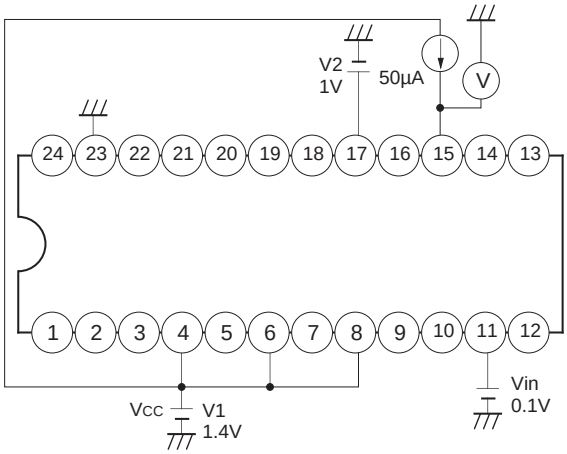
Measurement circuit 6



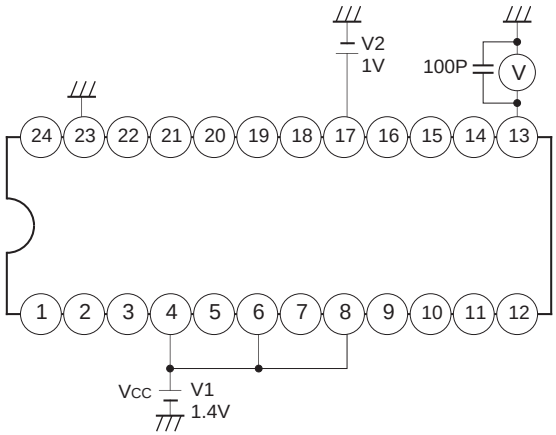
Measurement circuit 7



Measurement circuit 8

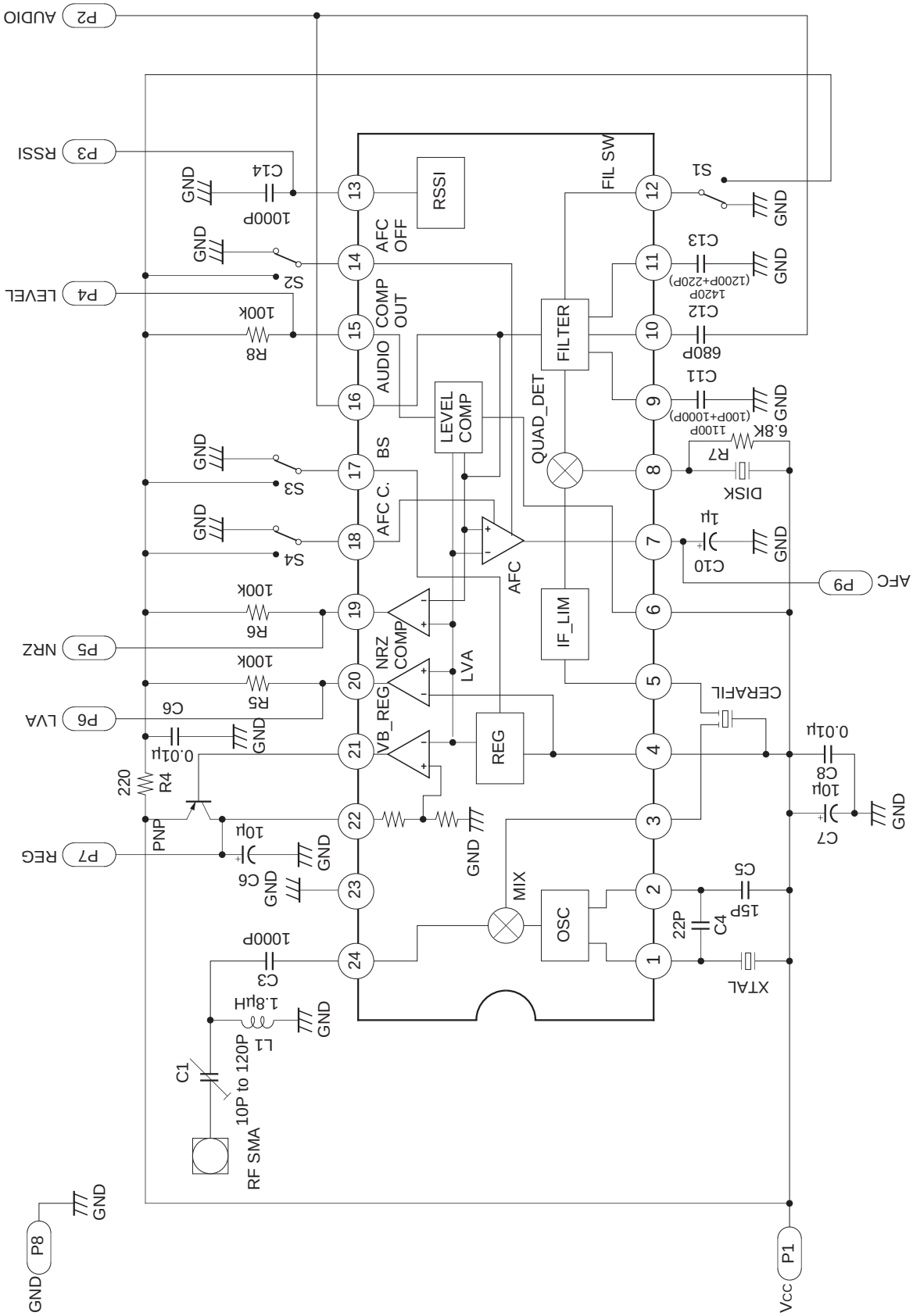


Measurement circuit 9



Measurement circuit 10

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Notes

1) Power Supply

The CXA3179N, with built-in regulator, is designed to permit stable operation at a wide range of supply voltage from 1.1 to 4.0 V. Decouple the wiring to V_{CC} (Pin 4) as close to the pin as possible.

2) Oscillator Input

Oscillator input method

a) Using Pins 1 and 2, input a self-excited oscillation signal through the composition of a Colpitts type crystal oscillator circuit.

b) Directly input a local oscillation signal to Pin 1.

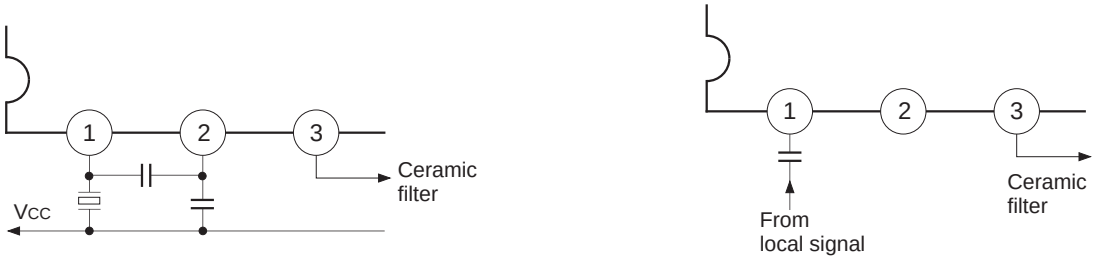


Fig. 1

3) Mixer

The mixer is of double-balance type. Pin 24 is the input pin. Input though a suitable matching circuit. The input impedance is 2.0 kΩ.

Pin 3 serves as the output pin for the mixer, and a load resistance of 1.5 kΩ is incorporated.

4) IF Filter

The filter to be connected between this mixer output and the IF limiter amplifier input should have the following specifications.

I/O impedance	: 1.5 kΩ ±10 %
Band width	: Changes according to applications.

5) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100 dB. Take notice of the following points in making connection to the IF limiter amplifier input pin (Pin 5).

a) Wiring to the IF limiter amplifier input (Pin 5) should be as short as possible.

b) As the IF limiter amplifier output appears at QUAD (Pin 8), wiring to the ceramic discriminator connected to QUAD should be as short as possible to reduce the interference with the mixer output and IF limiter amplifier input.

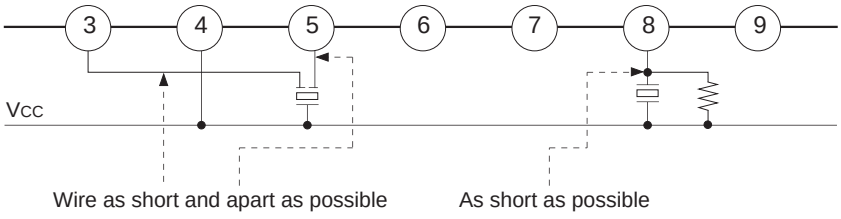


Fig. 2

6) Quick Charge

In order to hasten the Pin 7 rising time from when power is turned on, the CXA3179N features a quick charge circuit. The capacitance value connected to Pin 7 should be chosen such that the voltage does not vary much due to discharge during battery saving.

Connect a signal for controlling the quick charge circuit to Pin 18. Setting this pin high enables the quick charge mode, and setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time.

Connect Pin 18 to GND when quick charge is not being used.

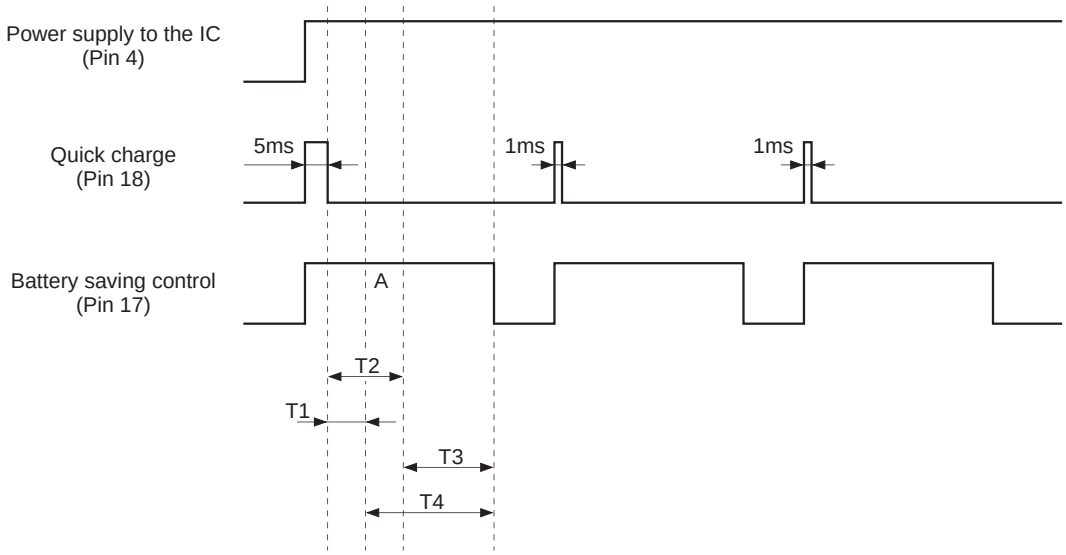


Fig. 3

Example when the Pin 7 REF capacitance value is 1 µF

T1 in Fig. 3 : 2-level data setting time after quick charge
0 ms

T2 in Fig. 3 : 4-level data setting time after quick charge
2 ms or less

T3 in Fig. 3 : 4-level data can be obtained

T4 in Fig. 3 : 2-level data can be obtained

7) Detector

The detector is of quadrature type. To perform phase shift, connect a ceramic discriminator to Pin 8.
The phase shifting capacitor for the quadrature detector is incorporated. The FM (FSK) signal demodulated with the detector will be output to AUDIO (Pin 16) through the internal LPF.
The AUDIO output is the anti-phase output to the NRZ OUT.

The CDBM455C50 (MURATA MFG. CO., LTD.) ceramic discriminator is recommended for the CXA3179N. For the 2-level system, the CDBM455C28 can also be used.

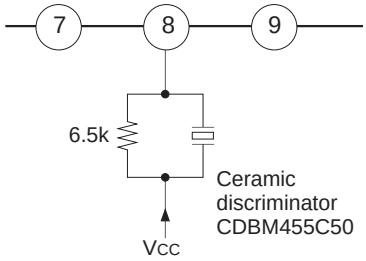


Fig. 4

The detector output level is changed according to the resistance value connected to Pin 8.

8) Filter Buffer, Level Comparator and NRZ Comparator

The LPF circuit is built in this IC.
The LPF output is connected internally to the NRZ comparator, level comparator and quick charge circuit.

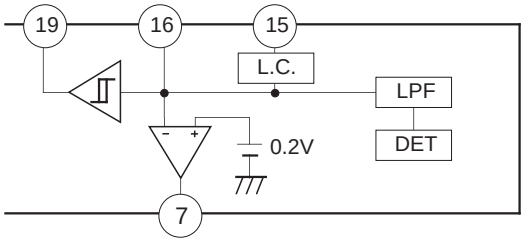


Fig. 5

Using the LPF, remove the noise from the demodulated signal and input the signal to the above three circuits.

8) -1. LPF Constant

The composition of the data filter is ternary.
The first-stage cut-off f_{C1} is

$$f_{C1} = \frac{1}{2\pi C_{11} R}$$

The second-stage cut-off f_{C2} is

$$f_{C2} = \frac{1}{2\pi R\sqrt{C_{12}\, C_{13}}} \quad , \quad Q = \sqrt{\frac{C_{12}}{C_{13}}}$$

C_{11}, C_{12}, C_{13} : External capacitance shown in the Application Circuit
R : IC internal resistance

The Butterworse characteristic is for $C_{12}=C_{13}=C_{14}$.

R is approximately 55 kΩ ±20 % when Pin 12 is low. The table below shows the example of constants to data rate.

		Capacitance (pF)	fc (Hz)	Data rate
Pin 12 filter switch	H	6800	—	—
	L		430	512 bps (2 levels)
	H	1500	950	1200 bps (2 levels)
	L		1900	2400 bps (2 levels)
	H	PIN9 1100 P PIN10 680 P PIN11 1420 P	1000	1600 bps (2 levels)
	L		2000	3200 bps (2 levels)
	H	PIN9 1100 P PIN10 680 P PIN11 1420	1000	3200 bps (4 levels)
	L		2000	6400 bps (4 levels)

8) -2. Comparator Output

The level comparator and the NRZ comparator shape the waveform of this input signal and output it as a square wave. The comparator output stage is for open collector.
Thus, if the CPU is of CMOS type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

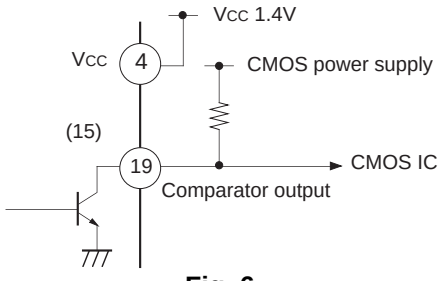
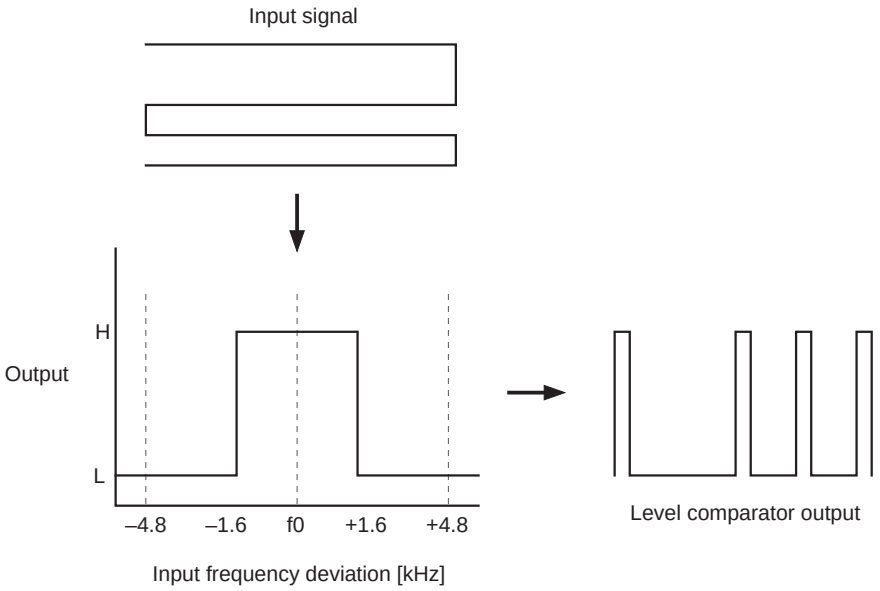


Fig. 6

8) -3. Level Comparator Output

The level comparator characteristics are as shown in the figure below. Therefore, a high signal is output at the bit border even if the input signal is a ±4.8 kHz signal. This high output interval varies according to the frequency response of the bit rate filter, and widens as the cut-off frequency becomes lower. The decoder avoids this high interval when processing data.



9) REG CONT

Controls the base bias of the external transistors.

10) LVA OUT

This pin goes high (open) when the supply voltage becomes lower. Since the output is an open collector, it can be used to directly drive the CMOS device. The setting voltage of the LVA is 1.05 V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 50 mV (typ.).

11) B.S.

Operation of the CXA3179N can be halted by setting this pin low. This pin can be connected directly to the CMOS device. The current consumption for battery saving is 10 µA or less (at 1.4 V).

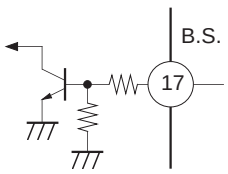


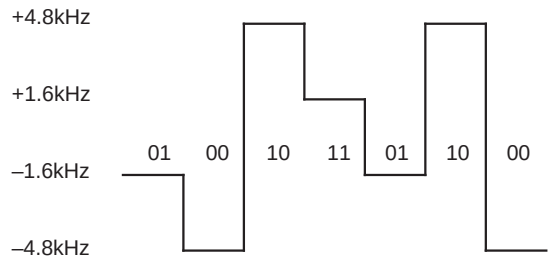
Fig. 7

12) M-ary (M=2- or 4-level) FSK Demodulation System

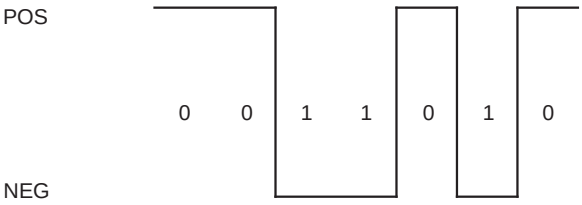
12)-1. Output Waveform

Polarity discrimination output and level comparator output are used to demodulate the 4-level waveform shown below.

[4-level FSK demodulating waveform]

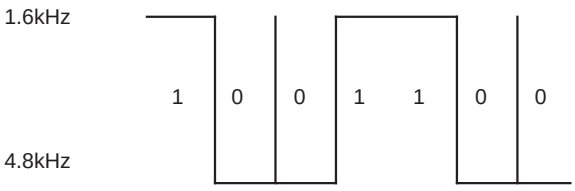


[NRZ OUT] Polarity discrimination output (When the input frequency is higher than the local frequency)



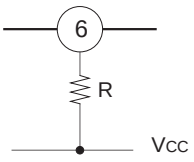
The polarity can be inverted by setting the local frequency higher than the input frequency.

[L.C. OUT] Level comparator output



The 4-level FSK demodulating data is divided into an NRZ OUT and L.C. OUT shown above. Here, the NRZ OUT corresponds to a conventional NRZ comparator output. The L.C. OUT is made comparing the demodulated waveform amplitude to the IC internal reference voltage levels. When the threshold value of L.C. OUT is not appropriate to the detector output, the resistance value on Pin 8 should be varied for the detector output level adjustment or the resistor should be inserted between Pin 6 and V_{CC} for the level comparator threshold value adjustment.

For the 2-level FSK demodulation, it corresponds to a conventional NRZ comparator output.

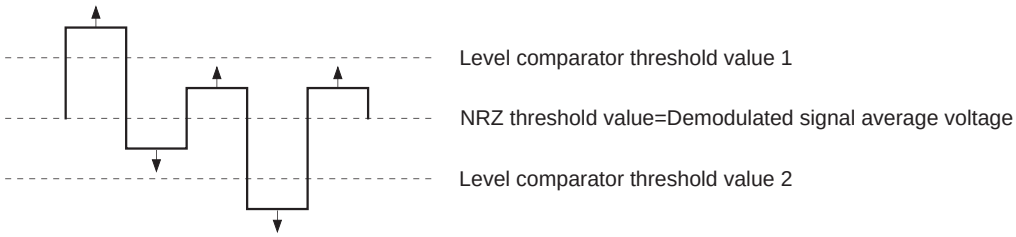


12)-2. 4-level Signal and Threshold Value

The demodulated signal is optimally matched to the NRZ comparator threshold value by applying AFC (see 13) AFC). (operation point correction using a feedback loop filter)

The comparator threshold value is fixed.

The level comparator threshold value can be adjusted by varying the detector output level by changing the damping resistance of the discriminator. (AC gain adjustment)



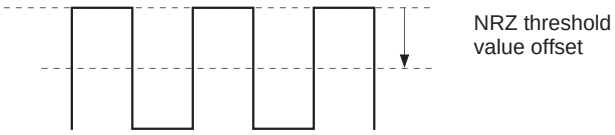
AC gain adjustment

12)-3. Offset Amount and Threshold Value

Immediately after power-on when the REF capacitor is not charged with the correction voltage, if the input frequency has an offset, some time is required to correct this offset. In addition, the times required to obtain 2-level and 4-level data differ according to the offset amount.

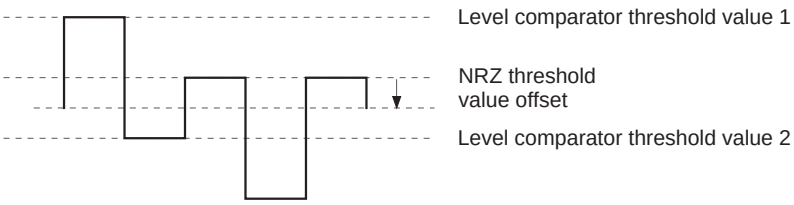
a) 2-level signals

In the case of 2-level signals, correct data is obtained when the offset amount is smaller than the detector output amplitude. This is 75 mV or less when the detector output level is 150 mVp-p which corresponds to within ±4.8 kHz when converted to a frequency by the S curve. Thus, 2-level data is obtained without an operation point correction time lag when the frequency offset is within ±4.8 kHz.



b) 4-level signals

In the case of 4-level signals, correct data is obtained when the offset amount is less than 1/3 of the detector output amplitude (during ±4.8 kHz DEV). This is 25 mV or less when the detector output level is 150 mVp-p which corresponds to ±1.6 kHz or less when converted to a frequency by the S curve. Thus, 4-level data is obtained without an operation point correction time lag when the frequency offset is within ±1.6 kHz

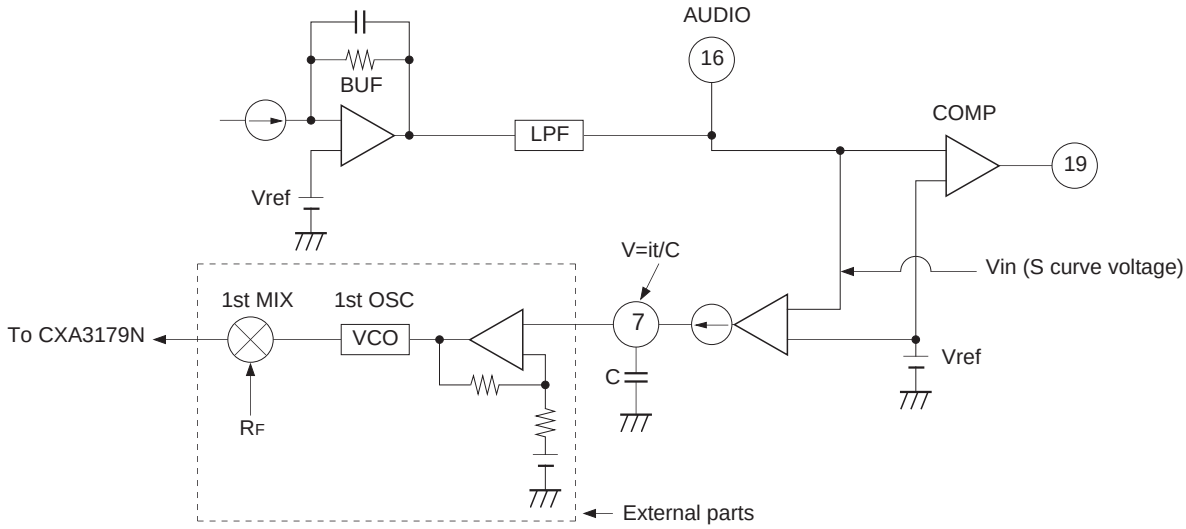


As shown above, 4-level signals have an allowable offset range 1/3 that of 2-level signals. When the offset exceeds this allowable range, time is required to determine the operation point and obtain correct data through feedback. Also, even if the offset is within the allowable range, the output pulse duty changes until the offset is 0.

13) AFC

The AFC is of the current output type which outputs the frequency deviation in the form of the current and converts it to the voltage. The output current range is approximately ±0.4 µA for the slow mode and ±70 µA for the fast mode. The circuit to be connected with this pin should have the higher impedance.

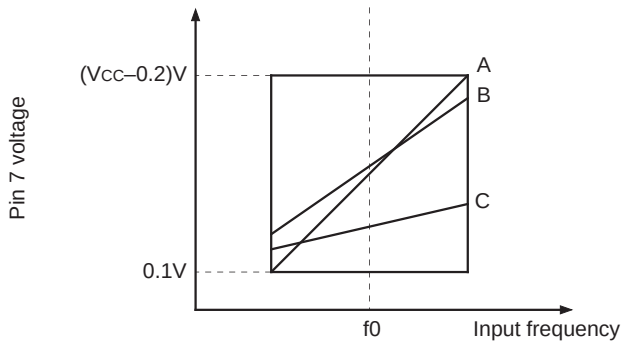
The operating range of the AFC pin is between approximately 0.1 V to (V_{CC} –0.2) V. Use the buffer amplifier to expand the operating range.



The Pin 7 voltage V continues to change till the Vin value reaches the Vref value. When these values are equal, the Pin 7 output current becomes “0” and the voltage is determined by the charge and time.

Therefore, the Pin 7 voltage is undefined.

The AFC voltage varies, for example, as shown below by the VCO characteristics. The AFC voltage follows the VCO characteristics because this voltage is independent of the slope of the S curve. In other words, the CXA3179N operates according to the VCO characteristics when the VCO characteristics have the linearity with respect to the voltage and the VCO characteristics can be controlled within the range shown in the graph below.



14) Sensitivity Adjustment Method

The constants shown in the Application Circuit are for the standard external parts. However, adjustment may be necessary depending on the conditions of use, characteristics of external parts, and the RF system circuit and decoder connected to the IF IC, etc. Adjust the sensitivity according to the following procedures.

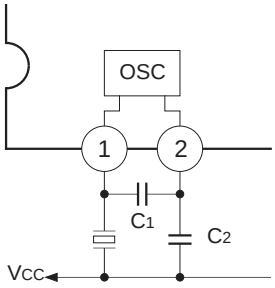
a) MIX IN matching

When using a matching circuit between the RF system circuit and MIX IN of the CXA3179N, adjust the trimmer to obtain the optimal sensitivity while monitoring the AUDIO output.

b) Local input level

The mixer circuit gain is dependent on the local signal input level to OSC IN. The input level to OSC IN should be set as high as possible within the range of –6 to +2 dBm as shown in the graph of "Local input level vs. Mixer gain characteristics". However, care should be taken as raising the input level above +2 dBm will cause the sensitivity to drop.

When creating the local signal using the internal oscillator circuit, the oscillation level varies according to the external capacitances attached to Pins 1 and 2 and the characteristics of the used crystal. Therefore, be sure to adjust the external capacitance values attached to Pins 1 and 2 according to the crystal characteristics.



C_1 and C_2 have the following range in the figure above.

$C_1 \geq C_2$

$C_1 = C_2$ to $C_1 = 5C_2$

As for the ratio of C_1 to C_2, the oscillation stabilizes as C_1 approaches equality with C_2.

The oscillation level decreases as the C_1 and C_2 values become larger, and increases as the C_1 and C_2 values become smaller.

Use a FET probe to confirm the local input level.

c) LPF constant

The data filter cut-off may need to be changed depending on the characteristics of the connected decoder. Adjust the capacitance values of Pins 9 to 12 while checking the incoming sensitivity including the decoder. If the capacitance values are too large, the detector output waveform will deviate at high data rates, causing the sensitivity to drop. Conversely, if the capacitance values are too small, the LPF will be easily affected by noise, causing the sensitivity to drop.

Adjust capacitance values of Pins 9 to 12 so that the capacitance value described in "8)-1. LPF Constant" becomes smaller.

d) Detector output level

The NRZ comparator and level comparator threshold values are fixed for the CXA3179N. In the case of 4-level signals, the relationship between the level comparator threshold value and the detector output level affects the sensitivity. The detector output level can be adjusted by the resistance attached to Pin 8. Increasing the resistance value also increases the output level, and vice versa.

The Pin 8 resistance value differs according to the ceramic discriminator attached to Pin 8. When the discriminator is changed to a different type, the resistance value must be adjusted.

Adjust the resistance value while monitoring the level comparator output waveform or the sensitivity including the decoder.

e) AFC

The CXA3179N uses AFC to correct the IF frequency deviation. When the IF frequency deviation amount is large, correction takes time and may lower the sensitivity. Adjust the oscillator frequency of the local oscillator so that the center frequency of the signal input to Pin 5 (IF IN) is as close to 455 kHz as possible.

15) CXA3179N Standard Board Description

- Outline

  This board contains the external parts shown in the Application Circuit in order to evaluate the CXA3179N operation

- Features

  The following CXA3179N basic operations can be checked.

  1) Varying the data filter cut-off
  2) Battery saving and other mode switching
  3) NRZ output and level comparator output pins
  4) AFC pin — Pin 7 serves as the output pin for the AFC.

- Method of use

  1) Input the CXA3179N supply voltage V_{CC}=1.4.
     This IC operates with a single power supply.
  2) The CXA3179N uses a 21.245 MHz crystal. Input the RF signal from the RF pin and use this IC in the condition where IF=455 kHz.
  3) The AFC pin voltage is undefined with the IC itself because the current output circuit is employed for the AFC. For the evaluation, be sure to apply the bias to the AFC pin externally or to make the AFC loop.
  4) Set the mode switches.

- Mode switch setting

  Mode switches S1, S2, S3 and S4 are provided in four locations in the board. Each basic operation can be confirmed by switching these mode switches while referring to the board layout. See the table in “15) Control Pins” for the mode switching.

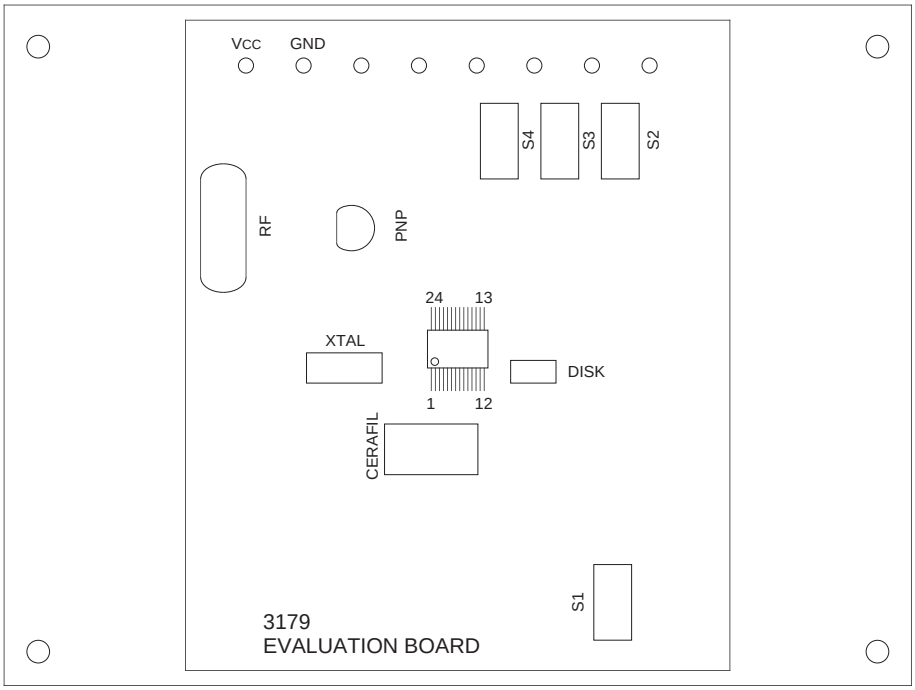
- Device specification

  See these specifications for the IC specifications. The ICs for this evaluation board are ES specification.

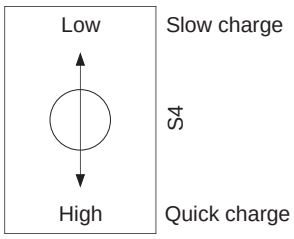
- Circuit diagram

  The circuit diagram is the same as the Application Circuit in these Specifications.

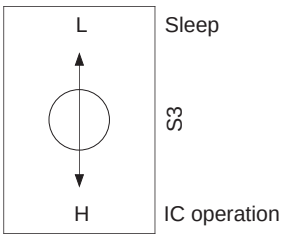
15) -1. Standard Board Layout



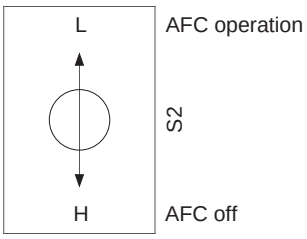
15) -2. Mode Switch Pattern



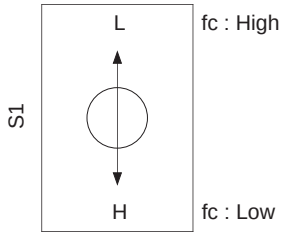
AFC C.



B.S.



AFC-OFF



FIL SW

15) -3. List of Standard Board Parts

Value	Part #	Remarks (Manufacture)	Note
Resistor			
220	R4	(RIVER)	E12 series 1/8W
8.7 k	R7		
100 k	R5 R6 R8		
Capacitor			
6.8 P to 45 P	C2	TZ03P450FR169 (MURATA PRODUCTS)	TRIMMER CAPACITOR
15 P	C5	DD100 series temperature characteristics type B (MURATA PRODUCTS)	CERAMIC CAPACITOR E12 series (high dielectric constant type)
22 P	C4		
100 P	C14		
1000 P	C3		
1100 P	C11		
680 P	C12		
1420 P	C13		
0.01 µ	C8 C9		
1 µ	C10	25 V 1 µ (SHIN-EI TUSHIN KOGYO CO., LTD.)	ELECTROLYTIC CAPACITOR E6 series
10 µ	C6 C7	25 V 10 µ (SHIN-EI TUSHIN KOGYO CO., LTD.)	
Inductor			
1.8 µH	L1	EL0405 (TDK Products)	E12 series 2.5 mm pitch (Lead Pitch)
Active Component			
	PNP	2SA1015 (TOSHIBA CORPORATION)	
Crystal			
21.245 MHz	XTAL	NR-18BN (NIHON DEMPA KOGYO CO., LTD.)	

Ceramic Filter

	CERAFIL	CFWS455D (MURATA PRODUCTS)	455 kHz 1.5 kΩ

Ceramic Discriminator

	DISC	CDBM455C50 (MURATA PRODUCTS)	455 kHz

Switch

	S1, S2 S3, S4	ATE1D-2M3-10 (FUJISOKU CORPORATION)	ON-ON (1 poles)

Connector

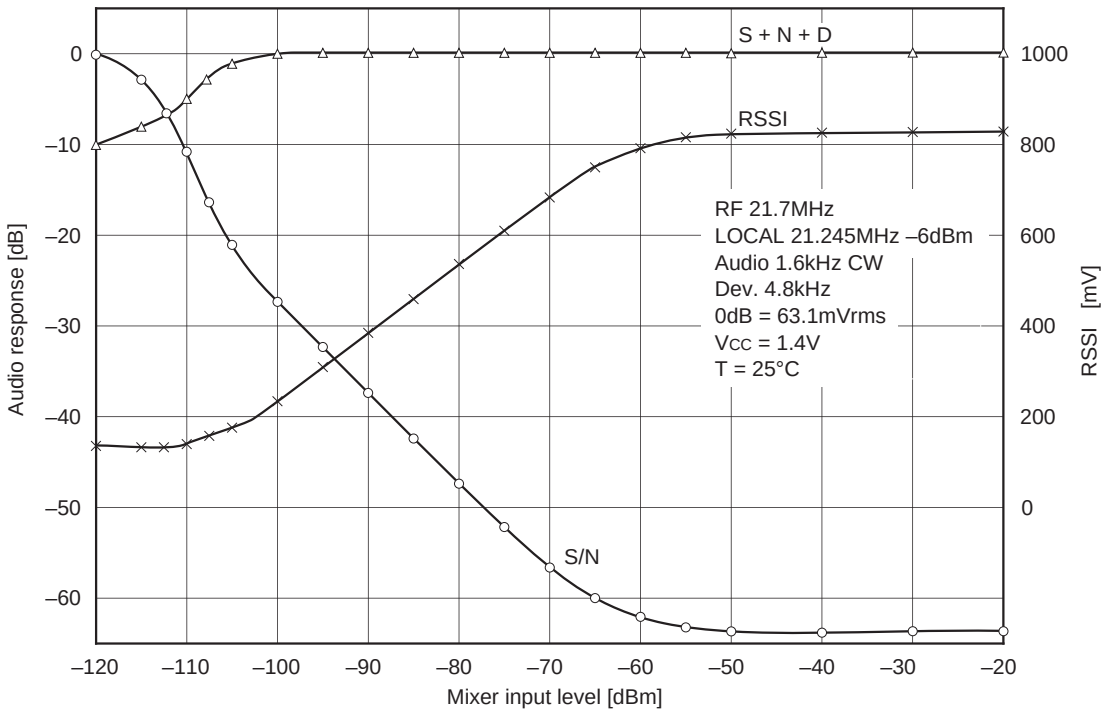
	RF	HRM300-25 (HIROSE ELECTRIC CO., LTD.)	SMA CONNECTOR

Pin

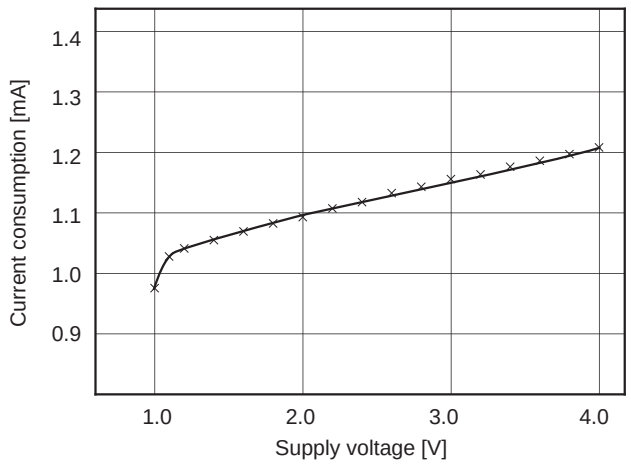
	× 2	Mac 8 test pin ST-1-3 (Mac eight)	L=10 mm 0.8 ϕ
	× 6	Mac 8 test pin LC-2-G (Mac eight)	

Example of Representative Characteristics

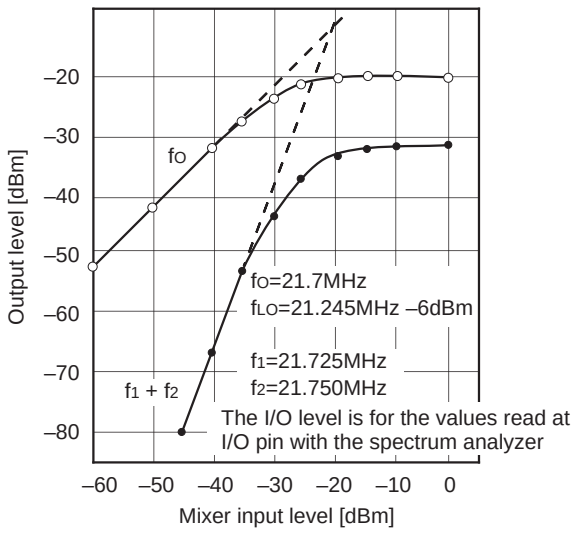
Mixer input audio response and RSSI characteristics



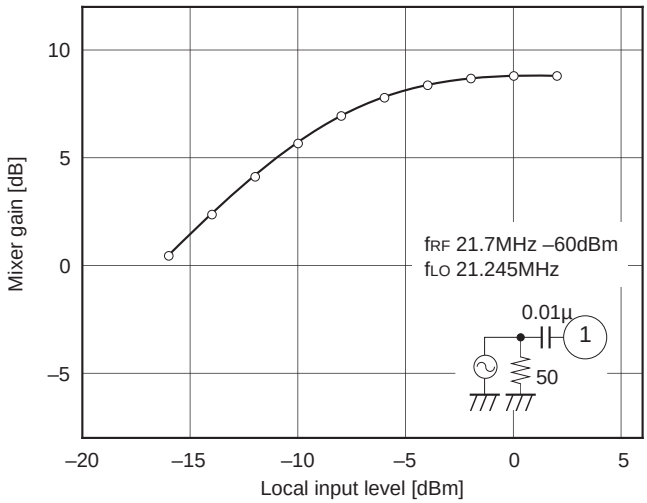
Current consumption characteristics



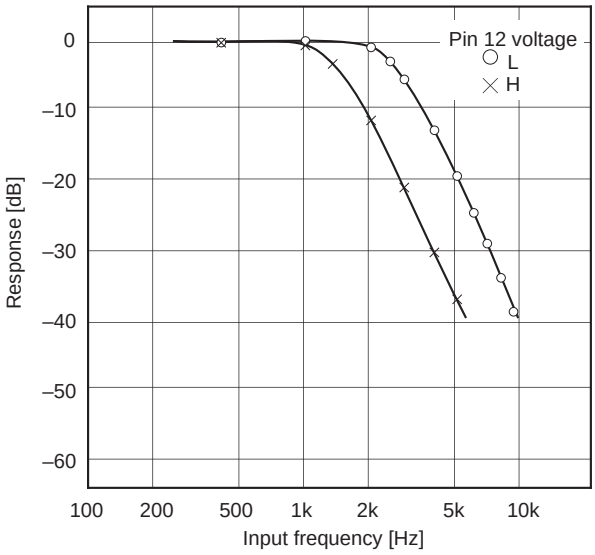
Mixer I/O characteristics and 3rd intercept point



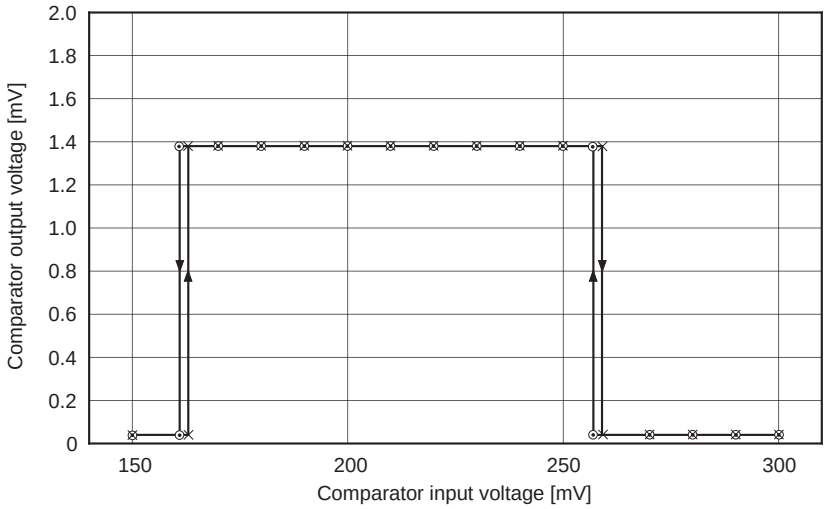
Local input level vs. Mixer gain characteristics



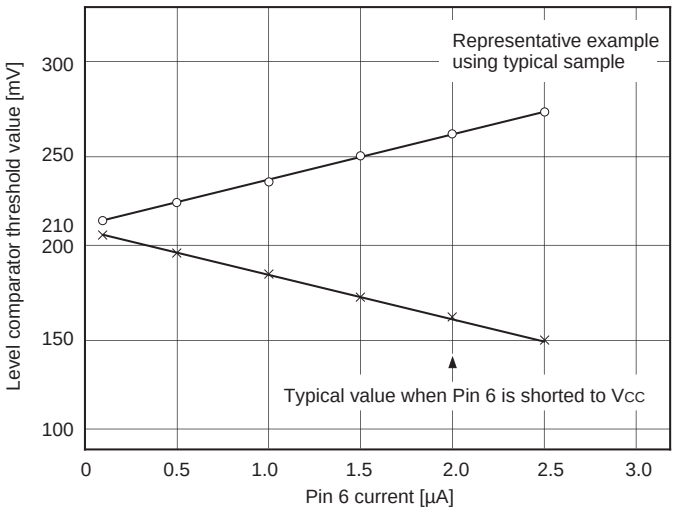
Variable cut-off characteristics of audio filter



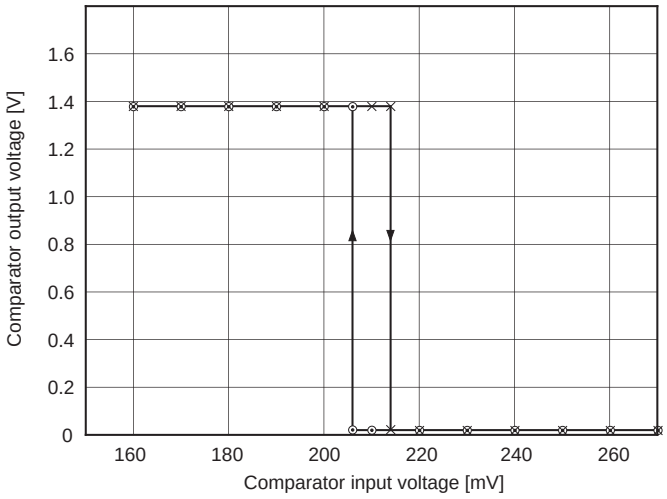
Level comparator characteristics



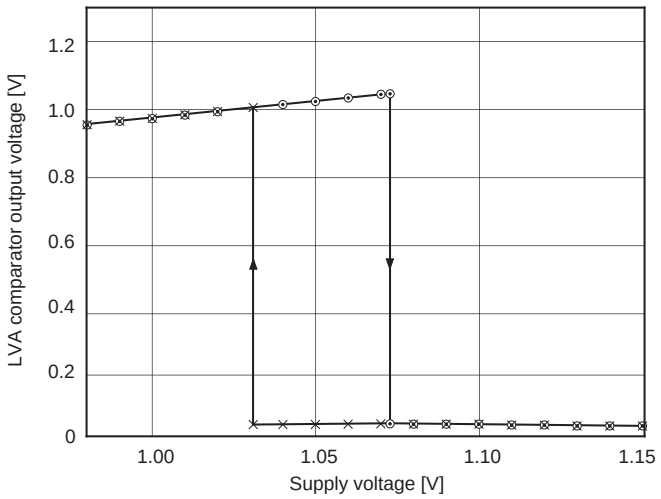
Level comparator threshold value control characteristics
(Output low → high switching level)



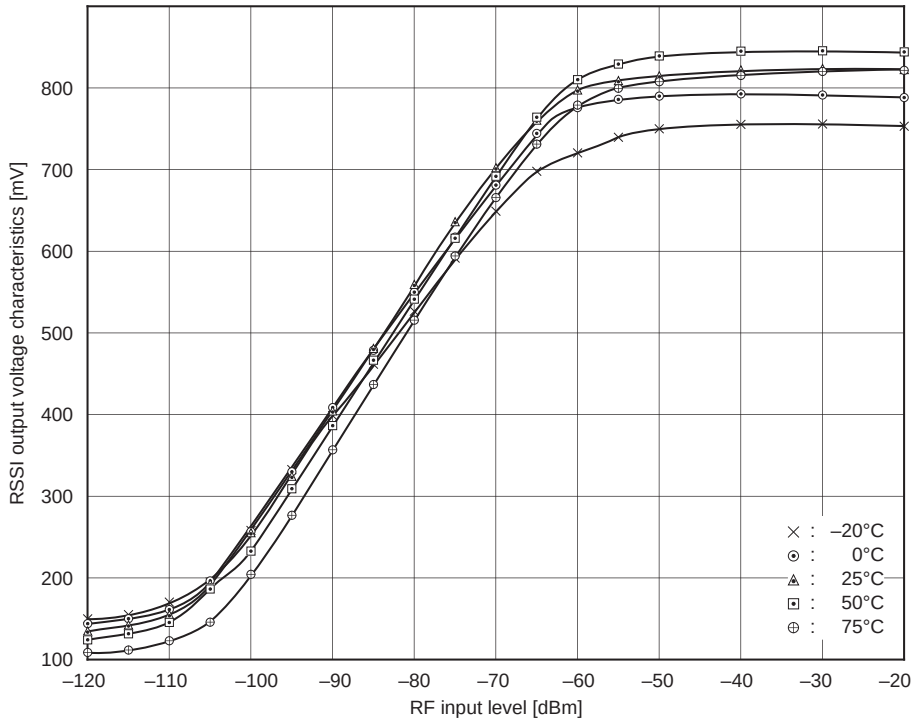
NRZ comparator characteristics



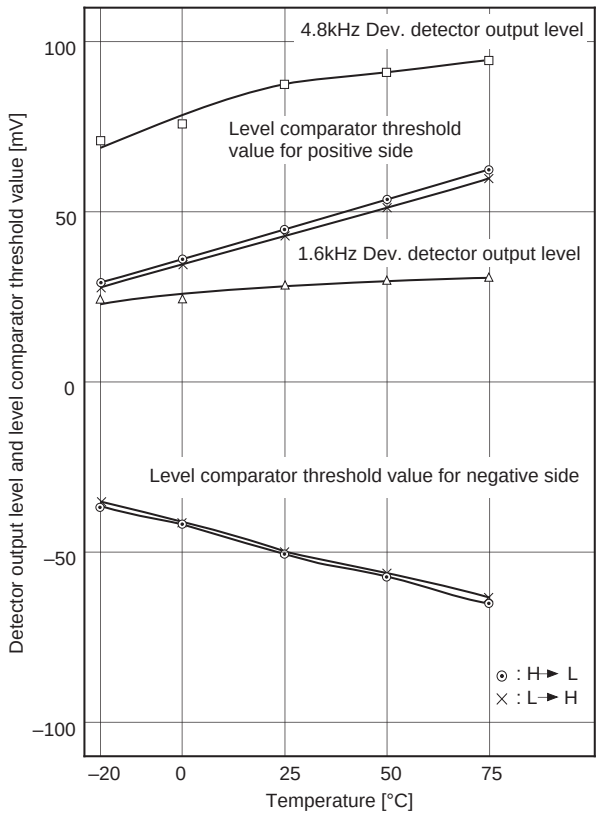
LVA characteristics



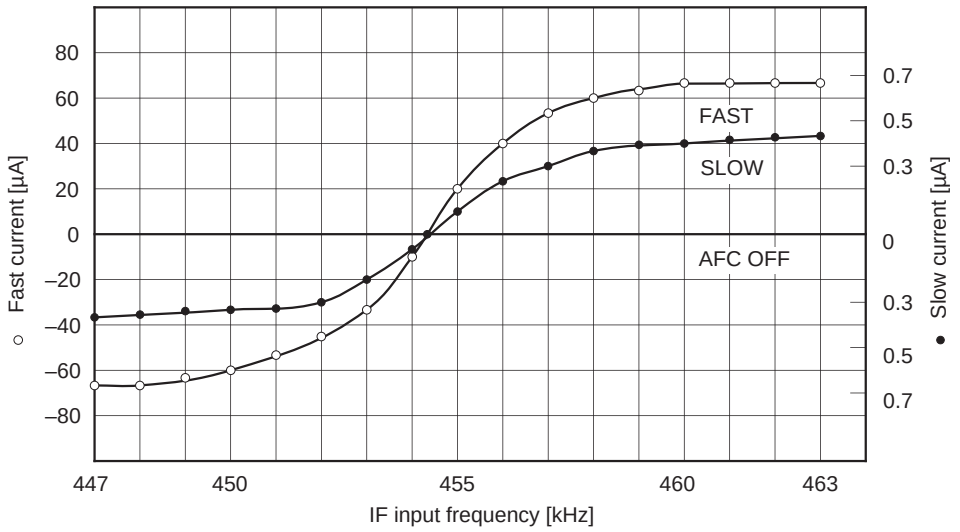
RSSI output voltage temperature characteristics



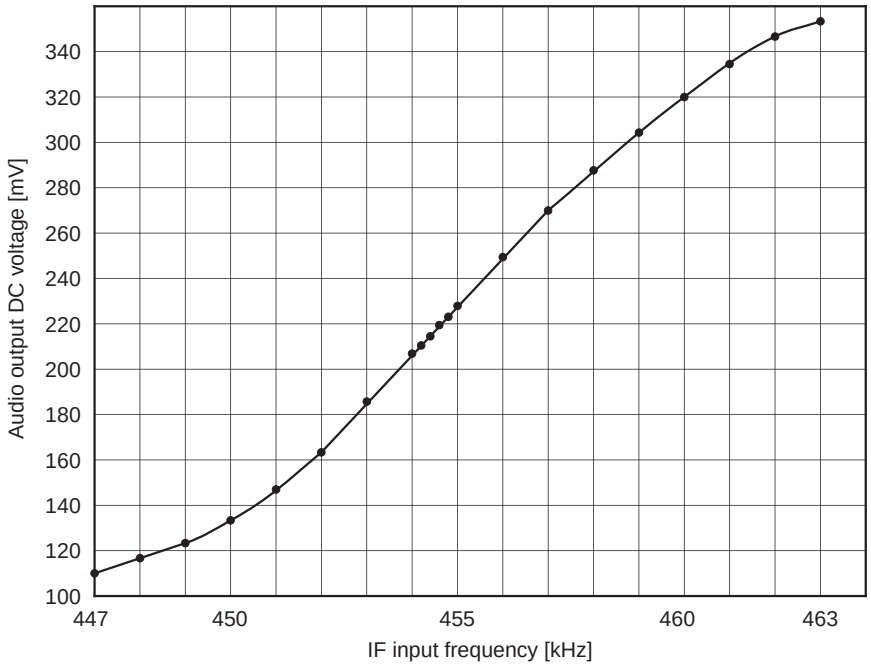
Detector output level and level comparator threshold value temperature characteristics



AFC output current characteristics

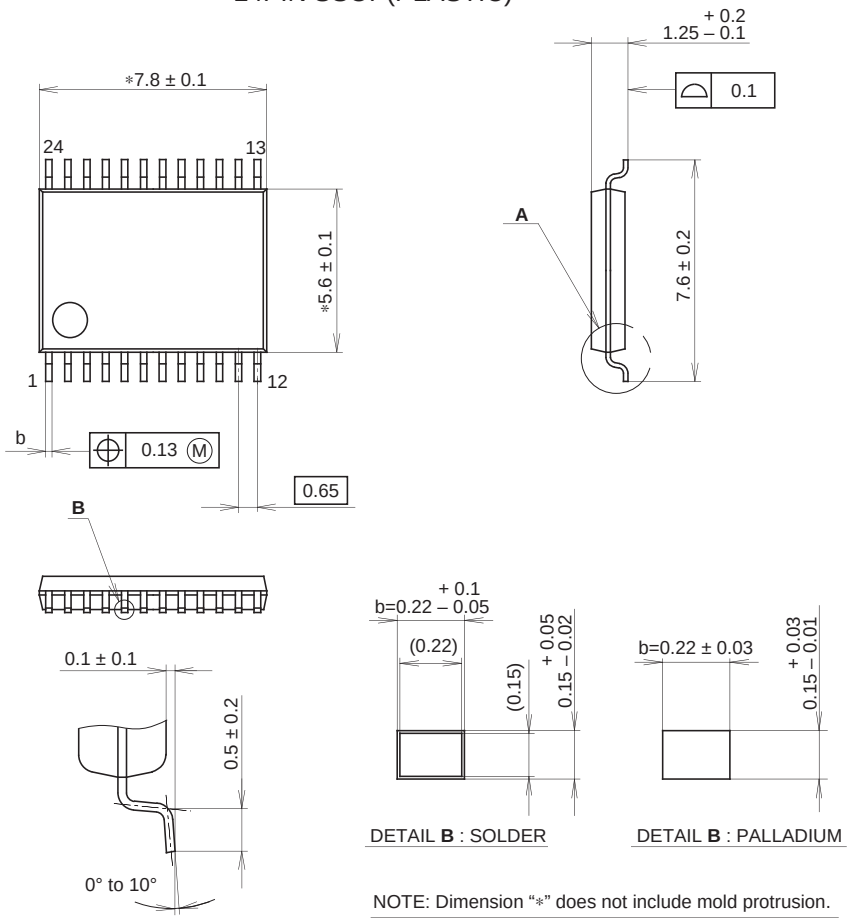


S curve characteristics



Package Outline Unit : mm

24PIN SSOP(PLASTIC)



DETAIL **A**

DETAIL **B** : SOLDER

DETAIL **B** : PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).