SONY

CXA3238TN/CXA3239TN

6/4-channel Read/Write Amplifier for GMR-Ind Head Hard Disk Drive

Description

The CXA3238TN/CXA3239TN is a Read/Write amplifier for GMR-Ind (Giant Magneto Resistive-Inductive) heads used in hard disk drives, and is capable of supporting up to six channels.

Features

- +5 V and –3 V power supply.
- Current bias voltage sense type.
- Drives up to six heads (CXA3238TN)
- Drives up to four heads (CXA3239TN)
- Low power 180 mW at Read
- Differential read amplifier gain ; ×140/190 (R_{MR}=50 Ω)
- Input noise of 0.77 nV/$\sqrt{\text{Hz}}$ (typ.), R_{MR}=50 Ω, I_B=6.0 mA.
- Recovery time write to read ; 300 nsec. (typ.)
- Write data is triggered by differential P-ECL signal.
- Servo bank write. (All channels)
- Write unsafe detection circuit.
- Serial port …
  - Head selection
  - MR bias
  - Write current

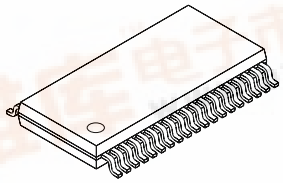
Applications

Hard disk drives with GMR-Ind heads.

Structure

Bipolar silicon monolithic IC

38 pin TSSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	–0.3 to +6	V
• Supply voltage	V_{EE}	–4.5 to +0.3	V
• Digital input voltage	Vdi	–0.3 to V_{CC}+0.3	V
• Operating temperature	Topr	–20 to +70	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation			
TSSOP38	P_D	1000	mW

Operating Conditions

• Supply voltage	V_{CC}	+4.4 to +5.5	V
	V_{EE}	–4.0 to –2.6	V
• MR bias voltage	V_{MR}	–300 to +300	mV
• Bias current	I_B	3 to 8	mA
• Write current	I_W	15 to 45	mA

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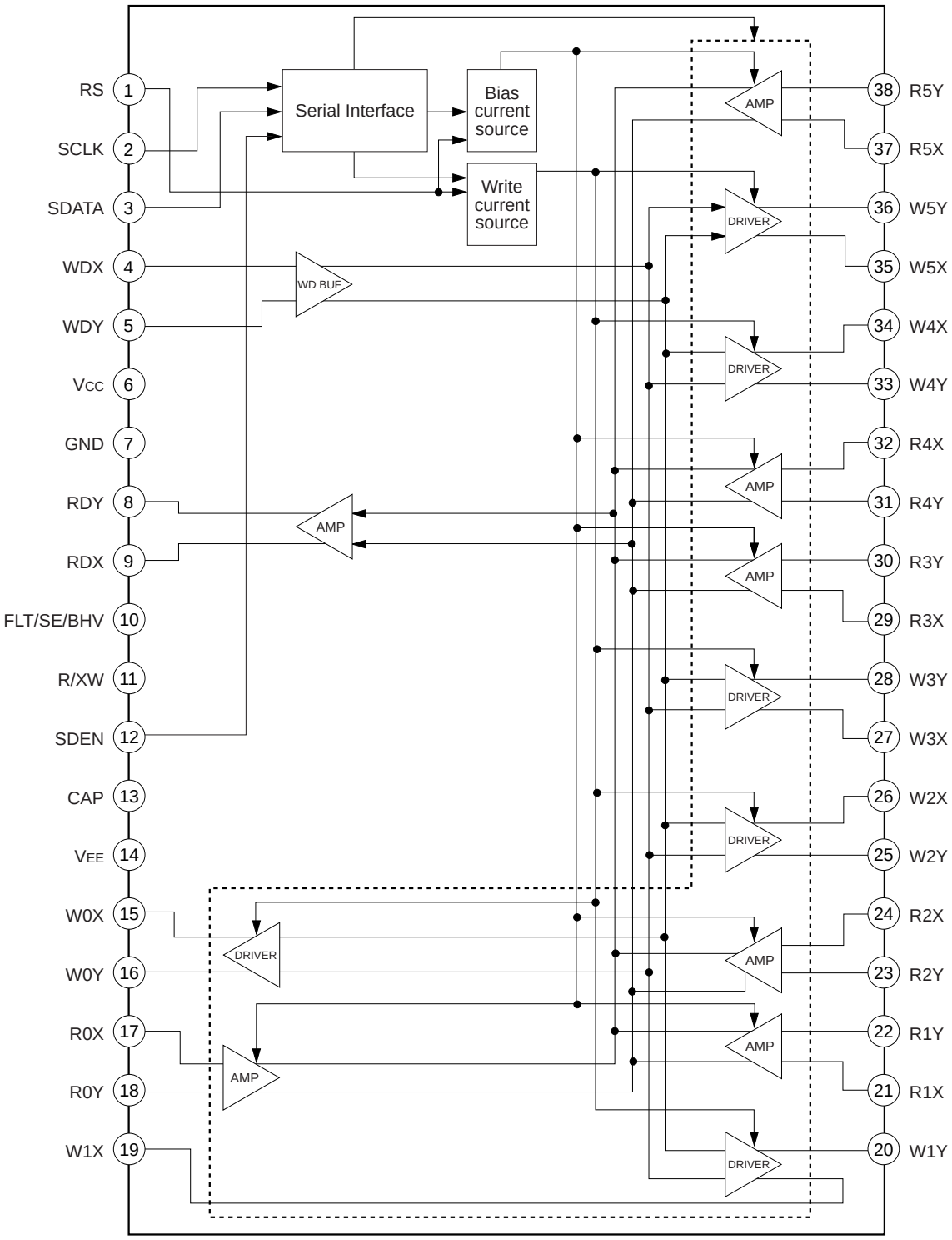
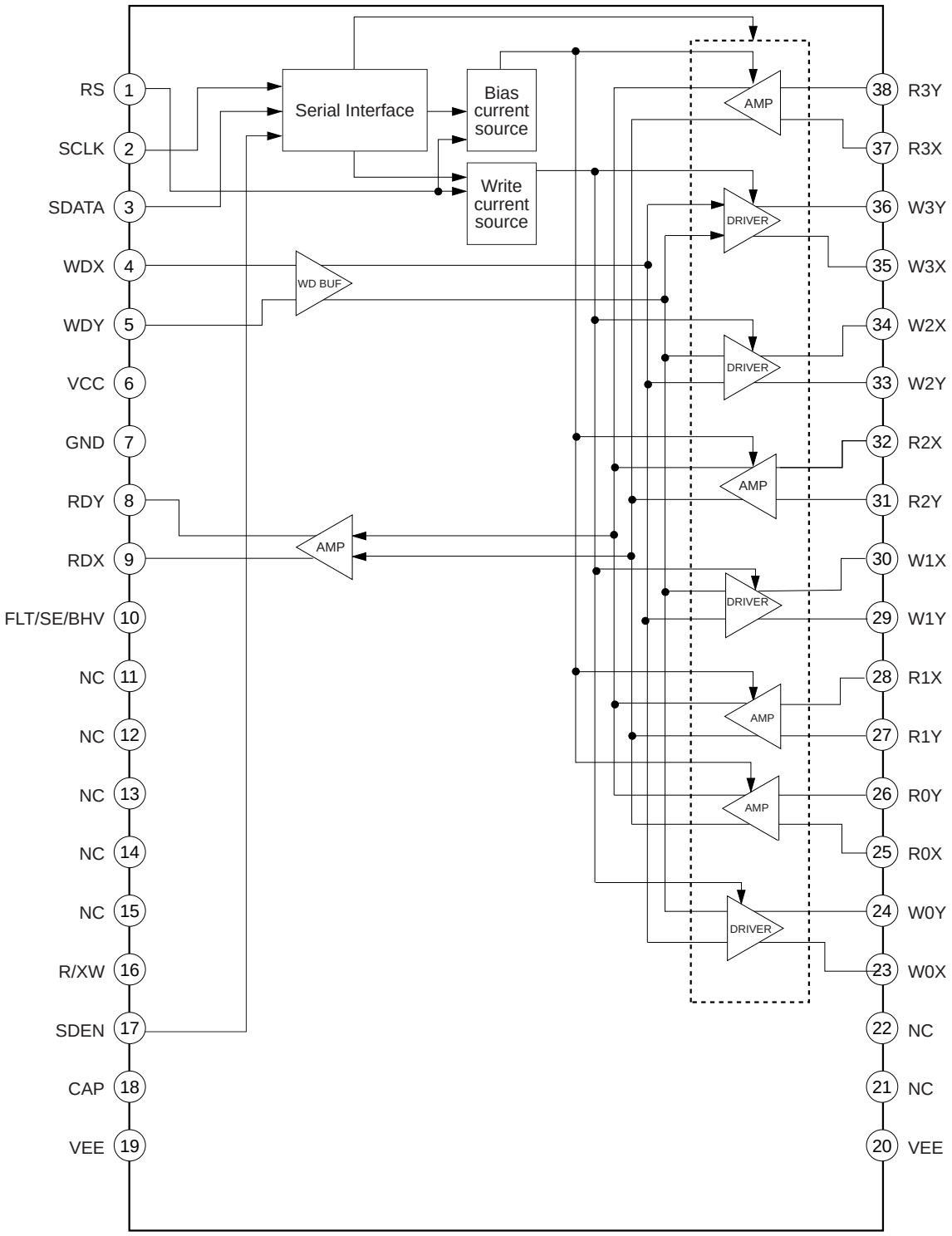
Block Diagram and Pin Configuration

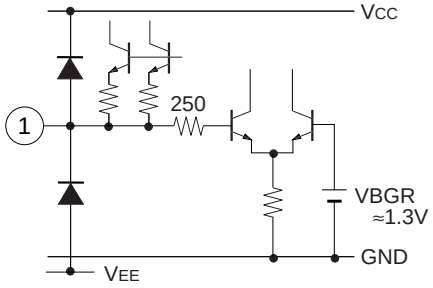
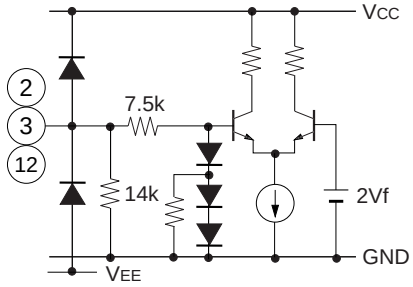
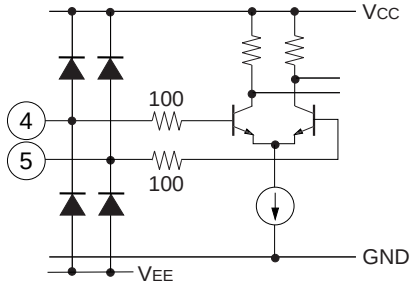
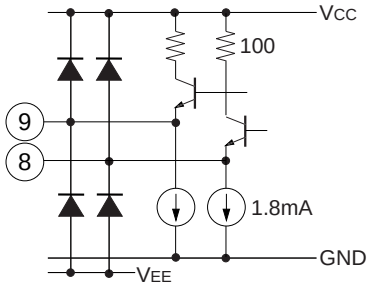
CXA3238TN

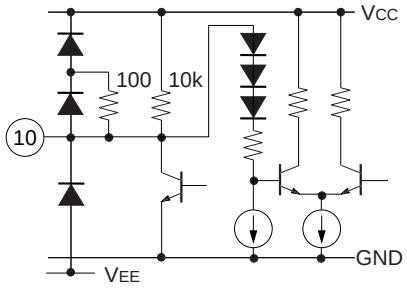
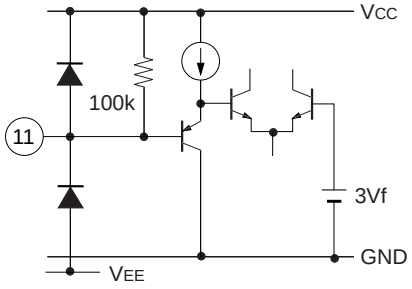
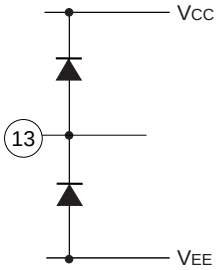
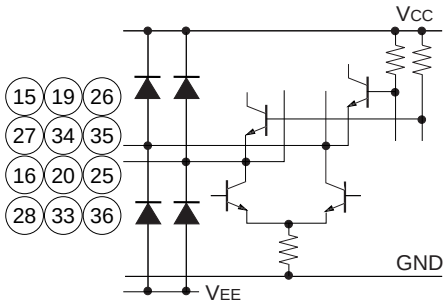


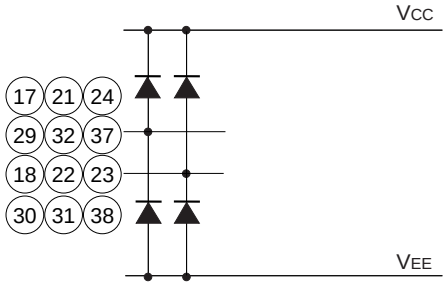
CXA3239TN


RS 1
SCLK 2
SDATA 3
WDX 4
WDY 5
VCC 6
GND 7
RDY 8
RDX 9
FLT/SE/BHV 10
NC 11
NC 12
NC 13
NC 14
NC 15
R/XW 16
SDEN 17
CAP 18
VEE 19
Serial Interface
Bias current source
Write current source
WD BUF
AMP
DRIVER
AMP
DRIVER
AMP
DRIVER
AMP
AMP
DRIVER
38 R3Y
37 R3X
36 W3Y
35 W3X
34 W2X
33 W2Y
32 R2X
31 R2Y
30 W1X
29 W1Y
28 R1X
27 R1Y
26 R0Y
25 R0X
24 W0Y
23 W0X
22 NC
21 NC
20 VEE

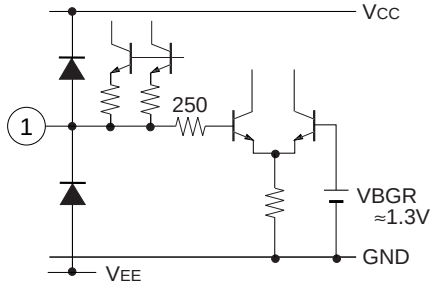
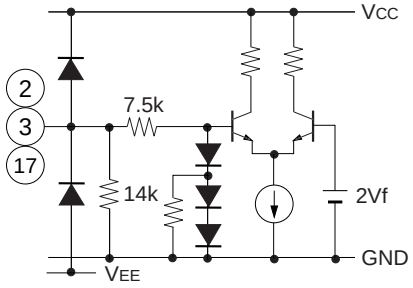
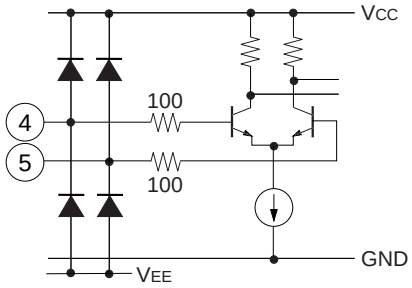
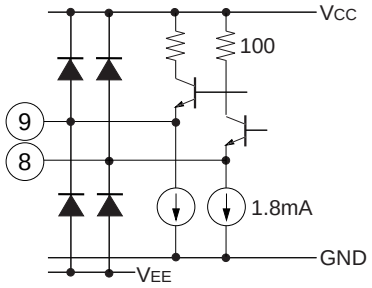
Pin Description CXA3238TN

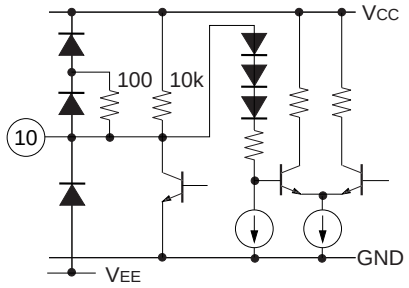
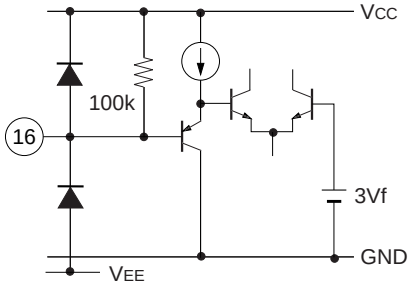
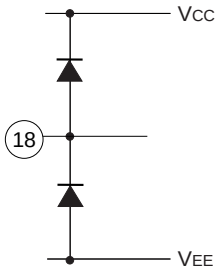
Pin No.	Symbol	Equivalent circuit	Description
1	RS		Bias current setting resister is connected between this pin and GND.
2 3 12	SCLK SDATA SDEN		Serial control signal input.
4 5	WDX WDY		Differential P-ECL write data input.
6	Vcc		5 V power supply.
7	GND		Ground
9 8	RDX RDY		Read amplifier output with coupling capacitors. High impedance in the write mode.

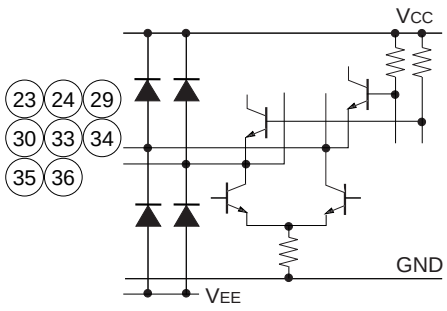
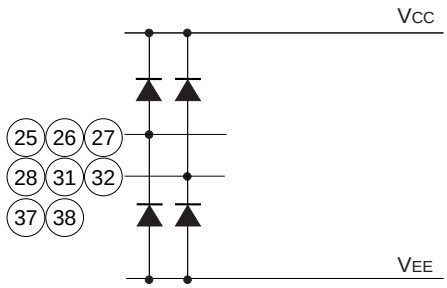
Pin No.	Symbol	Equivalent circuit	Description
10	FLT/SE/BHV		Head unsafe detection output. Servo Bank Write Enable input. Buffered Head Voltage output.
11	R/XW		Read / Write control signal input. Read when high, Write when low.
13	CAP		Connect an external capacitor of Read amplifier between this pin and VEE.
14	VEE		–3 V power supply.
15 16 19 20 26 25 27 28 34 33 35 36	W0X W0Y W1X W1Y W2X W2Y W3X W3Y W4X W4Y W5X W5Y		Inductive heads for Write. Six channels are provided.

Pin No.	Symbol	Equivalent circuit	Description
17 18 21 22 24 23 29 30 32 31 37 38	R0X R0Y R1X R1Y R2X R2Y R3X R3Y R4X R4Y R5X R5Y		MR heads for Read. Six channels are provided.

Pin Description CXA3239TN

Pin No.	Symbol	Equivalent circuit	Description
1	RS		Bias current setting resister is connected between this pin and GND.
2 3 17	SCLK SDATA SDEN		Serial control signal input.
4 5	WDX WDY		Differential P-ECL write data input.
6	Vcc		5 V power supply.
7	GND		Ground
9 8	RDX RDY		Read amplifier output with coupling capacitors. High impedance in the write mode.

Pin No.	Symbol	Equivalent circuit	Description
10	FLT/SE/BHV		Head unsafe detection output. Servo Bank Write Enable input. Buffered Head Voltage output.
11 12 13 14 15 21 22	NC		Non Connection
16	R/XW		Read / Write control signal input. Read when high, Write when low.
18	CAP		Connect an external capacitor of Read amplifier between this pin and VEE.
19, 20	VEE		–3 V power supply.

Pin No.	Symbol	Equivalent circuit	Description
23 24 29 30 33 34 35 36	W0X W0Y W1Y W1X W2Y W2X W3X W3Y		Inductive heads for Write. Four channels are provided.
25 26 27 28 31 32 37 38	R0X R0Y R1Y R1X R2Y R2X R3X R3Y		MR heads for Read. Four channels are provided.

Electrical Characteristics

(Unless otherwise specified; V_{CC}=5 V, V_{EE}=–3 V, Ta=25 °C, CAP=0.1 µF, RS=7.5 kΩ)

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Power Dissipation			I_W=31 mA, I_B=6.0 mA				
1-1	V_{CC} power supply current	I_{SP1}	SLEEP mode		2.1	2.8	mA
1-2		I_{ID1}	IDLE mode		22	29	mA
1-3		I_{RE1}	Read mode		36	47	mA
1-4		I_{WR1}	Write mode		80	100	mA
1-6	V_{EE} power supply current	I_{ID2}	IDLE mode		10	13	mA
1-7		I_{RE2}	Read mode		10	13	mA
1-8		I_{WR2}	Write mode		10	13	mA
1-9	Bank write mode	I_{CCBW}	I_{CCBW}=17+17×N+I_W×N, I_W=31 mA		300		mA
Digital Inputs							
2-1	TTL input low input voltage	V_{IL}	TTL input; R/XW Pull-up resister : 100 kΩ	0		0.8	V
2-2	TTL input high input voltage	V_{IH}		2.0		V_{CC}+0.3	V
2-3	TTL input input current	I_{TTL}	High voltage : 5 V Low voltage : 0 V	–100		100	µA
2-4	Serial interface input low input voltage	V_{SIL}	Serial input; SDATA, SCLK, SDEN			1	V
2-5	Serial interface input high input voltage	V_{SIH}		4			V
2-6	Serial interface input input current	I_{ST}	High voltage : 5 V, Low voltage : 0 V Pull-down resister : 14 kΩ	–1000		1000	µA
3-1	P ECL input Voltage range	V_{WDV}	Write data input	V_{CC} –2.5		V_{CC} +0.3	V
3-2	P ECL input Input amplitude	V_{WDA}		0.3		1.5	V
3-3	P ECL input current	I_{WD}	Input voltage : 4 V	–20		20	µA
3-4	P ECL input high input voltage 2	V_{PIH}	V_{DD}=3.3 V	V_{DD}–0.2	V_{DD}		V
3-5	P ECL input low input voltage 2	V_{PIL}		2.0	V_{DD}–0.5	V_{DD}–0.3	V
3-6	P ECL input differential voltage 2	Vdiff	(V_{PIH}–V_{PIL}) × 2	400	800	1300	mV

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
4-1	Bank Write Enable voltage	V_{SEH}		V_{CC} +1.2		V_{CC} +1.4	V
4-2	Bank Write Enable current	I_{SEH}		6		14	mA
5-1	FLT output low voltage	V_{FLTL}	External resistance=2.4 kΩ			0.8	V
5-2	FLT output high voltage	V_{FLTH}	External resistance=2.4 kΩ	4.5			V
6	BHV gain accuracy	E_{BHV}	$V_{BHV}=V_{CC}-4\times I_B\times(R_{MR}+5.5\ \Omega)$ I_B="1,1,1" R_{MR}=50 Ω	–8		8	%
Read Characteristics			R_{MR}=50 Ω, I_B=6.0 mA				
R1	Low Gain	A_{VL}	[GAIN]=0 R_{MR}=50 Ω, I_B=6.0 mA	115	140	165	V/V
R2	High Gain	A_{VH}	[GAIN]=1 R_{MR}=50 Ω, I_B=6.0 mA	155	190	225	V/V
R3	Low frequency cut-off (–3 dB)	F_{CL}			350	550	kHz
R4	High frequency cut-off (–3 dB)	F_{CH}		140	200		MHz
R5	Input reflected noise	E_{NI}	Exclusive of Head noise R_{MR}=50 Ω, I_B=6.0 mA		0.77	0.95	nV/$\sqrt{\text{Hz}}$
R6	MR bias current range 1	I_{BR1}		3		8	mA
R7	MR bias accuracy	E_{IB}		–7		+7	%
R8	MR bias resolution	RIB	3 bit DAC		0.714		mA
R9-1	V_{CC} power supply rejection ratio	PSRR1	Ripple voltage : 100 mVp-p 100 kHz to 50 MHz	38			dB
R9-2	V_{EE} power supply rejection ratio	PSRR2	Ripple voltage : 100 mVp-p 100 kHz to 10 MHz	45			dB
R10-1	Common mode rejection ratio 1	CMRR1	Ripple voltage : 100 mVp-p 100 kHz to 50 MHz	37			dB
R10-2	Common mode rejection ratio 2	CMRR2	Ripple voltage : 100 mVp-p 51 MHz to 80 MHz	27			dB
R11	Control line input noise rejection	CLRR	Ripple voltage : 100 mVp-p 4 MHz to 80 MHz	40			dB
R12	RDX/RDY offset difference magnitude	V_{OFF1}	Write to Read			50	mV
R13	RDX/RDY output impedance	RDro	Differential, read mode	30		100	Ω

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Read Safety Characteristics							
P1	MR head open threshold	MRop	Head X - Head Y	600	750	900	mV
P2	MR head short threshold	MRsh	Head X - Head Y IB= '000' to '011'	15	50	90	mV
Write Characteristics							
W1	Write current range	I_{WR}	DAC code=× '0000' to × '1111'	15		45	mA
W2	Write current accuracy	E_{IW}	R_H=0 Ω	–7		+7	%
W3	Write current resolution	R_{IW}	4 bit DAC		2		mA
W4	Leakage current	I_{LEAK}	Unselected head			200	µA
W6	Damping register	R_D		320	420	520	Ω
W7	Write current propagation delay time	Tpd	L_H=0, R_H=0 Write DATA to 50 % of Write current			10	ns
W8	Write current rise/fall time	T_R/T_F	R_H=15 Ω, L_H=150 nH, I_W=31 mA		2.5		ns
W9	Erase current accuracy	E_{IE}	V_{CC}=3.5 V DAC code=× '0101'	–18	–9	0	%
Write Safety Characteristics							
U1	Write head open threshold	R_{OP}	Detect open head		1.2	1.4	V
U2	Head voltage when short to GND	V_G	Detect short to GND			0.1	V
U3	WD frequency too low	f_{WDL}		0.5		1.8	MHz
U4	Write safety detect time	T_{WS}	T1 : 2 transitions on WDX/WDY			300 +T1	ns
U5	Low V_{CC} threshold	VWthL	Fault detected	3.7	3.9	4.1	V
U6	Low V_{CC} threshold	VWthH	Fault removed	3.9	4.1	4.3	V
U7	Low V_{CC} threshold hysteresis	Vhys			200		mV

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Switching Characteristics I_W=31 mA, I_B=6 mA							
S1	Write to Read	T_{WR}	Signal on WDX/WDY 90 % RD signal or 10 % I_W		300	500	ns
S2	Read to Write	T_{RW}	90 % I^W		50	70	ns
S3	Idle to Read	T_{IR}	90 % RD signal			1.0	µs
S4-1	Sleep to Read(A3238)	T_{SR1}	90 % RD signal ,90 % IB(*1) IB="0,1,1"		600	1000	µs
S4-2	Sleep to Read(A3239)	T_{SR2}	90 % RD signal ,90 % IB(*1) IB="0,1,1"		600	2000	µs
Bank Write Characteristics I_W=31 mA, I_B=6 mA							
S5	Read to Bank Write	T_{RB}	90 % I_W			100	ns
S6	Bank Write to Read	T_{BR}	10 % I_W			100	ns
S7	Idle to Bank Write Idle to Write	T_{IW}	90 % I_W			300	us
Serial port timing							
B1	Set up time	Tsu (sden)	SDEN to first SCLK	10			ns
B2	Hold time	Th (sden)	Last SCLK to deassert SDEN	10			ns
B4	SCLK frequency	f (sclk)				30	MHz
B5	SCLK pulse width	Tw (sclk)		10			ns
B6	SCLK-SDATA set up time	Tsu (d)		10			ns
B7	SCLK-SDATA hold time	Th (d)		10			ns
B8	SDEN low time	T_{SL}		100			ns

(*1) TSR is proportional to IB and external CAP value

Serial port characteristics

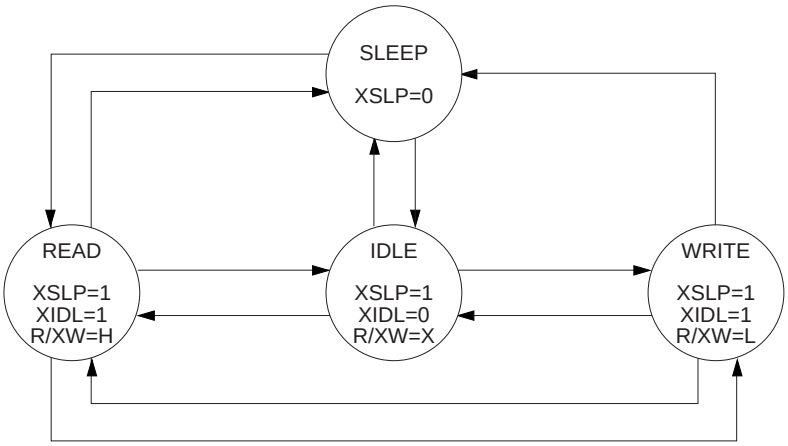
ADR1	ADR0	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
0	0	XSLP	XIDL	N/A	HS2	HS1	HS0
0	1	GAIN	BHV	N/A	IB2	IB1	IB0
1	0	MROPN	MRSHT	IW3	IW2	IW1	IW0

∗IB<2-0> bits are initialized by '0' at power on

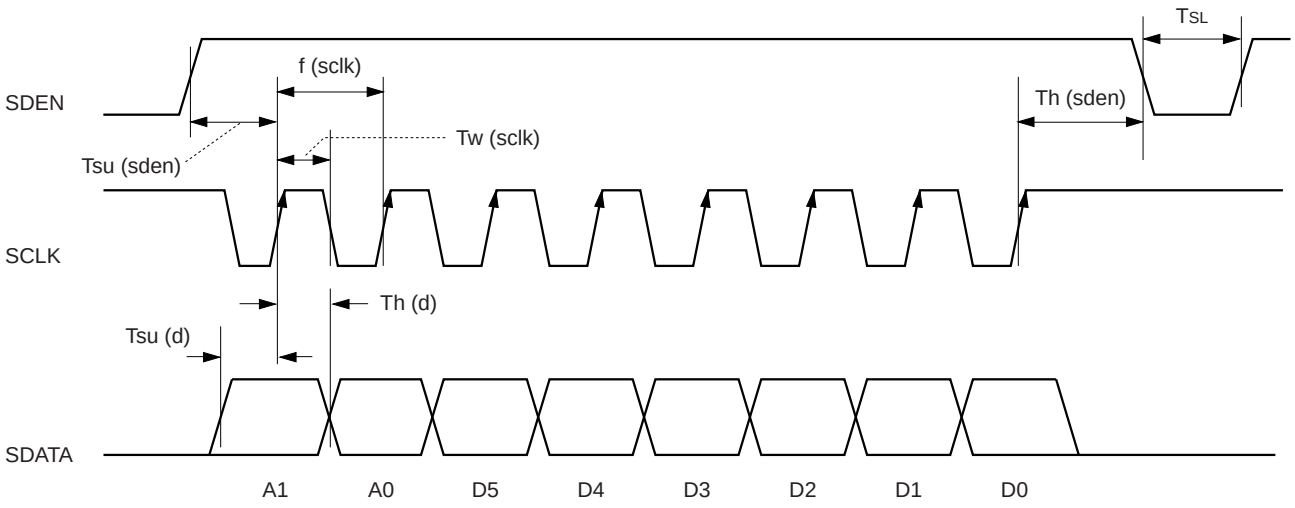
Code Description

Bit	Function
XSLP	"0" = Set the pre-amp into low power "sleep" mode
XIDL	"0" = Set preamplifier to idle mode
HS<2-0>	Head select bit
GAIN	Set the pre-amp to high or low gain mode. "1" = Set preamplifier to high gain mode
BHV	Activate the BHV test point pin. "1" active.
IB<2-0>	MR bias current set
MROPN	"1" = Set MR head open detector active.
MRSHT	"1" = Set MR head short detector active.
IW<3-0>	Set write current

Mode Control



Serial Port Timing Detail



Serial Port Timing

After the SDEN goes high, the last eight bits are transferred into the register. The SCLK will shift the data presented at the SDATA into an internal shift register on the rising edge of each clock.
As SCLK initial condition, both of Low and High signal is acceptable.

♦ Unsafe condition

1. Write fault condition

   FLT is a high level in write fault condition.

   - Open write head leads. f_{WD} < 15 MHz
   - Write head leads shorted to ground.
   - WD frequency is too low.
   - Power supply is out of tolerance.

2. Read fault condition

   FLT is a low level in read fault condition.

   - Open and short MR head. (This function is set by serial register)

♦ Bank write control (refer to 'Bank write current vs Current accuracy' characteristic curve)

1. Set the Read mode.
2. Force a certain voltage(min.V_{CC}+1.2V) to FLT/SE pin by using the pull-up resister(Rse=820Ω)

   #This operation disables all Fault detection.
3. Set V_{CC} at 3.5 V (in case of Erase mode only)
4. Start the write operation by setting R/XW = "L".
5. Terminate the write operation by setting R/XW = "H".

   i) Allow 50 % write duty or less.
   ii) Low voltage detector is disabled in Bank Write mode and Erase mode.
   iii) Don't change the serial register data bits in following conditions :
   ∗) V_{CC}=3.5 V
   ∗∗) On entering Write data

♦ BHV (Buffered Head Voltage)

1. Applicable within V_{CC}=5 V±5 %
2. Turn BHV on,but turn off MROPN and MRSHT
3. V_{BHV} is determined by basis of V_{CC}. $V_{BHV} = V_{CC} - 4 \times I_B \times (R_{MR} + 5.5\ \Omega)$

♦ Head select table

6ch

HS2	HS1	HS0	Head select, Normal operation
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	none
1	1	1	none

♦ Head select table

4ch

HS2	HS1	HS0	Head select, Normal operation
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	none
1	0	1	none
1	1	0	none
1	1	1	none

♦ MR Bias

IB2	IB1	IB0	I_B (mA)
0	0	0	3.0
0	0	1	3.714
0	1	0	4.429
0	1	1	5.143
1	0	0	5.857
1	0	1	6.571
1	1	0	7.286
1	1	1	8.0

♦ Write current

IW3	IW2	IW1	IW0	Write current (mA 0-P)
0	0	0	0	15
0	0	0	1	17
0	0	1	0	19
0	0	1	1	21
0	1	0	0	23
0	1	0	1	25
0	1	1	0	27
0	1	1	1	29
1	0	0	0	31
1	0	0	1	33
1	0	1	0	35
1	0	1	1	37
1	1	0	0	39
1	1	0	1	41
1	1	1	0	43
1	1	1	1	45

(*1) Actual head current is defined by the following equation:

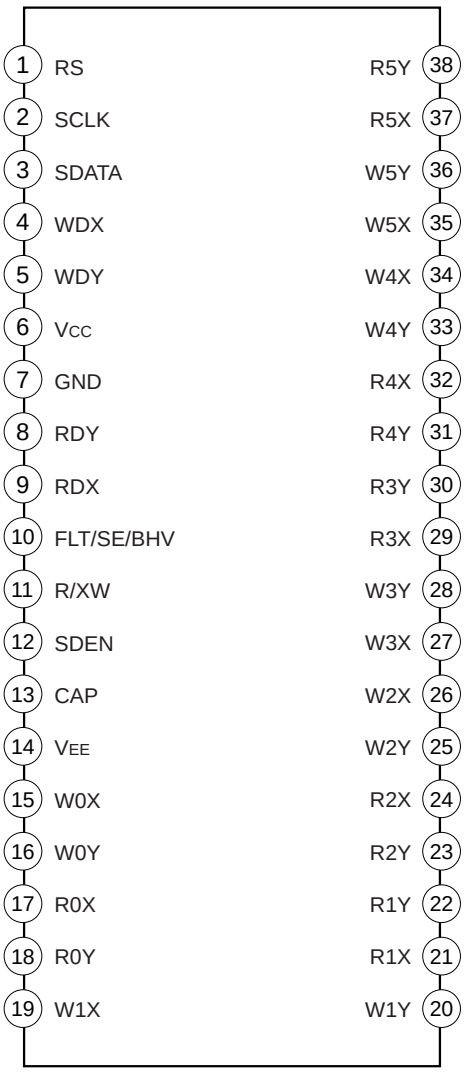
Ihead=Iw/ (I+Rh/Rd)

Rh : Head Resistance

Rd : Damping Resistance

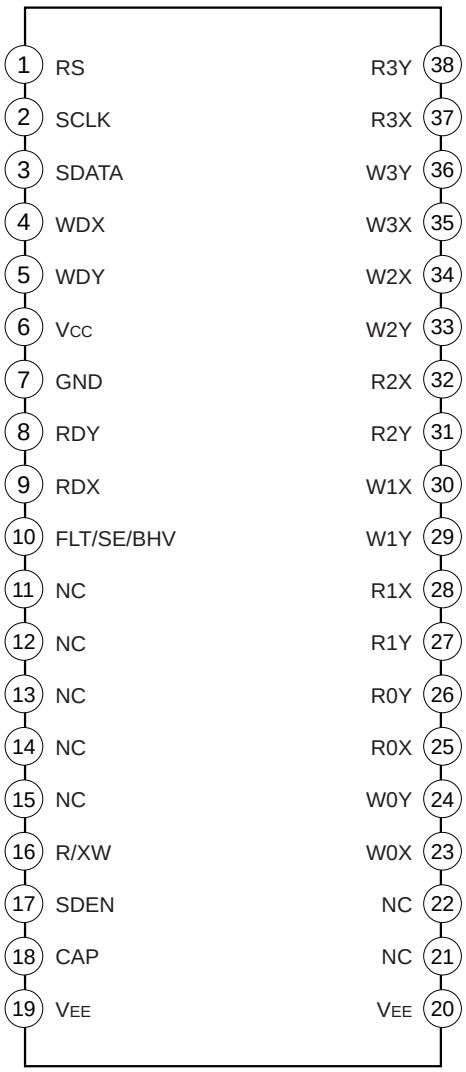
(*2) Short X-Y terminal on un-used head

♦ **6ch CXA3238TN**



TSSOP 38Pin 0.5 mm pitch
Package dimension including leads 6.4 × 9.7 mm

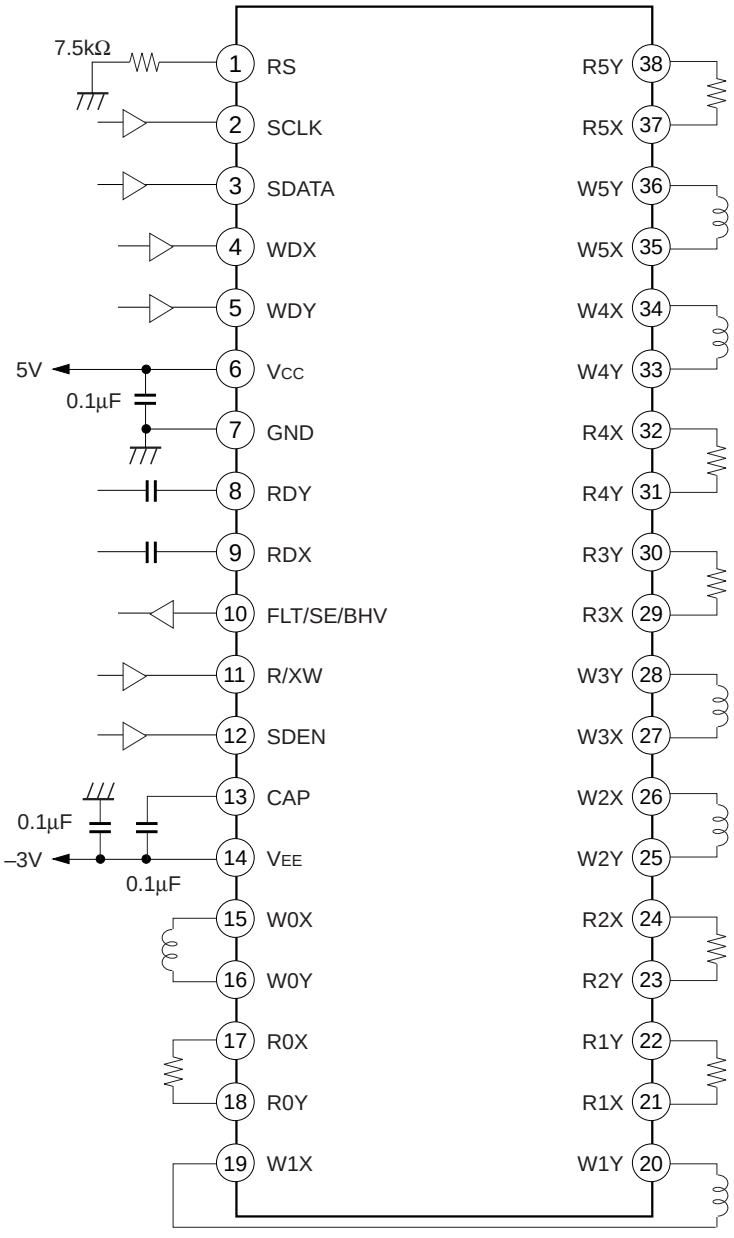
♦ **4ch CXA3239TN**



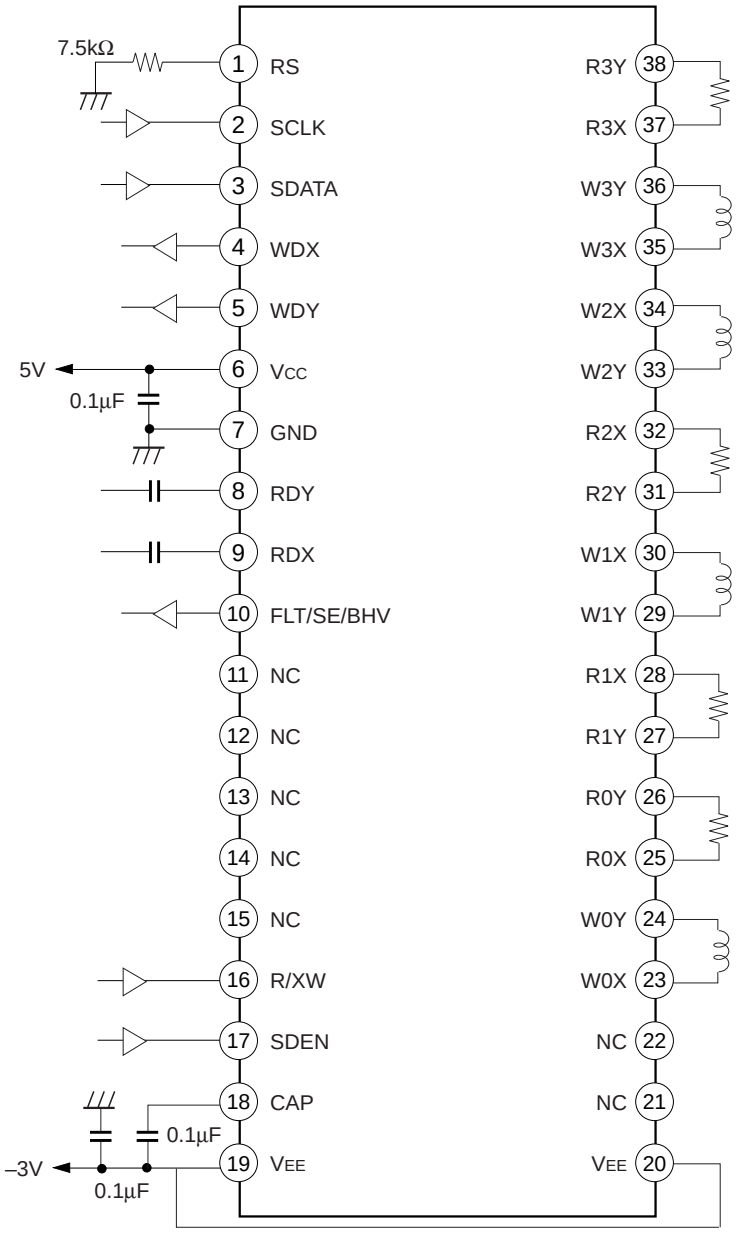
TSSOP 38Pin 0.5 mm pitch
Package dimension including leads 6.4 × 9.7 mm

Application Circuit

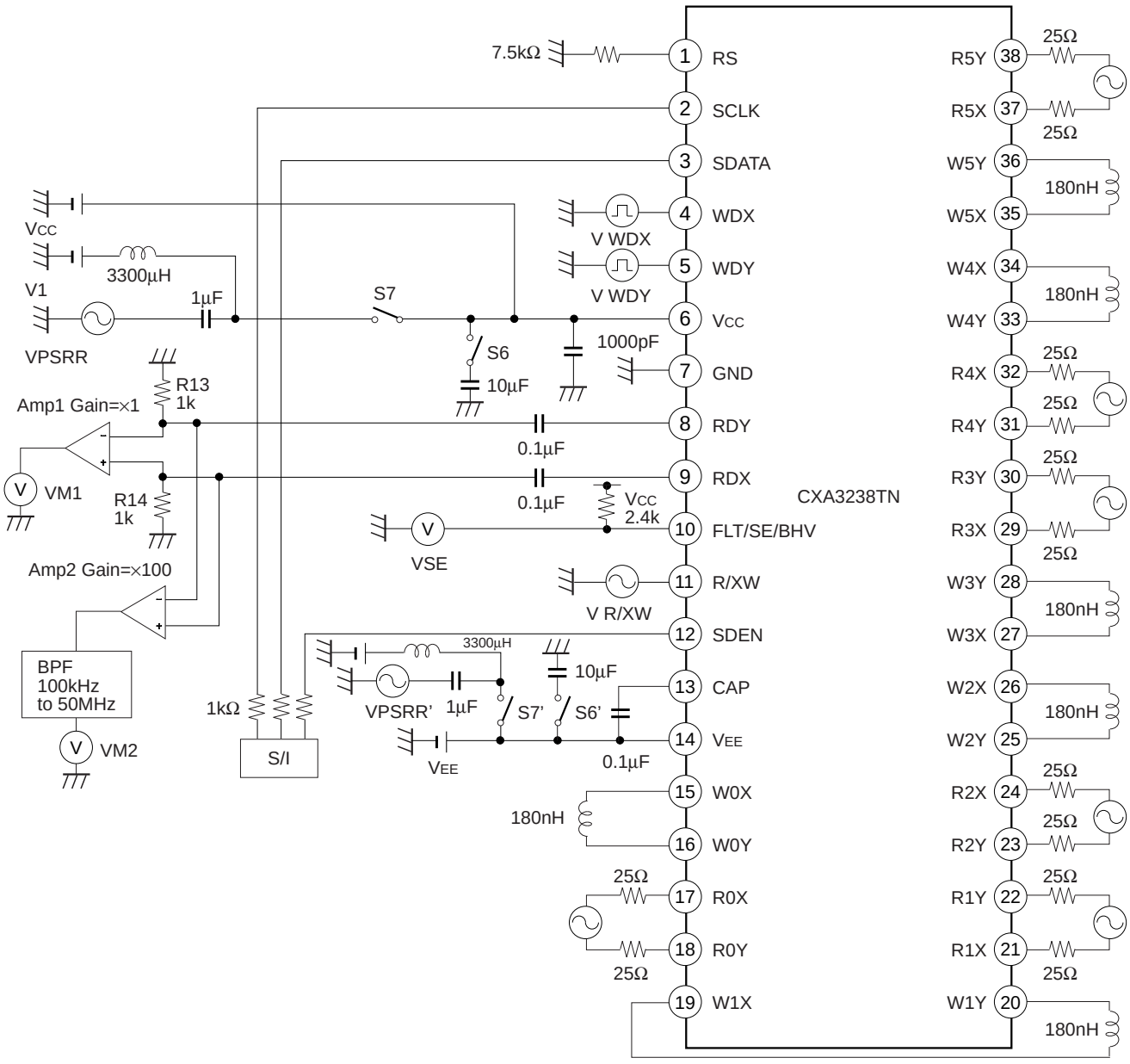
CXA3238TN

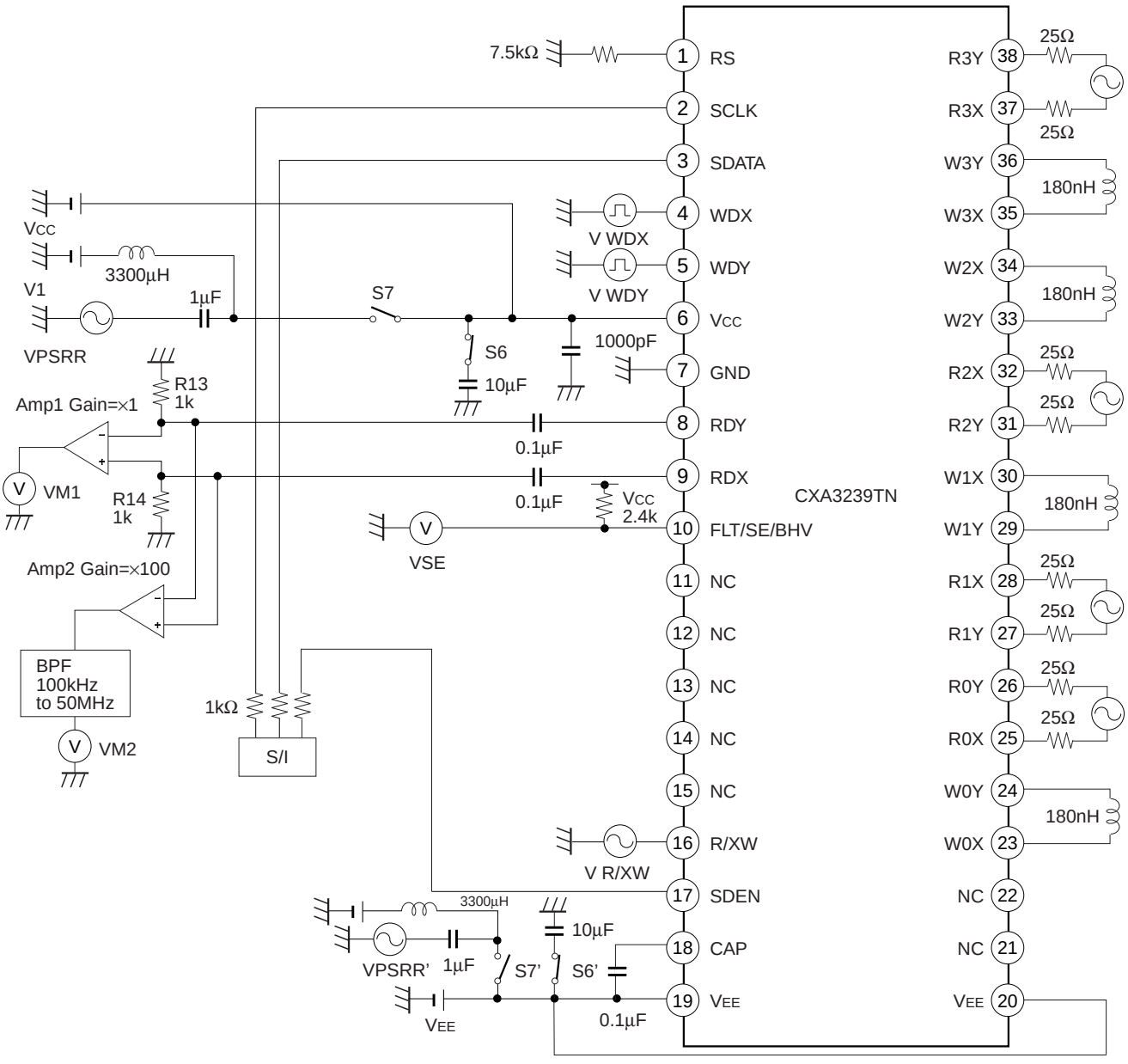


CXA3239TN

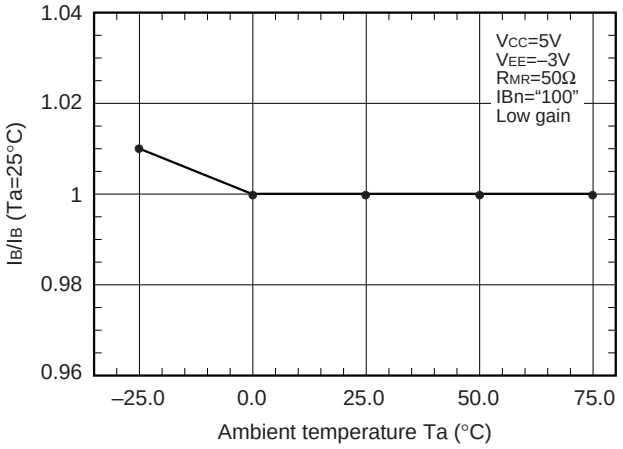

7.5kΩ
1 RS
2 SCLK
3 SDATA
4 WDX
5 WDY
5V
6 VCC
0.1µF
7 GND
8 RDY
9 RDX
10 FLT/SE/BHV
11 NC
12 NC
13 NC
14 NC
15 NC
16 R/XW
17 SDEN
18 CAP
0.1µF
–3V
19 VEE
0.1µF
R3Y 38
R3X 37
W3Y 36
W3X 35
W2X 34
W2Y 33
R2X 32
R2Y 31
W1X 30
W1Y 29
R1X 28
R1Y 27
R0Y 26
R0X 25
W0Y 24
W0X 23
NC 22
NC 21
VEE 20

Measurement Spec.Circuit

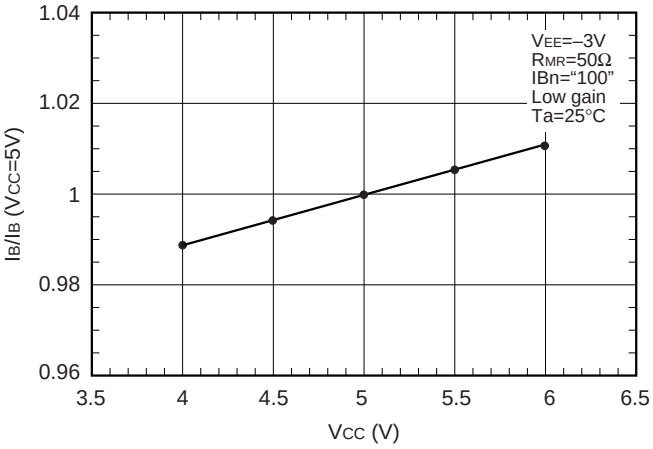



CXA3239TN
1 RS
2 SCLK
3 SDATA
4 WDX
5 WDY
6 VCC
7 GND
8 RDY
9 RDX
10 FLT/SE/BHV
11 NC
12 NC
13 NC
14 NC
15 NC
16 R/XW
17 SDEN
18 CAP
19 VEE
38 R3Y
37 R3X
36 W3Y
35 W3X
34 W2X
33 W2Y
32 R2X
31 R2Y
30 W1X
29 W1Y
28 R1X
27 R1Y
26 R0Y
25 R0X
24 W0Y
23 W0X
22 NC
21 NC
20 VEE
7.5kΩ
V WDX
V WDY
V R/XW
VCC
3300µH
V1
1µF
VPSRR
S7
S6
10µF
1000pF
R13
1k
Amp1 Gain=×1
0.1µF
VM1
R14
1k
Amp2 Gain=×100
VCC
2.4k
VSE
BPF
100kHz
to 50MHz
VM2
1kΩ
S/I
3300µH
VPSRR'
1µF
S7'
S6'
10µF
0.1µF
VEE
25Ω
180nH

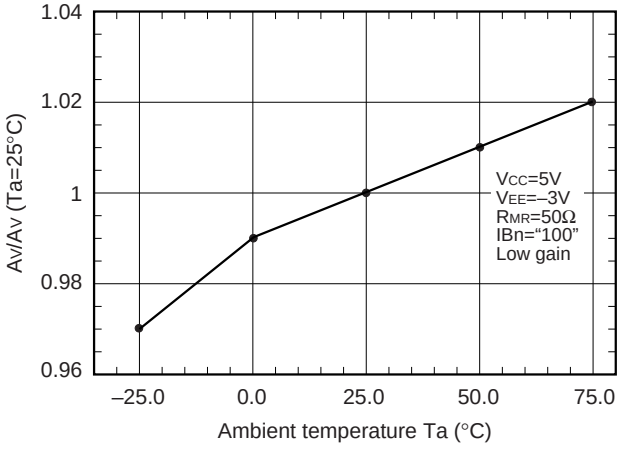
Normalized bias current vs Ambient temperature



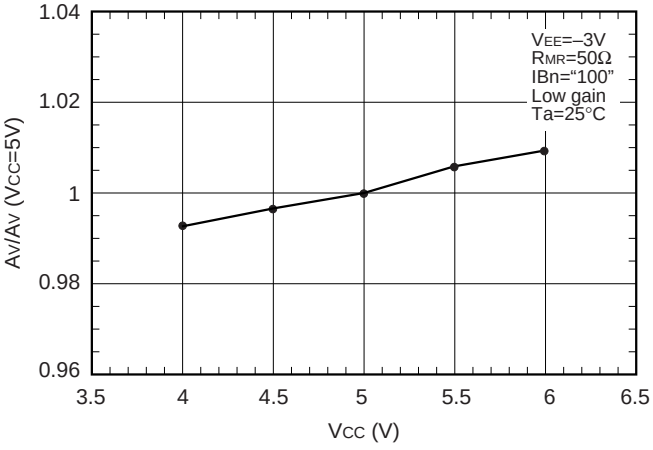
Normalized bias current vs Power supply voltage



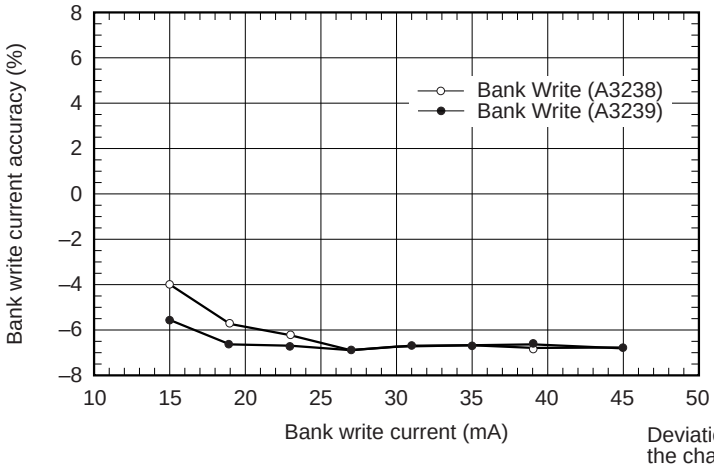
Normalized read amplifier voltage gain vs Ambient temperature



Normalized read amplifier voltage gain vs Power supply voltage



Bank write current vs Current accuracy



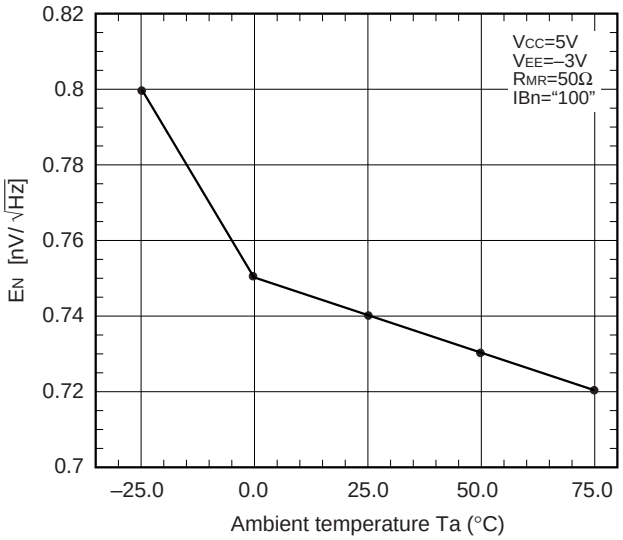
VCC=5V
Ta=25°C

RH=0Ω

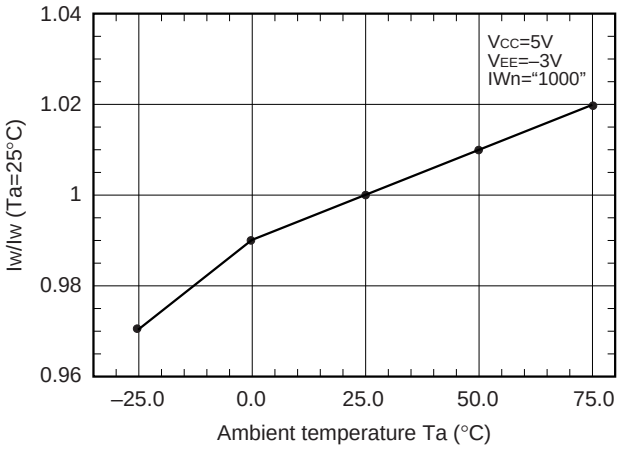
Read 170µs
Write 30µs

Deviation of Bank write current is within ±7% at basis of the chart

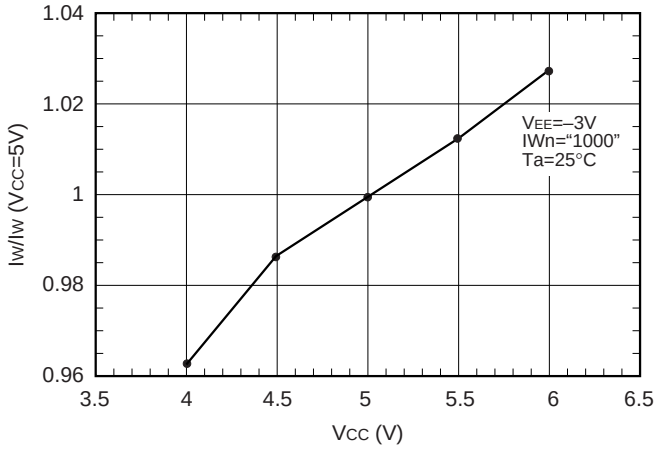
Input refered noise voltage vs Ambient temperature



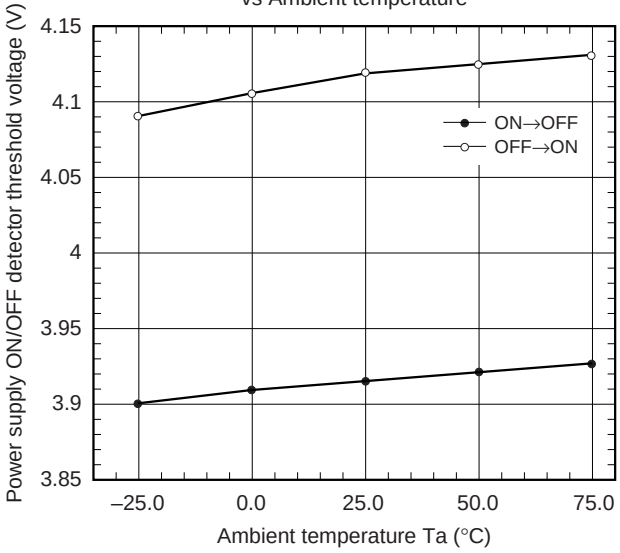
Normalized write current vs Ambient temperature



Normalized write current vs Power supply voltage

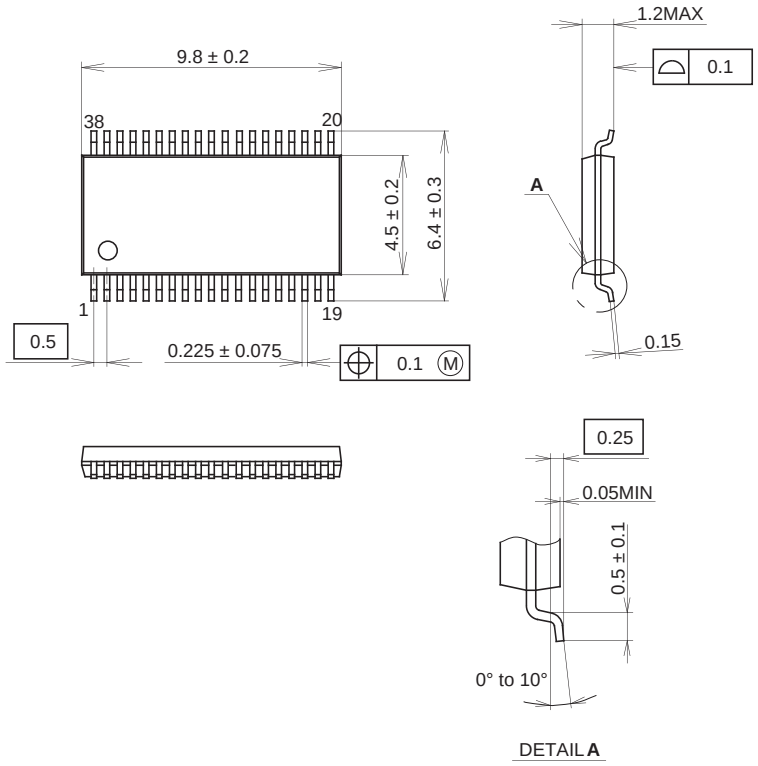


Power supply ON/OFF detector threshold voltage vs Ambient temperature



Package Outline Unit : mm

38PIN TSSOP(PLASTIC)



SONY CODE	TSSOP-38P-L121
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g