SONY

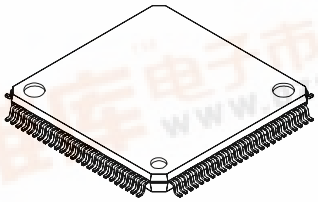
CXA3562AR

LCD Driver

Description

The CXA3562AR is a driver IC developed for use with Sony polycrystalline silicon TFT LCD panels. It supports digital 2-parallel and single input, and the input data is analog demultiplexed into 12 phases and output. The CXA3562AR can directly drive an LCD panel, and the VCOM setting circuit and precharge pulse waveform generator are also on-chip.

100 pin LQFP (Plastic)



Features

- Supports 10-bit 2-parallel and single input
- Supports signals up to UXGA
  (1/2 clock when using UXGA signals)
- Low output deviation by on-chip output offset cancel circuit
- Supports both line inversion and dot and line inversion
- On-chip timing generator with ECL
- VCOM voltage generation circuit
- Precharge pulse waveform generation circuit

Applications

LCD projectors and other video equipment

Absolute Maximum Ratings (V_{SS} = 0V)

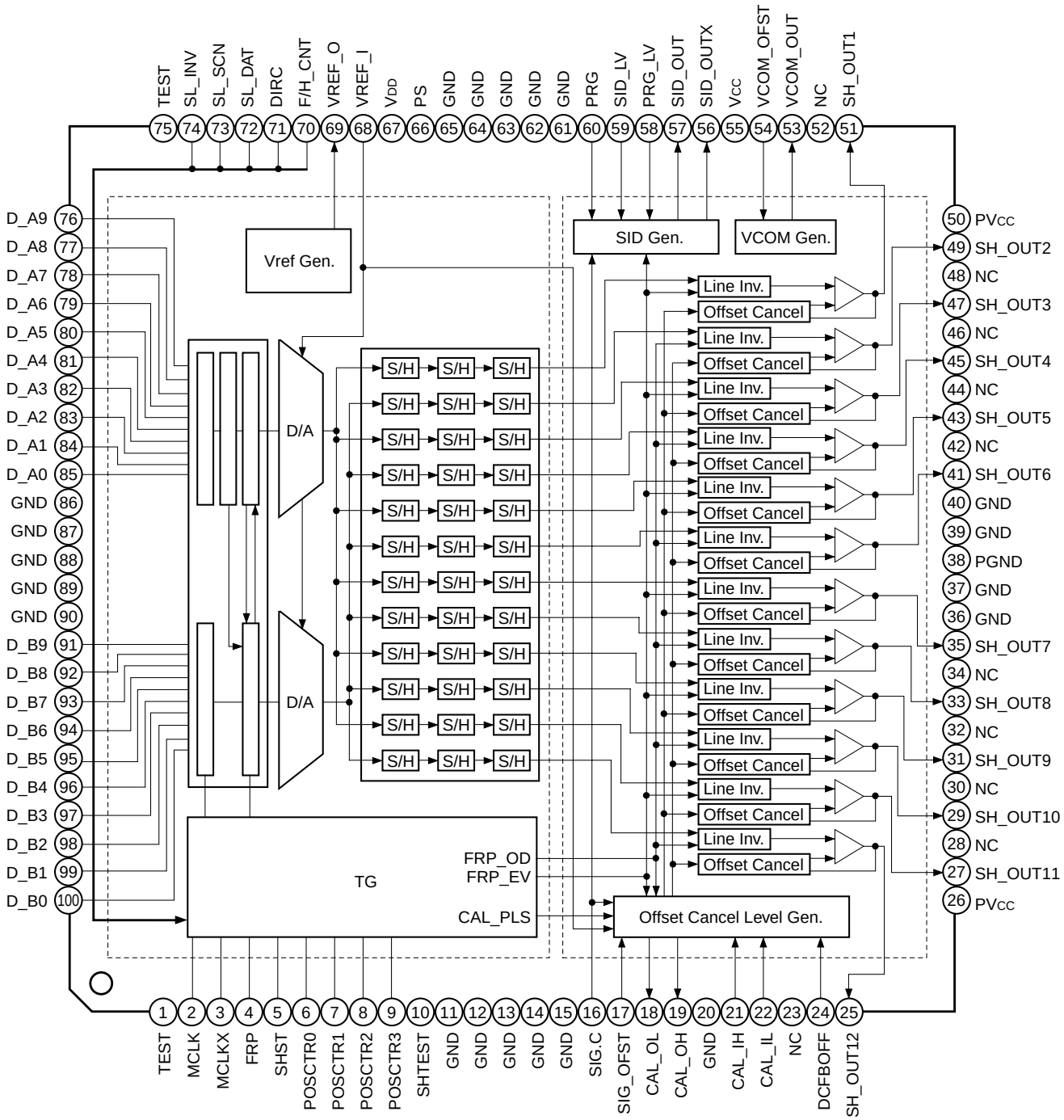
• Supply voltage	V_{CC}	16	V
	V_{DD}	5.5	V
• Operating temperature	Topr	–20 to +70	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	2000	mW

Recommended Operating Conditions

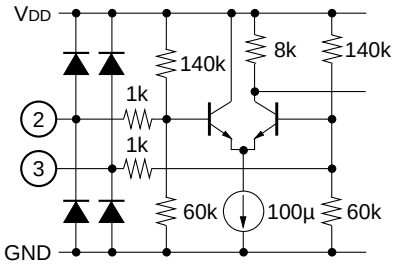
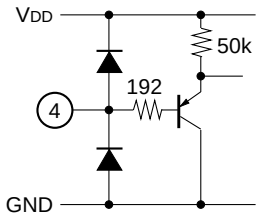
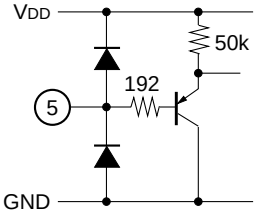
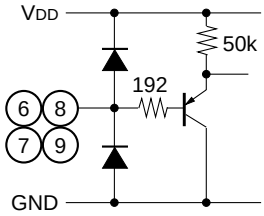
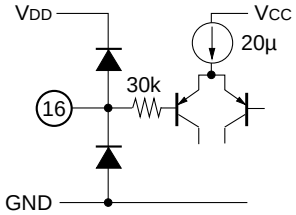
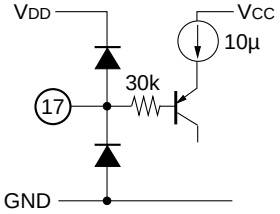
• Supply voltage	V_{CC}	15.0 to 15.5	V
	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	–20 to +70	°C

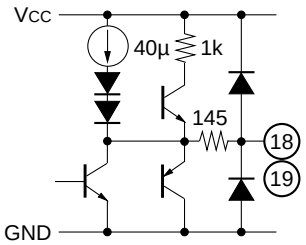
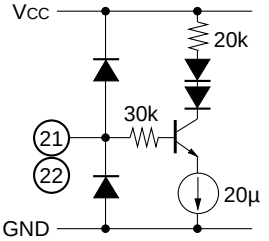
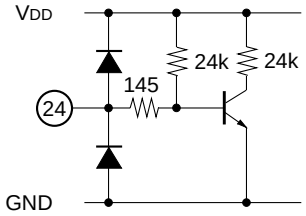
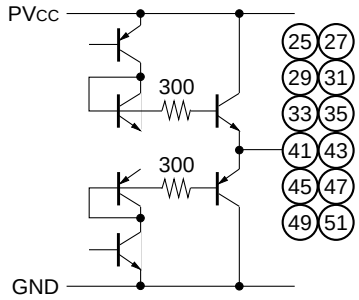
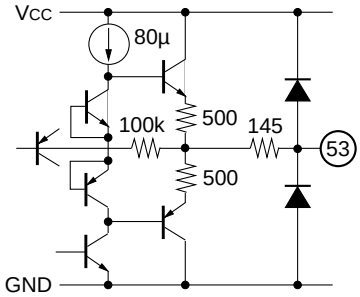
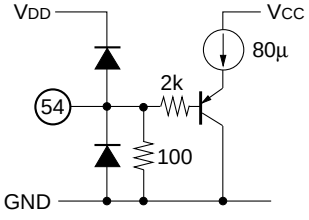
E01820A22

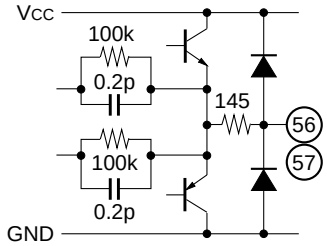
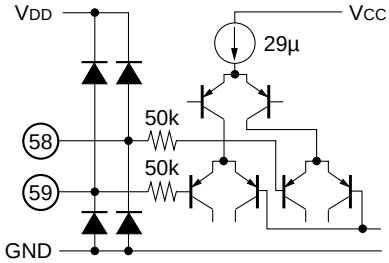
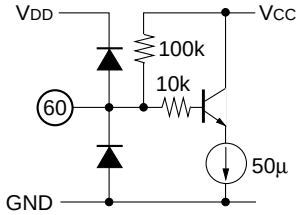
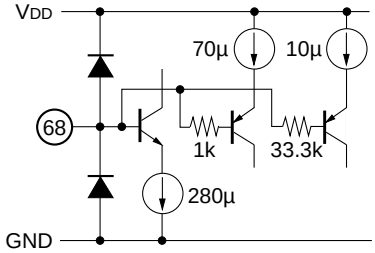
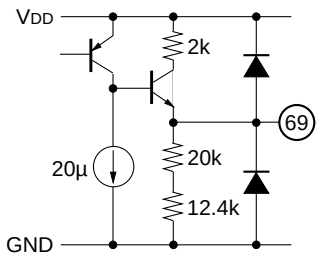
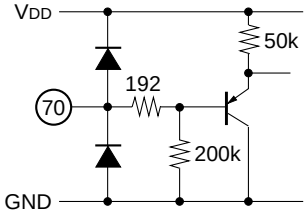
Block Diagram and Pin Configuration

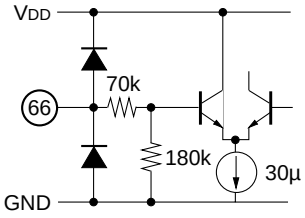
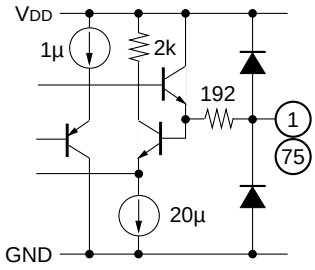
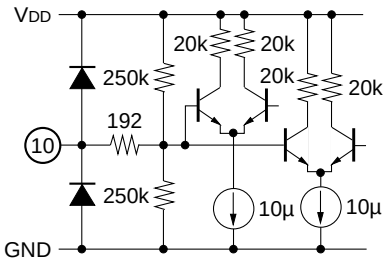
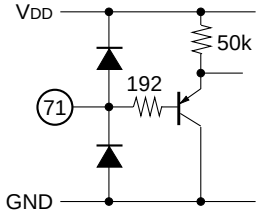


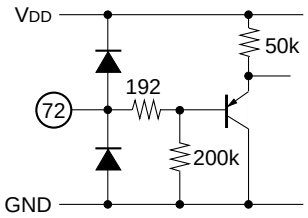
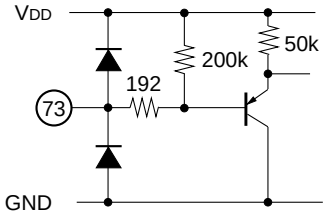
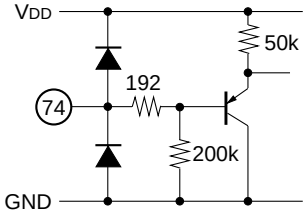
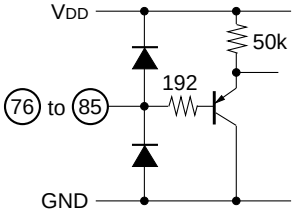
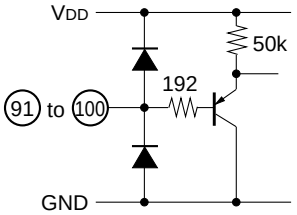
Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
2 3	MCLK MCLKX	I	PECL differential (amplitude 0.4V or more between V_{DD} to 2V) or TTL input		Dot clock input. PECL differential input or TTL input. For TTL input, input to MCLK and connect MCLKX to GND through a capacitor.
4	FRP	I	High: ≥2.0V Low: ≤0.8V		LCD panel AC drive inversion timing input. High: inverted Low: non-inverted See the Timing Chart.
5	SHST	I	High: ≥2.0V Low: ≤0.8V		Internal sample-and-hold timing circuit reset pulse input. This pin is also used as the offset cancel level insertion timing input. A reset is applied to the internal timing generator at the falling edge.
6 7 8 9	POSCTR0 POSCTR1 POSCTR2 POSCTR3	I	High: ≥2.0V Low: ≤0.8V		Output phase adjustment. The output phase is adjusted in MCLK period units when SL_DAT (Pin 72) is high, and in 1/2 MCLK period units when SL_DAT is low.
16	SIG.C	I	1 to 5.0V		Signal center voltage (inversion folded voltage) adjustment input. The SH_OUT output center voltage can be adjusted in the range from 7.0 to 8.0V.
17	SIG_OFST	I	0 to 5.0V		Output signal offset adjustment from signal center voltage. The SH_OUT output 100% white level (at 3FF input) voltage can be adjusted in the range from 0 to 1V from the center voltage.

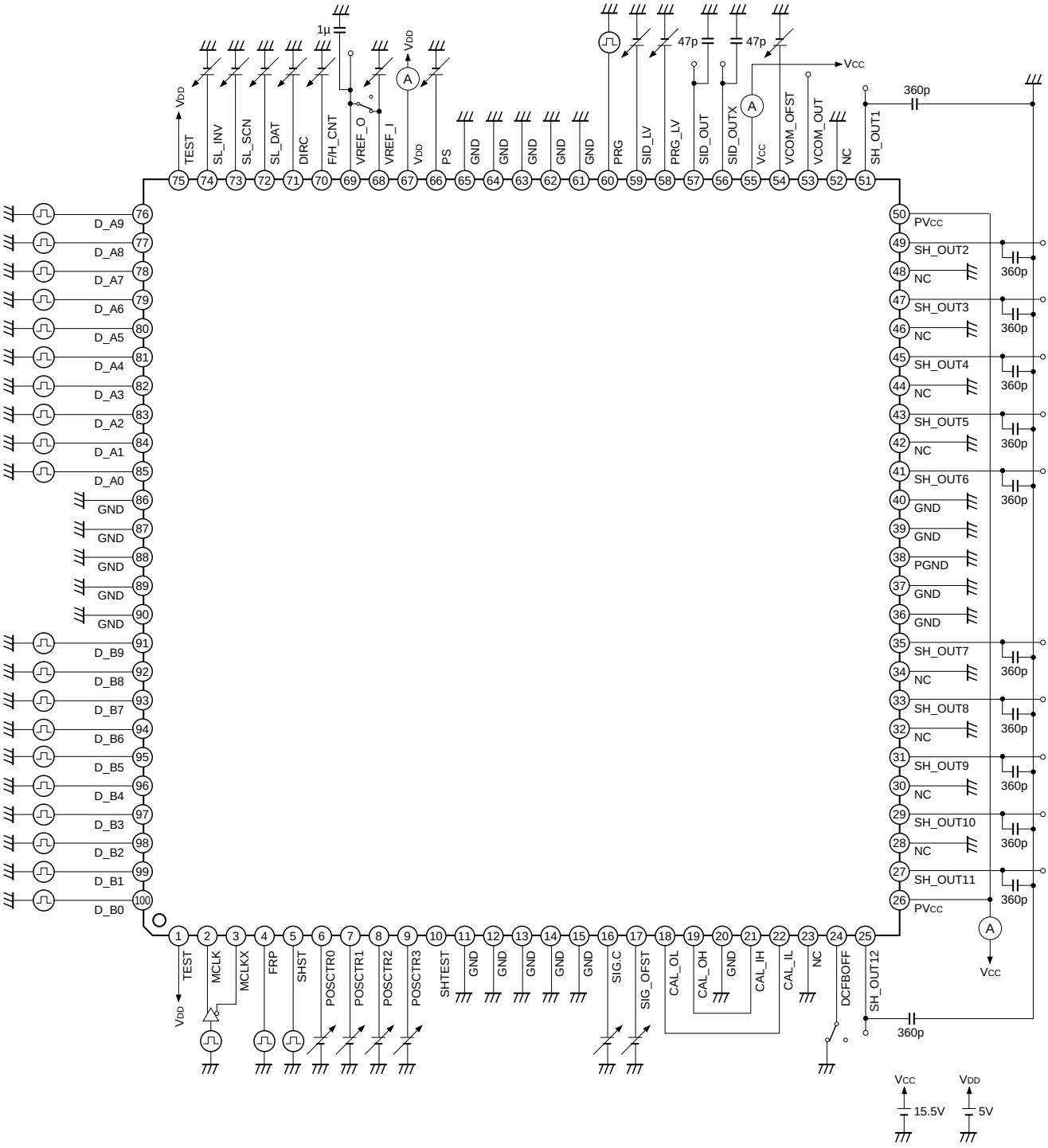
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
18 19	CAL_OL CAL_OH	O	3.0 to 6.0V 9.0 to 12.0V		Level output for canceling the offset between channels. Connect directly to CAL_IL and CAL_IH, respectively.
21 22	CAL_IH CAL_IL	O	9.0 to 12.0V 3.0 to 6.0V		Level input for canceling the offset between channels. Connect directly to CAL_OL and CAL_OH, respectively. When using two CXA3562R, connect the CAL_IL and CAL_IH of both chips to the CAL_OL and CAL_OH of only one CXA3562R.
24	DCFBOFF	I	GND		Offset cancel function off. Normally connect to GND to use with the offset cancel function on. High (offset cancel function off) when open.
25, 27, 29, 31, 33, 35, 41, 43, 45, 47, 49, 51	SH_OUT12 to SH_OUT1	O	1.5 to 13.5V		Demultiplexed output of AC inverse driven video signals. Can be connected directly to the LCD panel.
53	VCOM_OUT	O	5.0 to 8.0V		LCD panel common voltage output. Can be set in the range from the SH_OUT center potential Vsig.c to Vsig.c – 2V by VCOM_OFST.
54	VCOM_OFST	I	0 to 5.0V		LCD panel common voltage adjustment. VCOM_OUT can be set in the range from the SH_OUT center potential Vsig.c to Vsig.c – 2V by inputting 0 to 5V.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
56 57	SID_OUTX SID_OUT	O	1.5 to 13.5V		Precharge waveform output. SID_OUTX outputs the inverse of SID_OUT based on the output center voltage. These pins cannot directly drive the LCD panel, so input to the LCD panel with an external a buffer.
58 59	PRG_LV SID_LV	I	1.0 to 5.0V		Precharge level setting. Adjusts the SID_OUT and SID_OUTX output potential. PRG_LV is reflected when the PRG input pin (Pin 60) is high, and SID_LV is reflected when PRG is low.
60	PRG	I	High: ≥2.0V Low: ≤0.8V		Timing pulse input for switching the Pins 56 and 57 output levels. (See PRG_LV (Pin 58) and SID_LV (Pin 59).)
68	VREF_I	I	3.2V		Internal D/A converter reference voltage input. Normally connect directly to VREF_O.
69	VREF_O	O	3.2V		Reference voltage output. Normally connect directly to VREF_I, and connect to GND through a 0.5 to 1.0µF capacitor.
70	F/H_CNT	I	High: ≥2.0V Low: ≤0.8V Open: Low		SH_OUT output timing selection. High: SH_OUT1 to SH_OUT6 and SH_OUT7 to SH_OUT12 are output at different timing. Low: SH_OUT1 to SH_OUT12 are output at the same timing.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
66	PS	I	5V		Test. Normally connect to VDD.
38	PGND		GND		Power GND.
26, 50	PVCC		15.5V		Power VCC.
55	VCC		15.5V		15V power supply.
67	VDD		5V		5V power supply.
11 to 15, 20, 36, 37, 39, 40, 61 to 65, 86 to 90	GND		GND		GND.
23, 28, 30, 32, 34, 42, 44, 46, 48, 52	NC				
1, 75	TEST	O	1.7 to 3.2V		DAC output monitor test. Normally connect to VDD.
10	SHTEST	I	2.5V		Test. Leave open.
71	DIRC	I	High: ≥2.0V Low: ≤0.8V		Scan direction setting. High: output as a time series in ascending order of output pin symbol (in order from SH_OUT1 to SH_OUT12) Low: output in descending order

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
72	SL_DAT	I	High: ≥2.0V Low: ≤0.8V Open: Low		Digital input mode switch setting. High: single input from the A port Low: parallel input from both the A and B ports
73	SL_SCN	I	High: ≥2.0V Low: ≤0.8V Open: High		A and B port input switching interlocked/non-interlocked setting relative to scan direction setting during parallel input. High: A and B port switching interlocked to DIRC Low: fixed regardless of DIRC
74	SL_INV	I	High: ≥2.0V Low: ≤0.8V Open: Low		SH_OUT odd-numbered and even-numbered output polarity inverted/non-inverted setting. High: odd-numbered and even-numbered outputs inverted Low: non-inverted
76 to 85	D_A9 to D_A0	I	High: ≥2.0V Low: ≤0.8V		A port digital data input.
91 to 100	D_B9 to D_B0	I	High: ≥2.0V Low: ≤0.8V		B port digital data input.

Electrical Characteristics Measurement Circuit



Electrical Characteristics

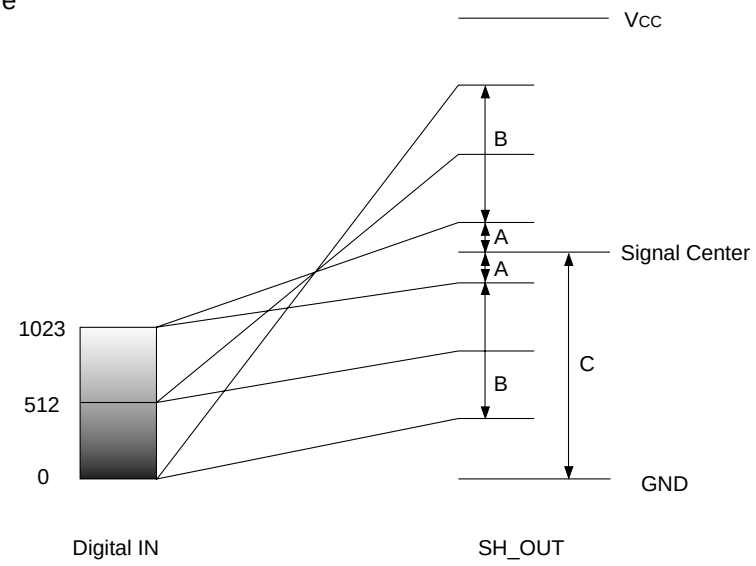
No.	Item	Symbol	Measurement points	Measurement conditions	Min.	Typ.	Max.	Unit
1	Digital input resolution	n			—	10	—	bit
2	Digital input setup time	T_S		SHST, D_A[9:0] and D_B[9:0] minimum setup time relative to MCLK input. (PELL)	2	—	—	ns
3	Digital input hold time	T_H		SHST, D_A[9:0] and D_B[9:0] minimum hold time relative to MCLK input. (PECL)	3	—	—	ns
4	MCLK input frequency range 1	f_{MCLK1}		SL_DAT: 5V; maximum frequency at which the internal timing generator and D/A converter operate normally.	30	—	80	MHz
5	MCLK input frequency range 2	f_{MCLK2}		SL_DAT: 0V; maximum frequency at which the internal timing generator and D/A converter operate normally.	60	—	100	MHz
6	VREF_O output voltage range	V_{VREF_O}		Measure the VREF_O (Pin 69) voltage.	3.10	3.20	3.32	V
7	SH_OUT amplitude 1	$V_{SHOUT1p-p}$	V_{OUT1}	Measure the SH_OUT1 voltage difference at D_A[9:0]: 000h and 3FFh.	4.44	4.50	4.83	V
8	SH_OUT amplitude 2	$V_{SHOUT2p-p}$	V_{OUT2}	Measure the SH_OUT2 voltage difference at D_B[9:0]: 000h and 3FFh.	4.44	4.50	4.83	V
9	SH_OUT minimum amplitude	$V_{OUTMINp-p}$	V_{OUT1}	Lower the VREF_I voltage and adjust the amplitude; minimum amplitude at which SH_OUT1 can be output at D_B[9:0]: 000h and 3FFh.	4	—	—	V
10	SH_OUT slew rate	SR_{OUT}	V_{OUT1} to V_{OUT12}	Load capacitance = 360pF; measure slew rate at 10 to 90% of output waveform rise and fall when D_A[9:0] is varied from 000h to 3FFh and from 3FFh to 000h.	160	300	—	V/µs
11	SH_OUT minimum output voltage	V_{MIN}	V_{OUT1} to V_{OUT12}	Minimum voltage at which sample-and-hold outputs V_{OUT1} to V_{OUT12} can be output.	1.5	—	—	V
12	SH_OUT maximum output voltage	V_{MAX}	V_{OUT1} to V_{OUT12}	Maximum voltage at which sample-and-hold outputs V_{OUT1} to V_{OUT12} can be output.	—	—	13.6	V
13	Output deviation between channels 1	D_{OUT1}	V_{OUT1} to V_{OUT12}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT12} value from maximum V_{OUT1} to V_{OUT12} value at D_A[9:0]: 200h and D_B[9:0]: 200h.	—	3	10	mVp-p
14	Output deviation between channels 2	D_{OUT2}	V_{OUT1} to V_{OUT12}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT12} value from maximum V_{OUT1} to V_{OUT12} value at D_A[9:0]: 000h or 3FFh and D_B[9:0]: 000h or 3FFh.	—	10	40	mVp-p
15	Output deviation between ICs 1	D_{IC1}	V_{OUT1} to V_{OUT12}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT12} value from maximum V_{OUT1} to V_{OUT12} value at D_A[9:0]: 200h and D_B[9:0]: 200h. (when using two CXA3562R)	—	10	—	mVp-p

No.	Item	Symbol	Measurement points	Measurement conditions	Min.	Typ.	Max.	Unit
16	Output deviation between ICs 2	D_{IC2}	V_{OUT1} to V_{OUT12}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT12} value from maximum V_{OUT1} to V_{OUT12} value at D_A[9:0]: 000h or 3FFh and D_B[9:0]: 000h or 3FFh. (when using two CXA3562R)	—	20	—	mVp-p
17	SID output gain 1	A_{SID1}	V_{SID_LV} V_{SID} V_{SIDX}	PRG: 0V; measure V_{SID_LV} and V_{SID} at FRP: 0V, and V_{SID_LV} and V_{SIDX} at FRP: 5V. Calculate as $A_{SID1} = V_{SID(X)}/V_{SID\_LV}$.	1.9	2.0	2.1	times
18	SID output gain 2	A_{SID2}	V_{PRG_LV} V_{SID} V_{SIDX}	PRG: 5V; measure V_{PRG_LV} and V_{SID} at FRP: 0V, and V_{PRG_LV} and V_{SIDX} at FRP: 5V. Calculate as $A_{SID2} = V_{SID(X)}/V_{PRG\_LV}$.	1.9	2.0	2.1	times
19	SID output slew rate	SR_{SID}	V_{SID} V_{SIDX}	Load capacitance = 47pF, PRG: 0V; input a repeating high/low pulse to FRP (Pin 4), and apply DC input voltage so that V_{SID} and V_{SIDX} are 2.5V/11.5V. Measure slew rate at 10 to 90% of output waveform rise and fall.	15	50	—	V/µs
20	Signal center adjustable range	V_{SIG}	V_{OUT1}	V_{OUT1} center voltage when SIG.C (Pin 16) is varied from 1 to 5V.	7	—	8	V
21	SH_OUT offset adjustable range	$V_{SIGOFST}$	V_{OUT1}	D_A[9:0]: 3FFh, FRP: 0V, D_B[9:0]: 3FFh; value obtained by subtracting V_{OUT1} from V_{OUT1} center voltage when SIG_OFST (Pin 17) is varied from 1 to 5V.	0	—	1	V
22	VCOM adjustable range	V_{COM}	V_{COM}	VCOM_OUT voltage when VCOM_OFST (Pin 54) is varied from 0 to 5V.	Vc – 2.5	—	Vc	V
23	V_{DD} current consumption	I_{DD}	I_{VDD}	$I_{DD} = I_{VDD}$	59	85	112	mA
24	V_{CC} current consumption	I_{CC}	I_{VCC1} I_{VCC2}	$I_{CC} = I_{VCC1} + I_{VCC2}$ (no digital data input)	21	40	59	mA
25	Current consumption in power saving mode	I_{PS}	I_{VDD} I_{VCC1} I_{VCC2}	GND (Pin 66), $I_{CC} = I_{VDD} + I_{VCC1} + I_{VCC2}$	31	47	65	mA
26	Differential linearity error	DLE	—	V_{VREF_I} = 3.2V	–0.7	—	0.7	LSB
27	Integral linearity error	ILE	—	V_{VREF_I} = 3.2V	–1.2	—	1.2	LSB

Description of Operation

The flow of internal operations is described below.
The digital signals input to D_A9 to D_A0 and D_B9 to D_B0 are internally D/A converted into approximately 1.5V (at VREF_I: 3.2V) analog signals. After that, the signal that has been demultiplexed into 12 phases is amplified by a factor of three times, inverted at the signal center potential according to FRP, and output.
The output level relative to the digital input changes according to the following settings.

A: SIG_OFST voltage
B: VREF_I voltage
C: SIG.C voltage



1. Digital input block

The CXA3562AR can be set to single input from only the A port or parallel input from both the A and B ports, and port switching by right/left inversion is also possible in parallel input mode. This makes it possible to support various systems.
In single input mode, the signal is internally demultiplexed to 2-parallel format and input to the D/A converter.

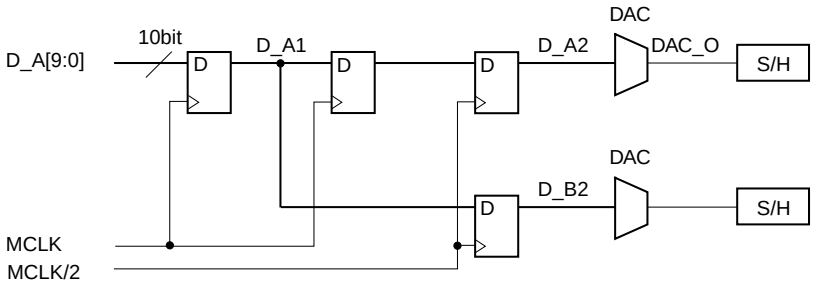
2. D/A converter block

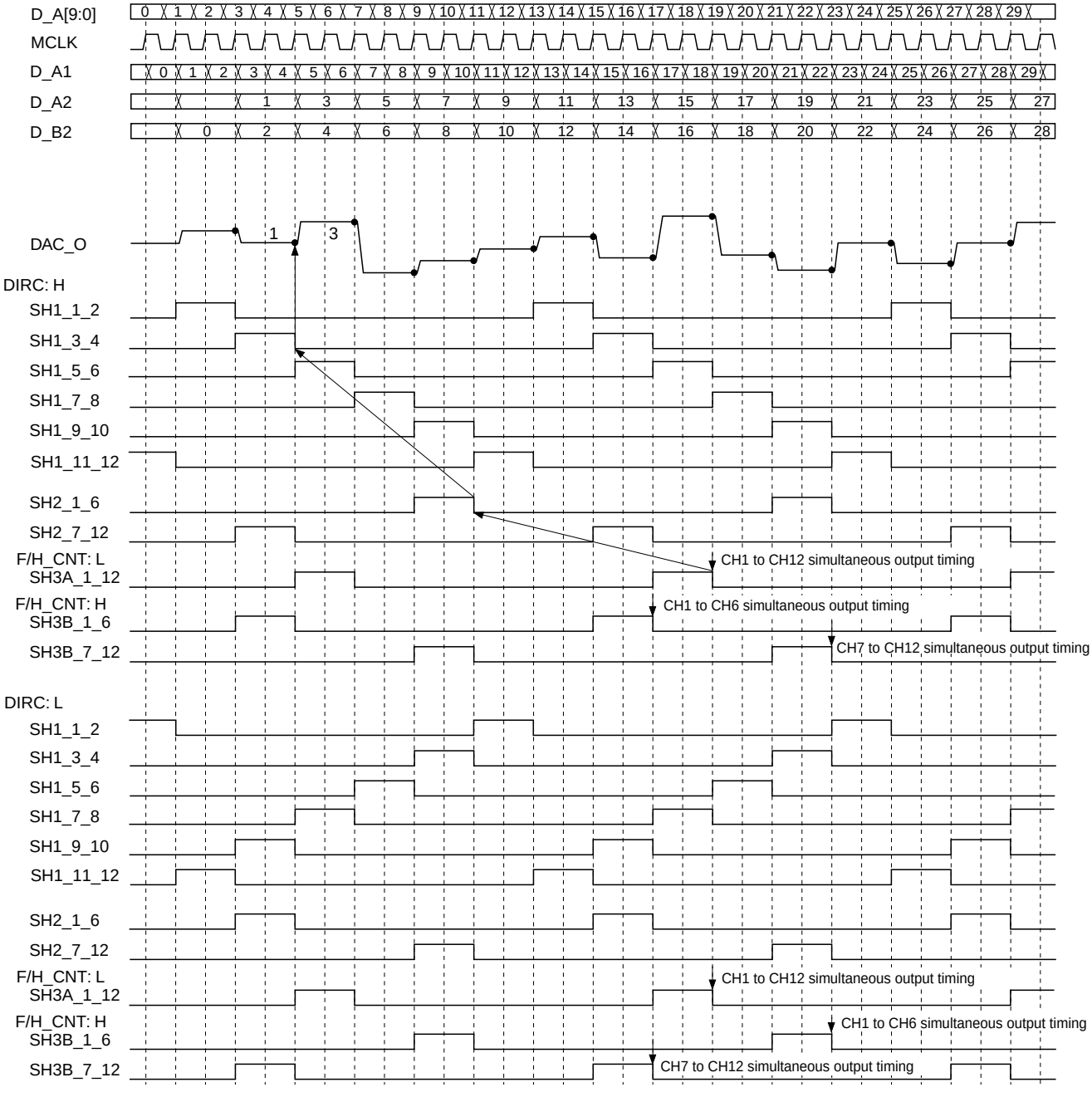
The internal D/A converter has two systems for odd-numbered and even-numbered outputs. The voltage input from VREF_I becomes the 100% white level potential of the analog converted signal, and this amplitude is a maximum 1.5Vp-p with respect to input data of 000h to 3FFh.

3. Sample-and-hold (S/H) block

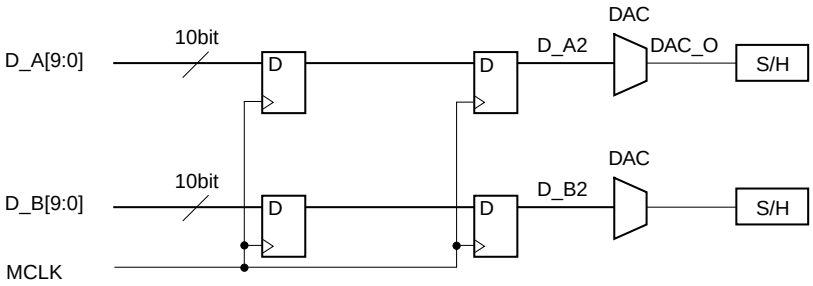
The odd-numbered and even-numbered D/A converter outputs are input to the odd-numbered and even-numbered sample-and-hold blocks, respectively. The signals are converted from time series signals into 6-phase cyclic parallel signals by the sample-and-hold group which is appropriately controlled by the internal timing generator. For forward scan, the signals are output in the ascending order of SH_OUT1, SH_OUT2, SH_OUT3 ... SH_OUT12. For reverse scan, this order is inverted and the signals are output in descending order. Connect the signals to the LCD panel according to the order used. The timing of each sample-and-hold pulse is shown on the following pages. These pulses are not output and are used only inside the IC.

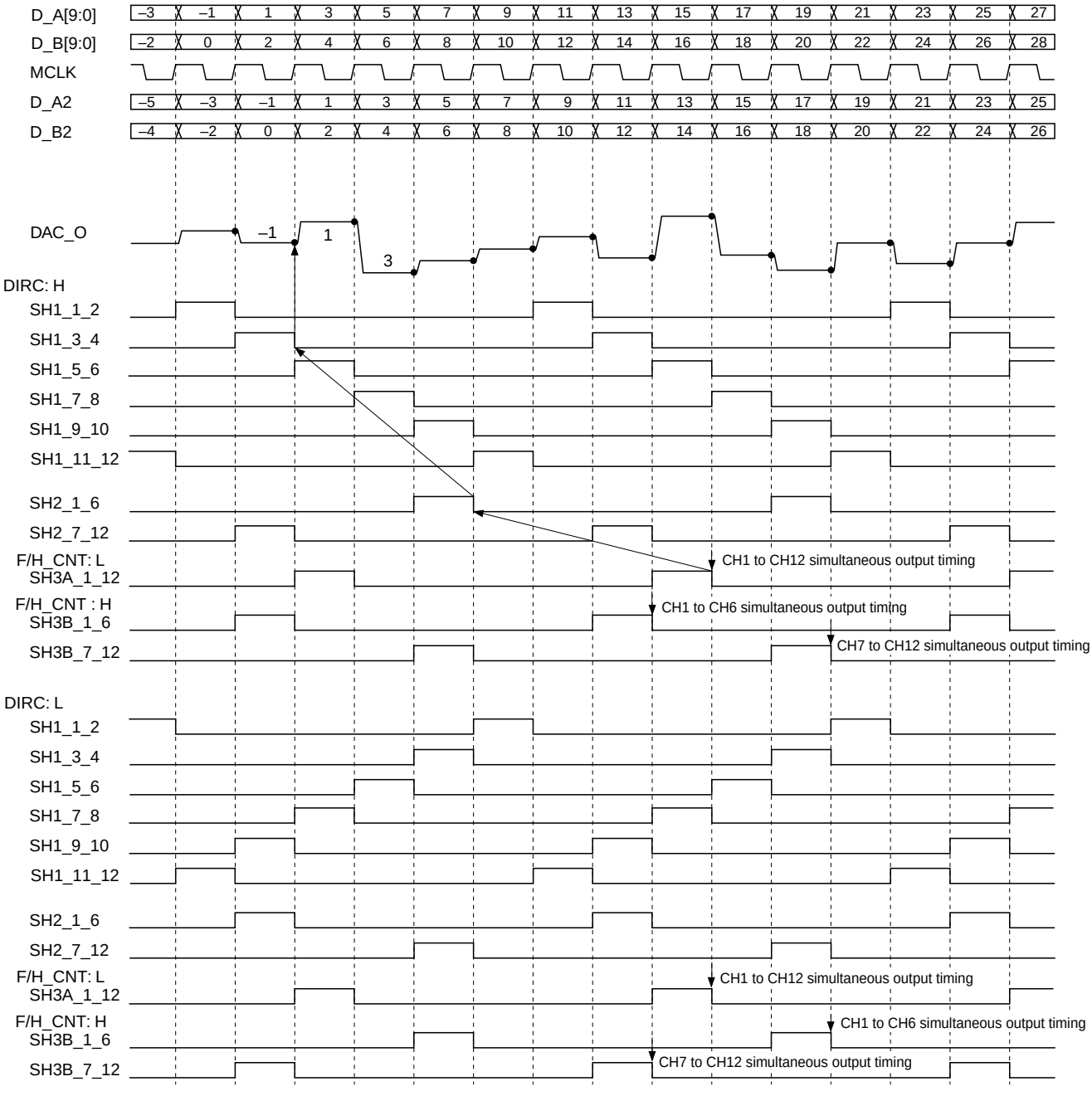
Single input mode





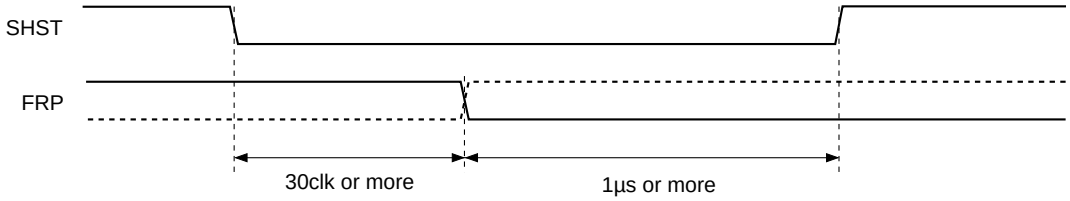
2-parallel input mode





4. Timing generator (TG) block

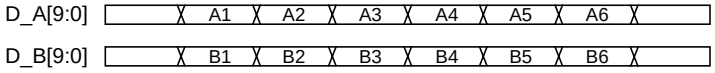
The internal timing generator operates by one pair of differential clock inputs (MCLK, MCLKX) and a horizontal sync signal input (SHST), and generates the timing pulses needed by the demultiplexer block, dot inversion control pulse and output deviation cancel circuit. The various operating modes can be designated by the pin settings.
The SHST and FRP inputs should satisfy the relationship shown in the figure below with the MCLK and MCLKX input period as 1clk.



The CXA3562AR can select various operating modes according to the timing generator block settings. These settings are described below.

• SL_DAT (Pin 72)
Digital input selection. Single input from only the A port is selected when set to high level, and parallel input from both the A and B ports is selected when set to low level. When inputting a 2-parallel processed digital video signal in parallel input mode, input the earlier time series data to the A port and the later time series data to the B port. Input a master clock having the same period as the input data rate to MCLK in both modes.
This pin is low level (2-parallel input mode) when left open.

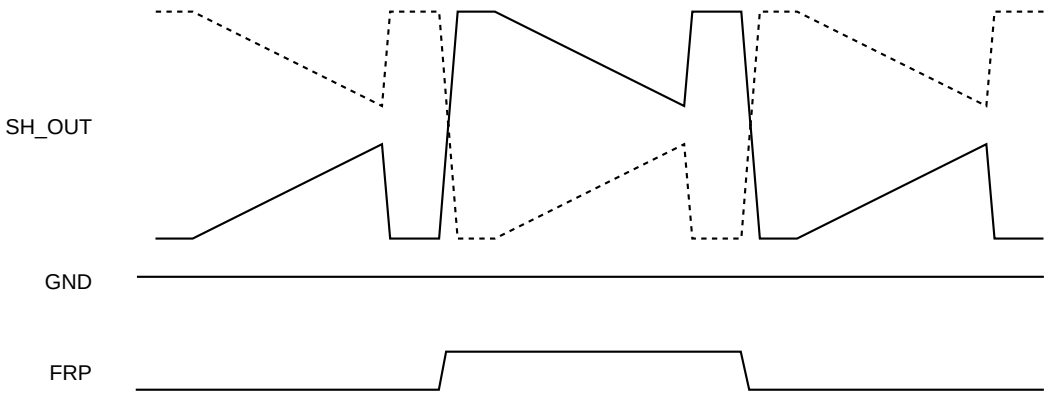
• DIRC (Pin 71), SL_SCN (Pin 73)
Scan direction settings. Output is ascending order when DIRC is set to high level, and inverted to descending order (SH_OUT1 to SH_OUT12) when set to low level. At this time if SL_SCN is set to high, the A and B port data can be switched by switching DIRC between high and low. When SL_SCN is set to low, the A port data is output from the odd-numbered SH_OUT and the B port data is output from the even-numbered SH_OUT regardless of the DIRC setting.
Set SL_SCN to high when SL_DAT is high.



	DIRC: L	DIRC: H
SL_SCN: L	SH_OUT1: A6, SH_OUT2: B6, SH_OUT3: A5, SH_OUT4: B5, SH_OUT5: A4, SH_OUT6: B4, SH_OUT7: A3, SH_OUT8: B3, SH_OUT9: A2, SH_OUT10: B2, SH_OUT11: A1, SH_OUT12: B1	SH_OUT1: A1, SH_OUT2: B1, SH_OUT3: A2, SH_OUT4: B2, SH_OUT5: A3, SH_OUT6: B3, SH_OUT7: A4, SH_OUT8: B4, SH_OUT9: A5, SH_OUT10: B5, SH_OUT11: A6, SH_OUT12: B6
SL_SCN: H	SH_OUT1: B6, SH_OUT2: A6, SH_OUT3: B5, SH_OUT4: A5, SH_OUT5: B4, SH_OUT6: A4, SH_OUT7: B3, SH_OUT8: A3, SH_OUT9: B2, SH_OUT10: A2, SH_OUT11: B1, SH_OUT12: A1	SH_OUT1: A1, SH_OUT2: B1, SH_OUT3: A2, SH_OUT4: B2, SH_OUT5: A3, SH_OUT6: B3, SH_OUT7: A4, SH_OUT8: B4, SH_OUT9: A5, SH_OUT10: B5, SH_OUT11: A6, SH_OUT12: B6

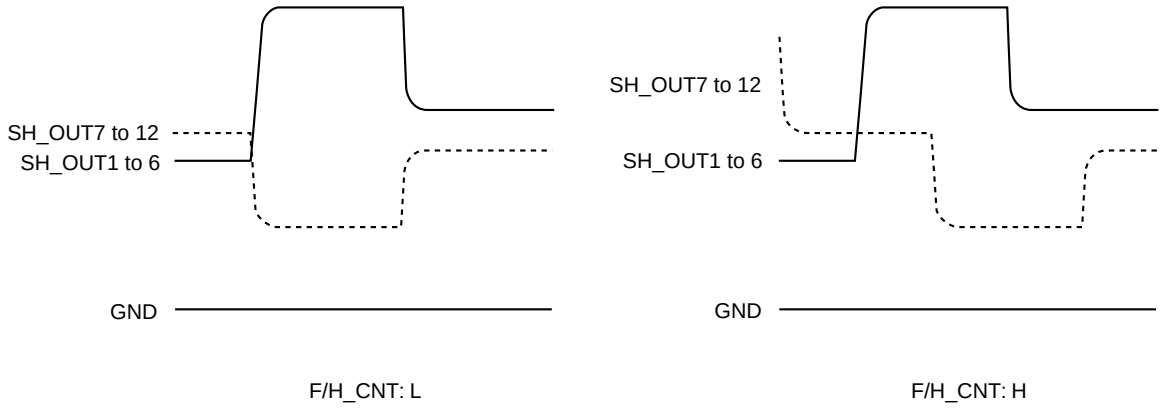
• SL_INV (Pin 74)

Dot inversion and line inversion selection. When set to low level, all SH_OUT channels are output at the same polarity as shown by the solid line in the figure below. When set to high level, the odd-numbered and even-numbered SH_OUT outputs are output at inverse polarities. At this time the odd-numbered outputs are inverted when the FRP pulse is high, and non-inverted when the FRP pulse is low. Conversely, the even-numbered outputs are inverted when the FRP pulse is low, and non-inverted when the FRP pulse is high.



• F/H_CNT (Pin 70)

SH_OUT output timing phase setting. When set to low level, all SH_OUT outputs are output at the same timing. When set to high level, SH_OUT1 to SH_OUT6 and SH_OUT7 to SH_OUT12 are output at phases offset by 1/2 clock period from each other.

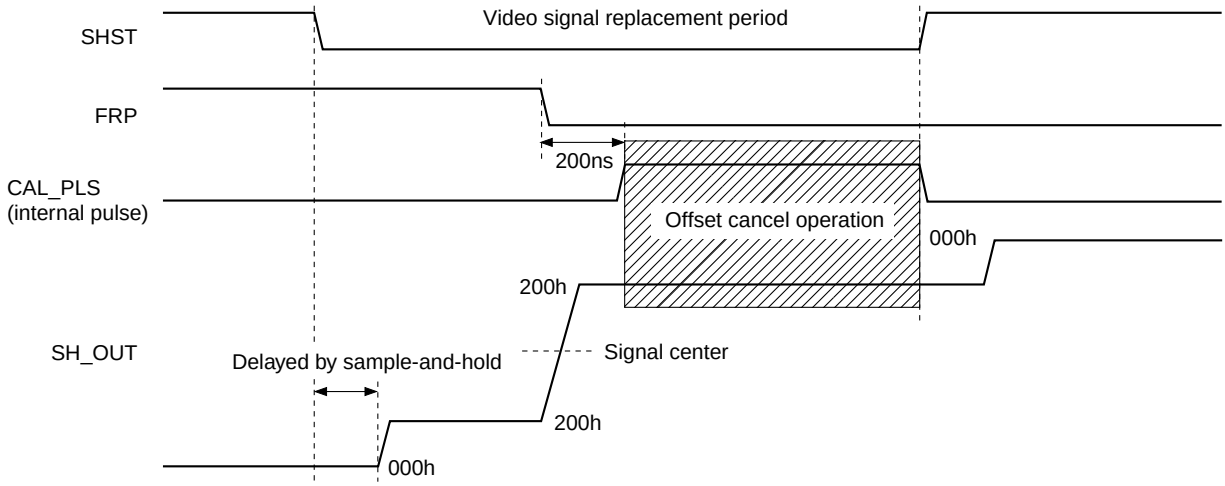


• Output phase setting

The phase of each SH_OUT output can be adjusted in MCLK period units when SL_DAT is high or in 1/2 MCLK period units when SL_DAT is low by POSCTR[3:0] (Pins 6 to 9). The phase can be set in 16 ways by 4-bit digital input. The output phase shifts backward by the above unit each time this setting is increased by one bit.

5. Calibration level generator block

The CXA3562AR generates the offset cancel circuit reference with a calibration level generator in order to minimize the deviation between channels at the center level.
The 200h output level is generated at both the AC output high and low sides, and these levels are DC output from CAL_OH and CAL_OL, respectively. At the same time, 200h data is forcibly inserted into the video signal while the video blanking period SHST pulse is low level, and feedback is applied so that the output levels of all SH_OUT channels conform to CAL_IH and CAL_IL during this period.



6. SID signal generator block

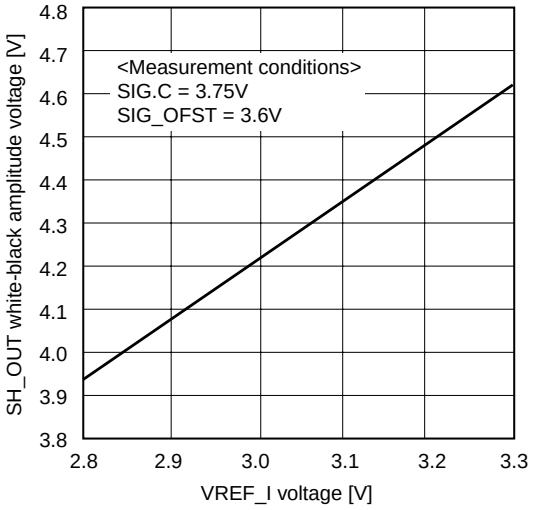
This circuit generates the precharge signal waveform used by the LCD panel.
The voltage input from PRG_LV (Pin 58) and SID_LV (Pin 59) is switched by the PRG pulse (Pin 60). The PRG_LV voltage is selected when PRG is high, and the SID_LV voltage is selected when PRG is low. This signal is then further amplified by a factor of two times and folded by the FRP pulse. The folded center voltage is the SH_OUT center voltage (voltage set by the SIG.C pin). SID_OUT (Pin 57) is inverted when FRP is high, and non-inverted when FRP is low. Conversely, SID_OUTX (Pin 56) is inverted when FRP is low, and non-inverted when FRP is high.
SID_OUT and SID_OUTX cannot directly drive the precharge signal input of the LCD panel, so they should be connected via a buffer having sufficient current supply capability.

7. VCOM potential generator block

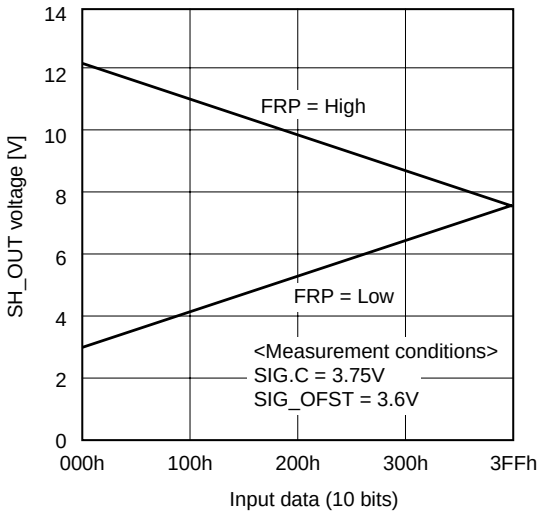
This block sets the DC common potential for the LCD panel.
VCOM_OFST (Pin 54) sets the deviation relative to the SH_OUT center potential, which is set by SIG.C.

Example of Representative Characteristics (V_{CC} = 15.5V, V_{DD} = 5.0V, Ta = 25°C)

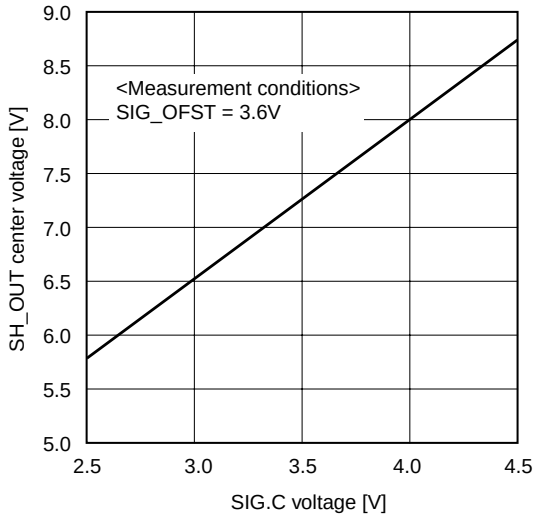
VREF_I voltage vs. SH_OUT voltage white-black amplitude



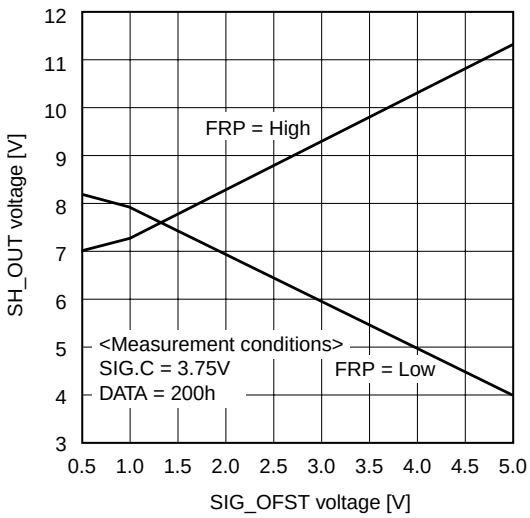
Input data vs. SH_OUT voltage



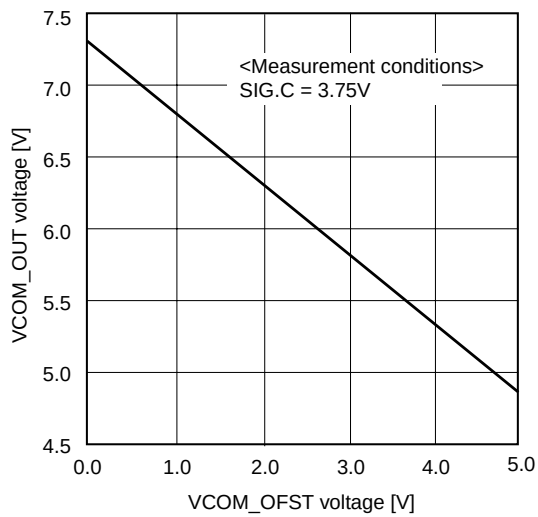
SIG.C voltage vs. SH_OUT center voltage



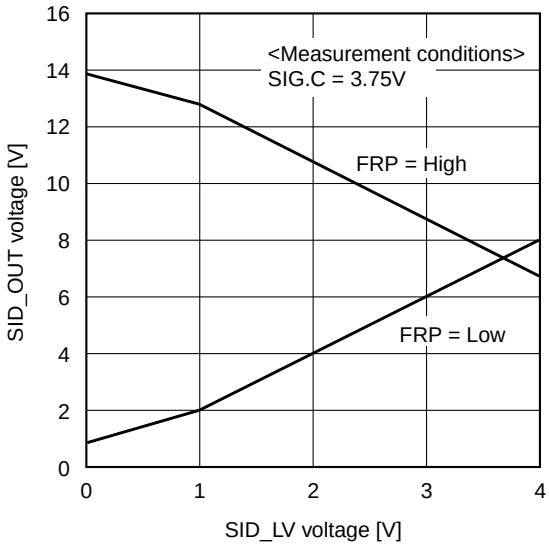
SIG_OFST voltage vs. SH_OUT voltage



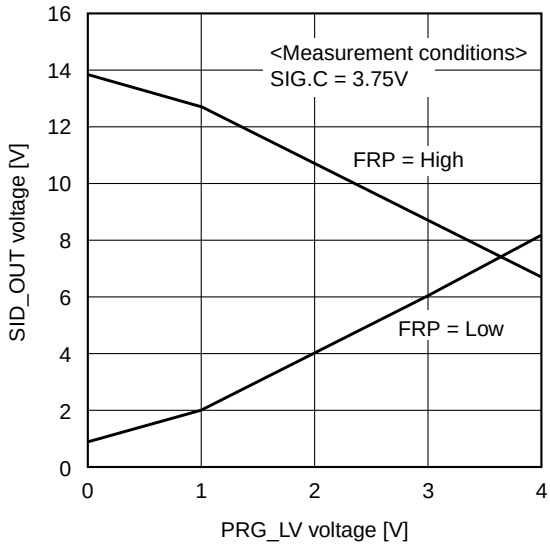
VCOM_OFST voltage vs. VCOM_OUT voltage



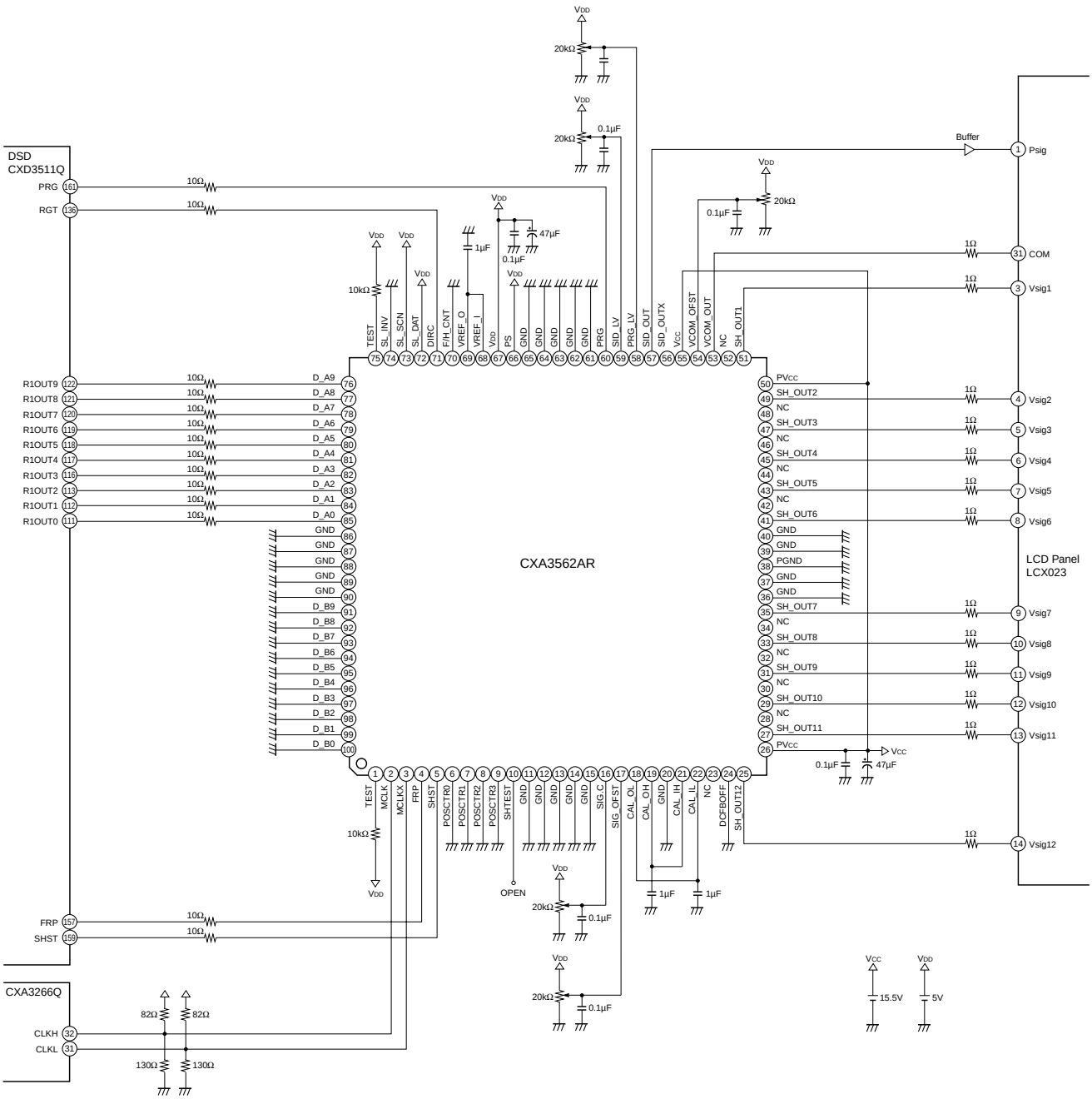
SID_LV voltage vs. SID_OUT voltage



PRG_LV voltage vs. SID_OUT voltage

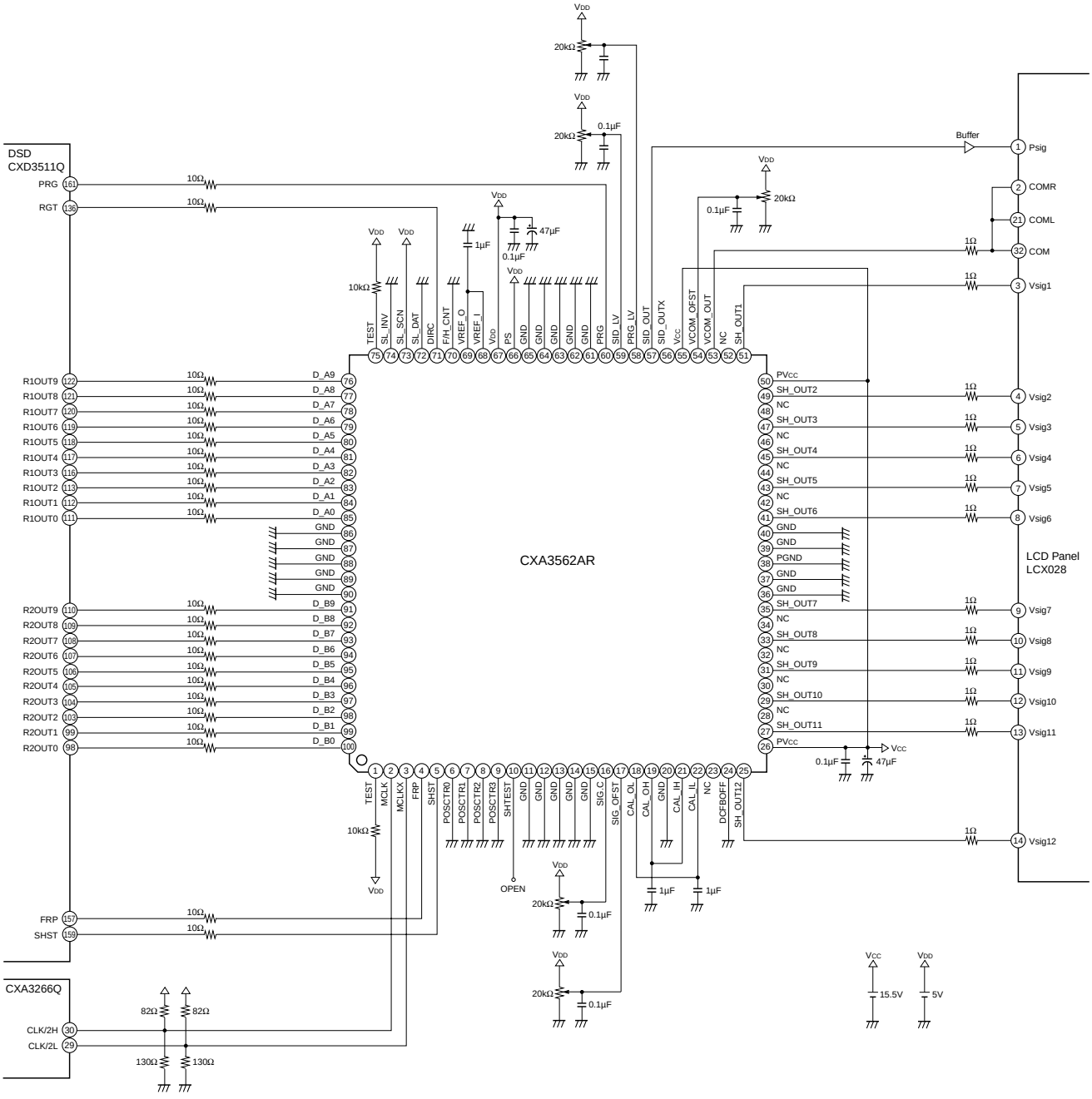


Application Circuit 1 (to XGA Panel)



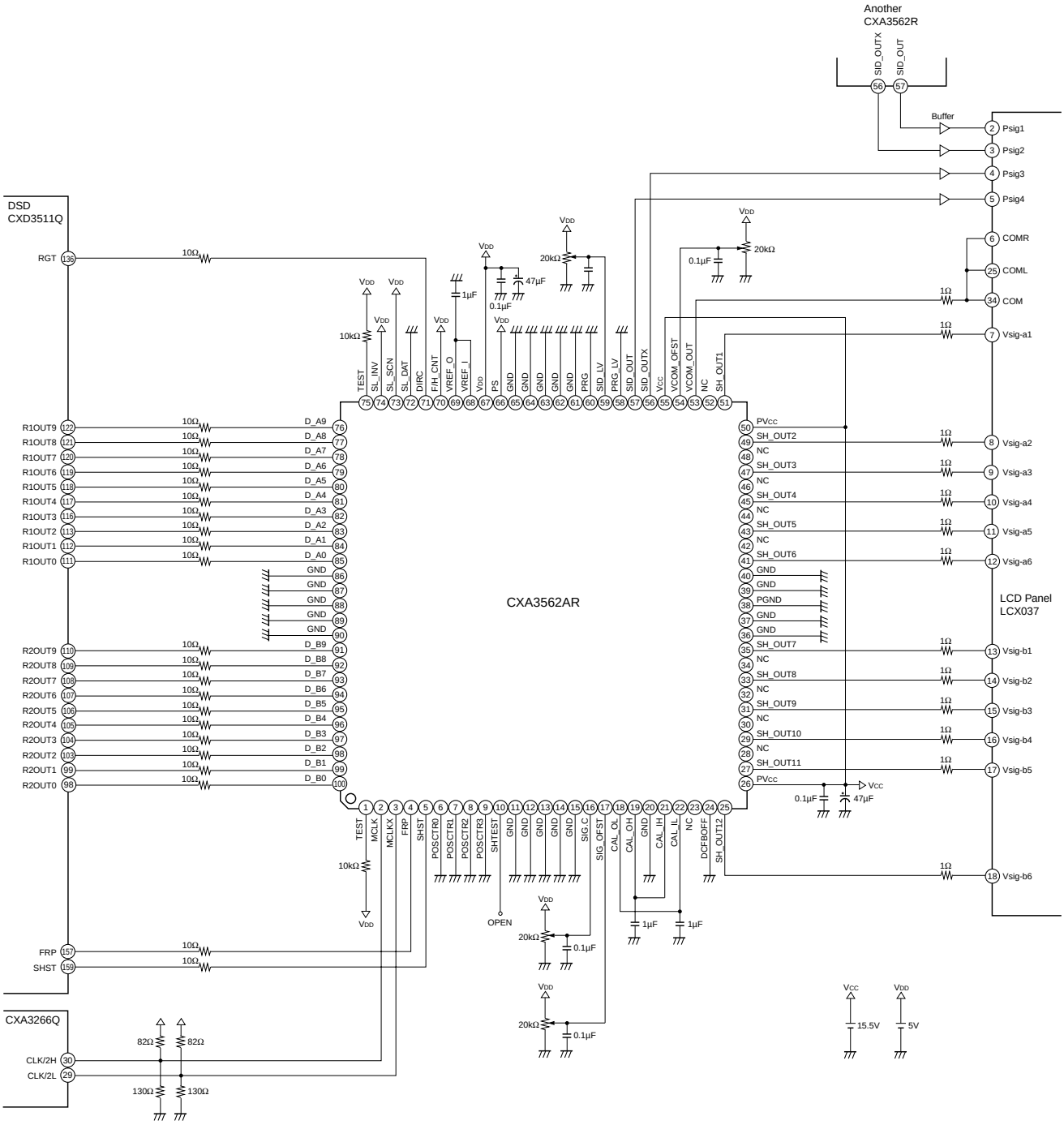
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 (to SXGA Panel)



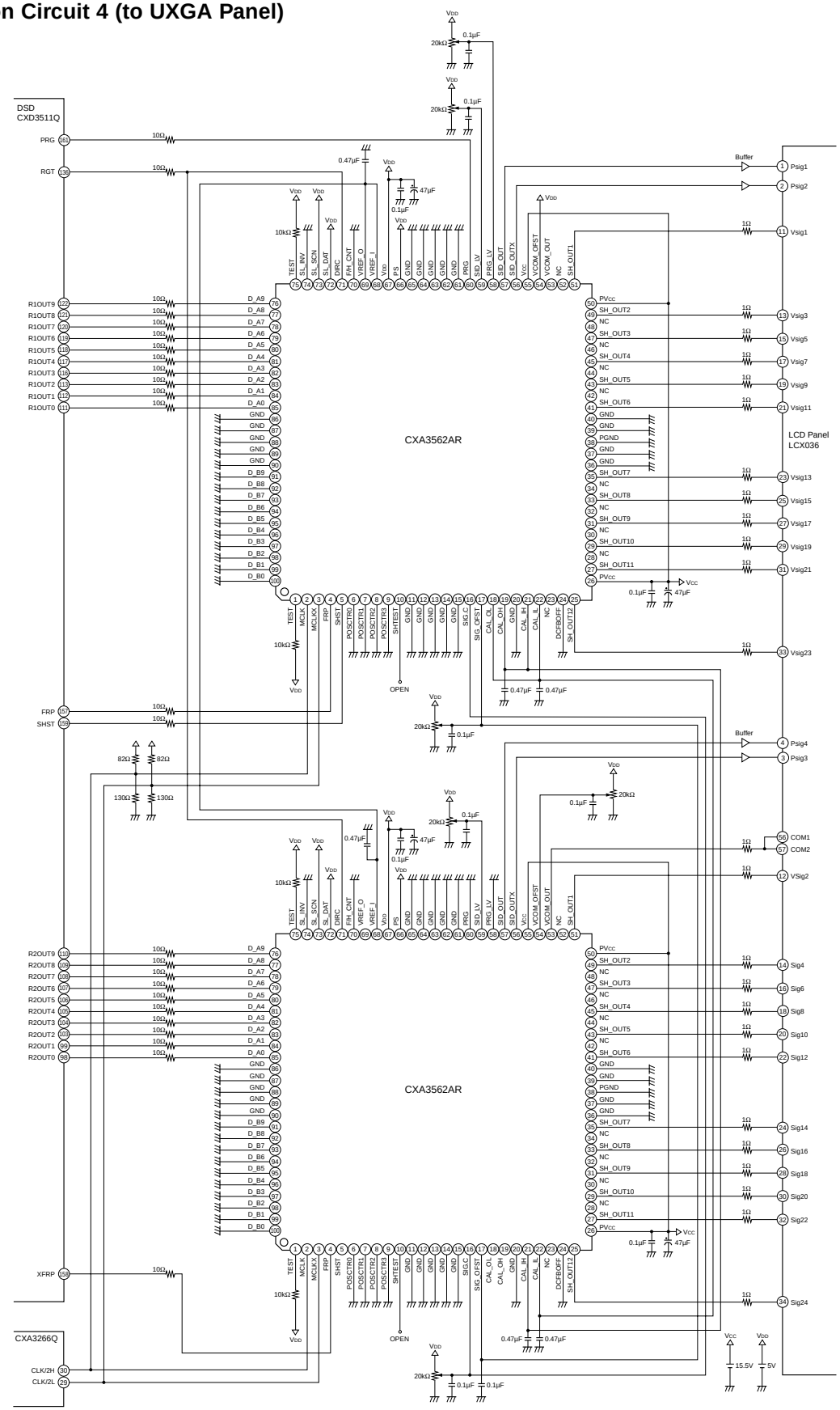
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 3 (to WXGA Panel)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 4 (to UXGA Panel)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

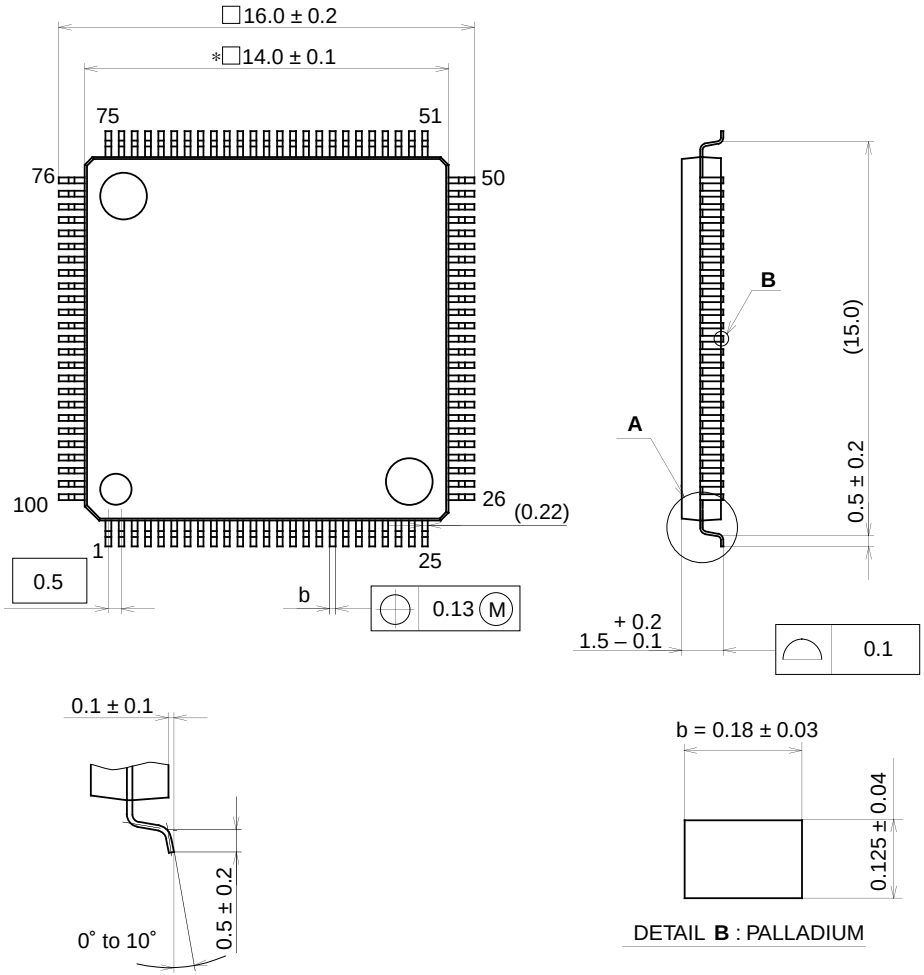
Notes on Operation

The CXA3562AR has high power consumption, so be sure to take the following radiation measures.

- Use four-layer substrate.
- GND lines connected between Pins 11 to 15, Pins 36 to 40, Pins 61 to 65 and Pins 86 to 90 should be as thick as possible.

Package Outline Unit: mm

100PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B** : PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g