SONY

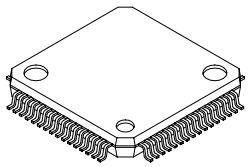
CXA7000R

LCD Driver

Description

The CXA7000R is a driver IC developed for use with Sony polycrystalline silicon TFT LCD panels. It supports 10-bit digital input, and the input data is analog demultiplexed into 6 phases and output. The CXA7000R can directly drive an LCD panel, and the VCOM setting circuit and precharge pulse waveform generator are also on-chip.

64 pin LQFP (Plastic)



Features

- Supports 10-bit input
- Supports signals up to XGA
- Low output deviation by on-chip output offset cancel circuit
- On-chip timing generator with ECL
- VCOM voltage generation circuit
- Precharge pulse waveform generation circuit

Applications

LCD projectors and other video equipment

Absolute Maximum Ratings (V_{SS} = 0V)

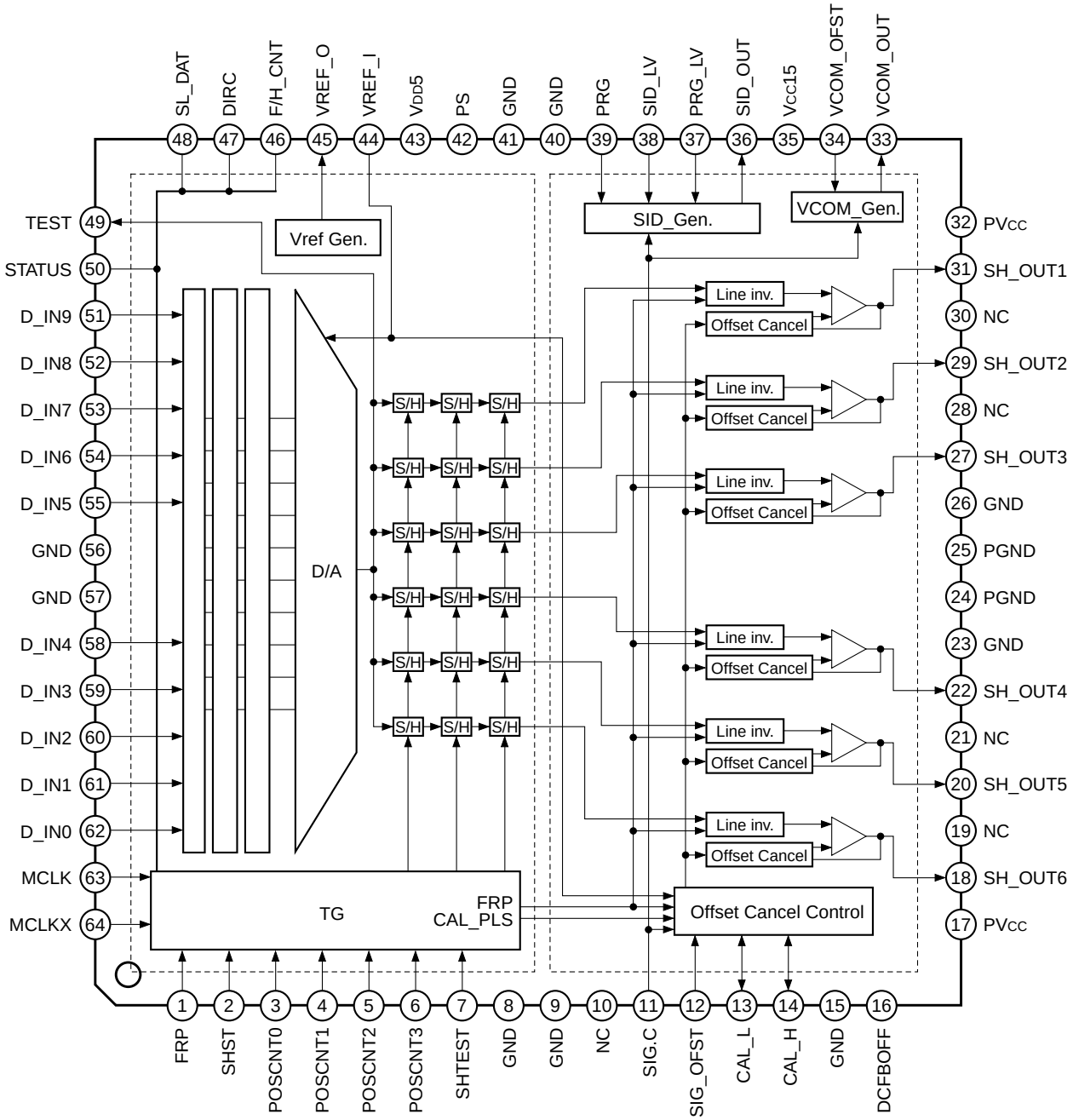
• Supply voltage	V_{CC}	16	V
	V_{DD}	5.5	V
• Operating temperature	Topr	–20 to +70	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1250	mW

Recommended Operating Conditions

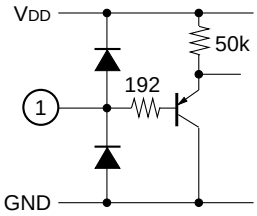
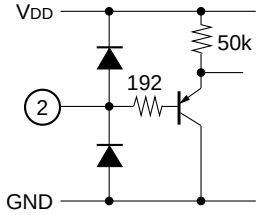
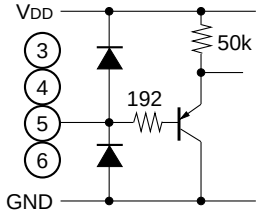
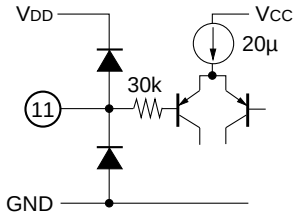
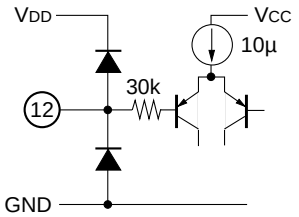
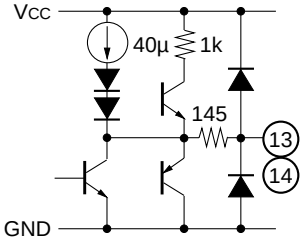
• Supply voltage	V_{CC}	15.0 to 15.5	V
	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	–20 to +70	°C

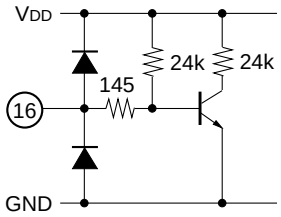
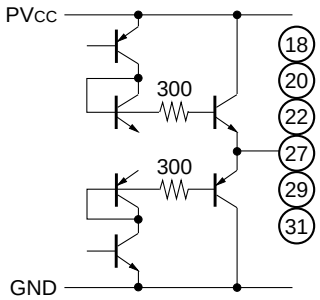
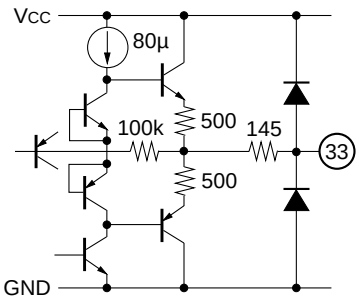
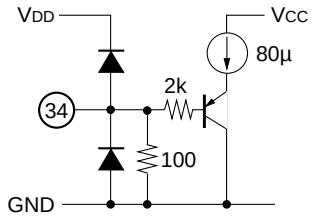
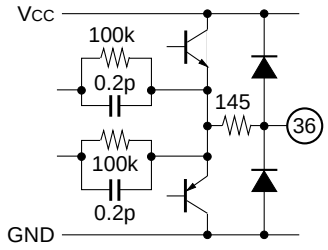
E01821A22

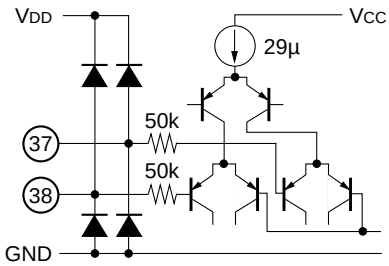
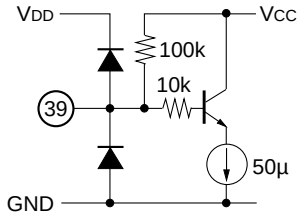
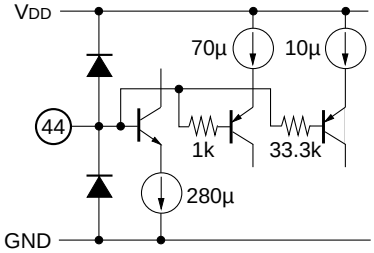
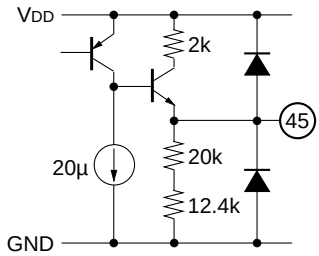
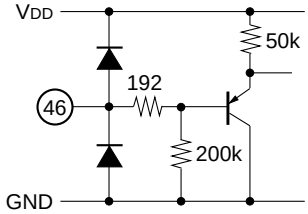
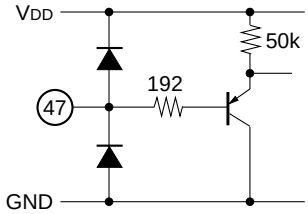
Block Diagram

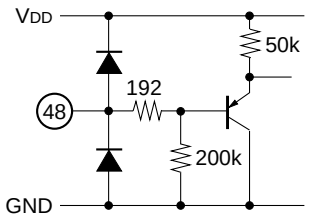
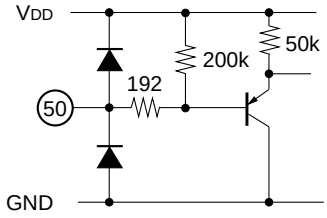
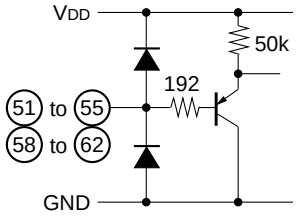
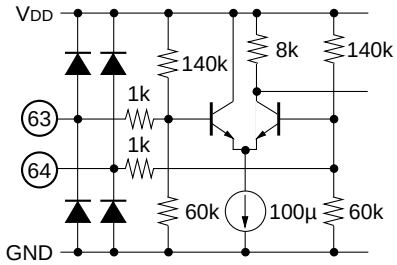
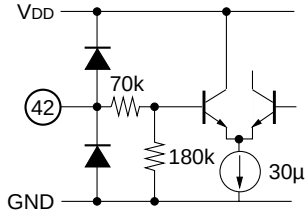


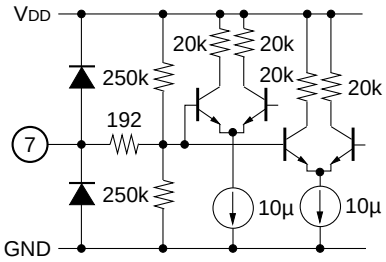
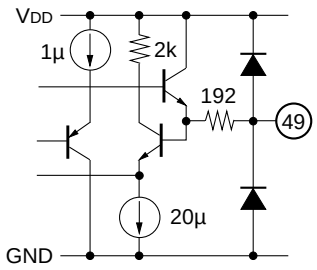
Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	FRP	I	High: ≥2.0V Low: ≤0.8V		LCD panel AC drive inversion timing input. High: inverted Low: non-inverted See the Timing Chart.
2	SHST	I	High: ≥2.0V Low: ≤0.8V		Internal sample-and-hold timing circuit reset pulse input. This pin is also used as the offset cancel level insertion timing input. A reset is applied to the internal timing generator at the falling edge.
3 4 5 6	POSCNT0 POSCNT1 POSCNT2 POSCNT3	I	High: ≥2.0V Low: ≤0.8V		Output phase adjustment. The output phase is adjusted in MCLK period units when SL_DAT is high, and in 1/2 MCLK period units when SL_DAT is low.
11	SIG.C	I	1 to 5.0V		Signal center voltage (inversion folded voltage) adjustment input. The SH_OUT output center voltage can be adjusted in the range from 7.0 to 8.0V.
12	SIG_OFST	I	0 to 5.0V		Output signal offset adjustment from signal center voltage. The SH_OUT output 100% white level (at 3FF input) voltage can be adjusted in the range from 0 to 1V from the center voltage.
13 14	CAL_L CAL_H	I/O	3.0 to 6.0V 9.0 to 12.0V		Level output for canceling the offset between channels. Connect the CAL_L and CAL_H, between ICs when using two CXA7000R.

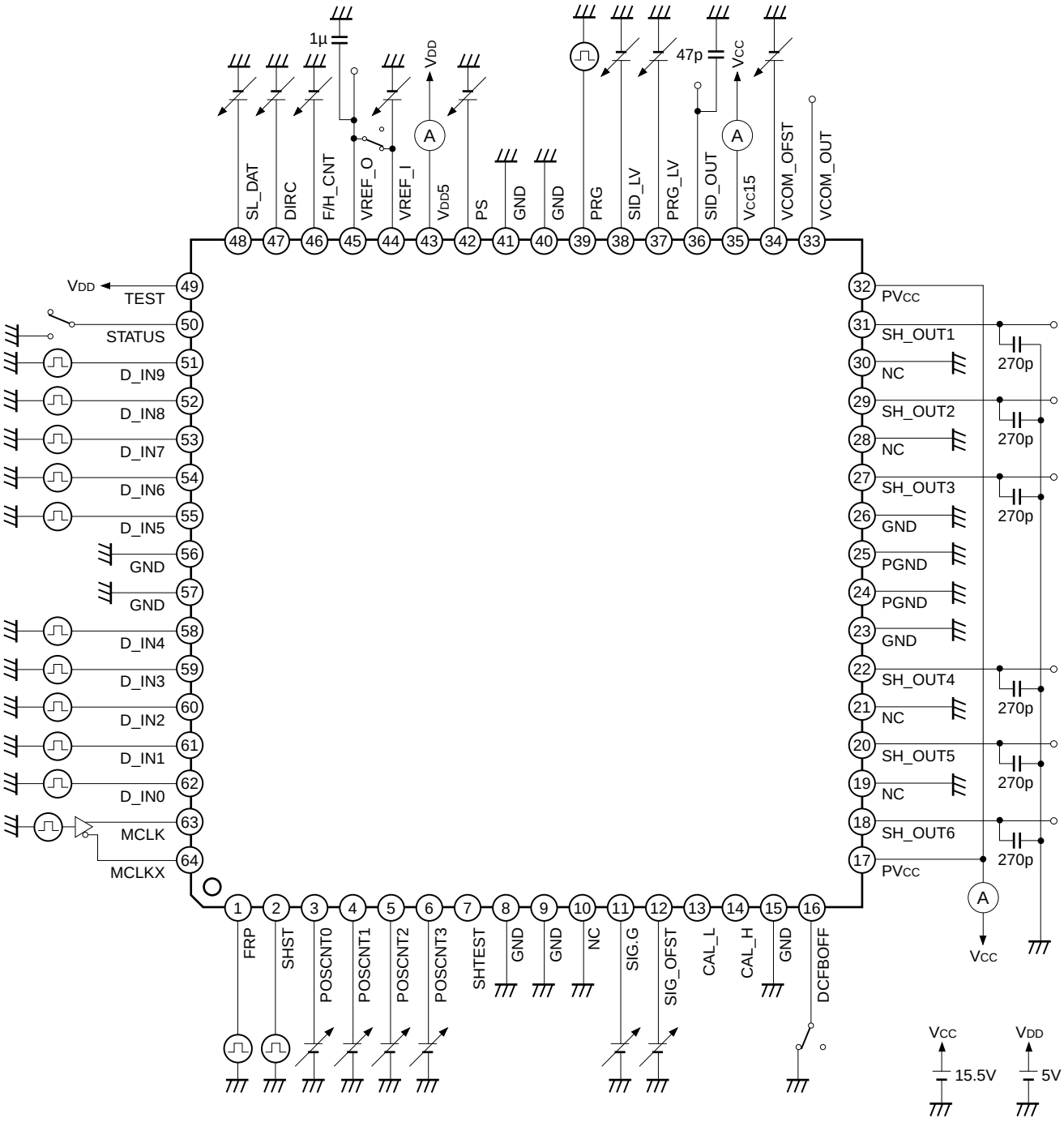
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
16	DCFBOFF	I	GND		Offset cancel function off. Normally connect to GND to use with the offset cancel function on. High (offset cancel function off) when open.
18 20 22 27 29 31	SH_OUT6 to SH_OUT1	O	1.5 to 13.5V		Demultiplexed output of AC inverse driven video signals. Can be connected directly to the LCD panel.
33	VCOM_OUT	O	5.0 to 8.0V		LCD panel common voltage output. Can be set in the range from the SH_OUT center potential Vsig.c to Vsig.c – 2V by VCOM_OFST.
34	VCOM_OFST	I	0 to 5.0V		LCD panel common voltage adjustment. VCOM_OUT can be set in the range from the SH_OUT center potential Vsig.c to Vsig.c – 2V by inputting 0 to 5V.
36	SID_OUT	O	1.5 to 13.5V		Precharge waveform output. These pins cannot directly drive the LCD panel, so input to the LCD panel with an external buffer.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
37 38	PRG_LV SID_LV	I	1.0 to 5.0V		Precharge level setting. Adjusts the SID_OUT and SID_OUTX output potential. PRG_LV is reflected when the PRG input pin (Pin 60) is high, and SID_LV is reflected when PRG is low.
39	PRG	I	High: ≥2.0V Low: ≤0.8V		Timing pulse input for switching the Pin 36 output levels. (See PRG_LV (Pin 37) and SID_LV (Pin 38).)
44	VREF_I	I	3.2V		Internal D/A converter reference voltage input. Normally connect directly to VREF_O.
45	VREF_O	O	3.2V		Reference voltage output. Normally connect directly to VREF_I, and connect to GND through a 0.5 to 1.0µF capacitor.
46	F/H_CNT	I	High: ≥2.0V Low: ≤0.8V Open: Low		SH_OUT output timing selection. High: SH_OUT1 to SH_OUT3 and SH_OUT4 to SH_OUT6 are output at different timing. Low: SH_OUT1 to SH_OUT6 are output at the same timing.
47	DIRC	I	High: ≥2.0V Low: ≤0.8V		Scan direction setting. High: output as a time series in ascending order of output pin symbol (in order from SH_OUT1 to SH_OUT6) Low: output in descending order

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
48	SL_DAT	I	High: ≥2.0V Low: ≤0.8V Open: Low		Digital input mode switch setting. High: when using master/slave mode two CXA7000R. Low: when using normal mode one CXA7000R.
50	STATUS	I	High: ≥2.0V Low: ≤0.8V		Master/slave setting when using two CXA7000R. High: master IC. Offset cancel level is output. Low: slave IC. This pin is left open (high) when using one CXA7000R.
51 to 55 58 to 62	D_IN9 to D_IN0	I	High: ≥2.0V Low: ≤0.8V		Digital data input.
63 64	MCLK MCLKX	I	PECL differential (amplitude 0.4V or more between VDD to 2V) or TTL input		Dot clock input. PECL differential input or TTL input. For TTL input, input to MCLK and connect MCLKX to GND through a capacitor.
42	PS	I	5V		Test. Normally connect to VDD.
24, 25	PGND		GND		Power GND.
17, 32	PVCC		15.5V		Power VCC.
35	VCC15		15.5V		15V power supply.
43	VDD5		5V		5V power supply.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
8, 9, 15, 23, 26, 40, 41, 56, 57	GND		GND		GND.
10, 19, 21, 28, 30	NC				NC. These pins are not connected to anything.
7	SHTEST	I	2.5V		Test. Leave open.
49	TEST	O	1.7 to 3.2V		DAC output monitor test. Normally connect to VDD.

Electrical Characteristics Measurement Circuit



Electrical Characteristics

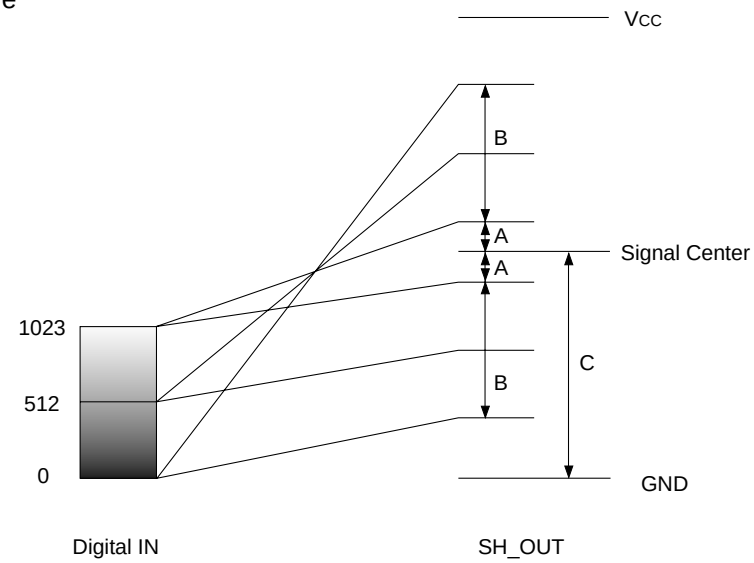
No.	Item	Symbol	Measurement points	Measurement conditions	Min.	Typ.	Max.	Unit
1	Digital input resolution	n			—	10	—	bit
2	Digital input setup time	T_S		SHST and D_IN[9:0] minimum setup time relative to MCLK input.	2	—	—	ns
3	Digital input hold time	T_H		SHST and D_IN[9:0] minimum hold time relative to MCLK input.	3	—	—	ns
4	MCLK input frequency range 1	f_{MCLK1}		SL_DAT: 5V; maximum frequency at which the internal timing generator and D/A converter operate normally.	60	—	100	MHz
5	MCLK input frequency range 2	f_{MCLK2}		SL_DAT: 0V; maximum frequency at which the internal timing generator and D/A converter operate normally.	30	—	80	MHz
6	VREF_I input voltage range	V_{VREF_I}		VREF_I input voltage range at which the D/A converter operate normally.	2.7	3.2	3.5	V
7	VREF_O output voltage range	V_{VREF_O}		Measure the VREF_O (Pin 45) voltage.	3.1	3.2	3.3	V
8	SH_OUT amplitude	$V_{SHOUTp-p}$	V_{OUT1}	Measure the SH_OUT1 voltage difference at D_IN[9:0]: 000h and 3FFh.	4.39	4.5	4.64	V
9	SH_OUT minimum amplitude	$V_{OUTMINp-p}$	V_{OUT1}	Lower the VREF_I voltage and adjust the amplitude; minimum amplitude at which SH_OUT1 can be output at D_IN[9:0]: 000h and 3FFh.	3.9	—	—	V
10	SH_OUT slew rate	SR_{OUT}	V_{OUT1} to V_{OUT6}	Load capacitance = 270pF; measure slew rate at 10 to 90% of output waveform rise and fall when D_IN[9:0] is varied from 000h to 3FFh and from 3FFh to 000h.	150	150	—	V/µs
11	SH_OUT minimum output voltage	V_{MIN}	V_{OUT1} to V_{OUT6}	Minimum voltage at which sample-and-hold outputs V_{OUT1} to V_{OUT6} can be output.	1.5	—	—	V
12	SH_OUT maximum output voltage	V_{MAX}	V_{OUT1} to V_{OUT6}	Maximum voltage at which sample-and-hold outputs V_{OUT1} to V_{OUT6} can be output.	—	—	13.5	V
13	Output deviation between channels 1	D_{OUT1}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value at D_IN[9:0]: 200h.	—	3	10	mVp-p
14	Output deviation between channels 2	D_{OUT2}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value at D_IN[9:0]: 000h or 3FFh.	—	10	40	mVp-p
15	Output deviation between ICs 1	D_{IC1}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value at D_IN[9:0]: 200h. (when using two CXA7000R)	—	10	—	mVp-p

No.	Item	Symbol	Measurement points	Measurement conditions	Min.	Typ.	Max.	Unit
16	Output deviation between ICs 2	D_{IC2}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value at D_IN[9:0]: 000h or 3FFh. (when using two CXA7000R)	—	20	—	mVp-p
17	SID output gain 1	A_{SID1}	V_{SID_LV} V_{SID}	PRG: 0V; measure V_{SID_LV} and V_{SID} at FRP: 0V, and V_{SID_LV} at FRP: 5V. Calculate as $A_{SID1} = V_{SID}/V_{SID\_LV}$.	1.9	2	2.1	times
18	SID output gain 2	A_{SID2}	V_{PRG_LV} V_{SID}	PRG: 5V; measure V_{PRG_LV} and V_{SID} at FRP: 0V, and V_{PRG_LV} at FRP: 5V. Calculate as $A_{SID2} = V_{SID}/V_{PRG\_LV}$.	1.9	2	2.1	times
19	SID output slew rate	SR_{SID}	V_{SID}	Load capacitance = 47pF, PRG: 0V; input a repeating high/low pulse to FRP (Pin 1), and apply DC input voltage so that V_{SID} is 4V/10V. Measure slew rate at 10 to 90% of output waveform rise and fall.	27	50	—	V/µs
20	Signal center adjustable range	V_{SIG}	V_{OUT1}	V_{OUT1} center voltage when SIG.C (Pin 11) is varied from 0 to 5V.	7	—	8	V
21	SH_OUT offset adjustable range	$V_{SIGOFST}$	V_{OUT1}	D_IN[9:0]: 3FFh, FRP: 0V; value obtained by subtracting V_{OUT1} from V_{OUT1} center voltage when SIG_OFST (Pin 12) is varied from 0 to 5V.	0	—	1	V
22	VCOM adjustable range	V_{COM}	V_{COM}	VCOM_OUT voltage when VCOM_OFST (Pin 34) is varied from 0 to 5V.	Vc – 2.5	—	Vc	V
23	V_{DD} current consumption	I_{DD}	I_{VDD}	$I_{DD} = I_{VDD}$	—	52	—	mA
24	V_{CC} current consumption	I_{CC}	I_{VCC1} I_{VCC2}	$I_{CC} = I_{VCC1} + I_{VCC2}$	—	18	—	mA
25	Current consumption in power saving mode	I_{PS}	I_{VDD} I_{VCC1} I_{VCC2}	GND (Pin 42), $I_{CC} = I_{VDD} + I_{VCC1} + I_{VCC2}$	—	28	—	mA
26	Differential linearity error	D_{LE}	—	V_{VREF_I} = 3.2V	–0.5		0.7	LSB
27	Integral linearity error	I_{LE}	—	V_{VREF_I} = 3.2V	–1.5		0.4	LSB

Description of Operation

The flow of internal operations is described below.
The digital signals input to D_IN0 to D_IN9 are internally D/A converted into approximately 1.5V (at VREF_I: 3.2V) analog signals. After that, the signal that has been demultiplexed into 6 phases is amplified by a factor of three times, inverted at the signal center potential according to FRP, and output.
The output level relative to the digital input changes according to the following settings.

A: SIG_OFST voltage
B: VREF_I voltage
C: SIG.C voltage



1. Digital input block

The CXA7000R can be set to master/slave mode, single mode and left/light inversion. This makes it possible to support various systems.
In master/slave mode, the even and odd data is internally selected respectively and input to the D/A converter.

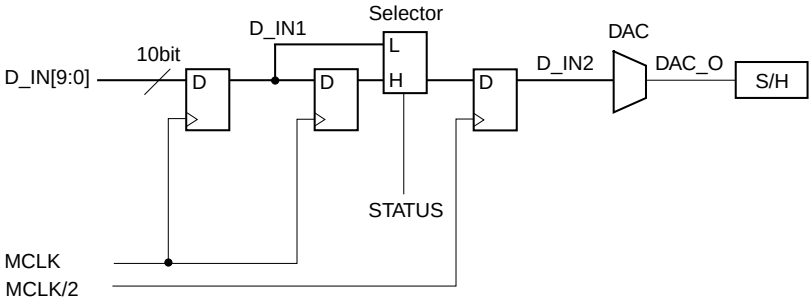
2. D/A converter block

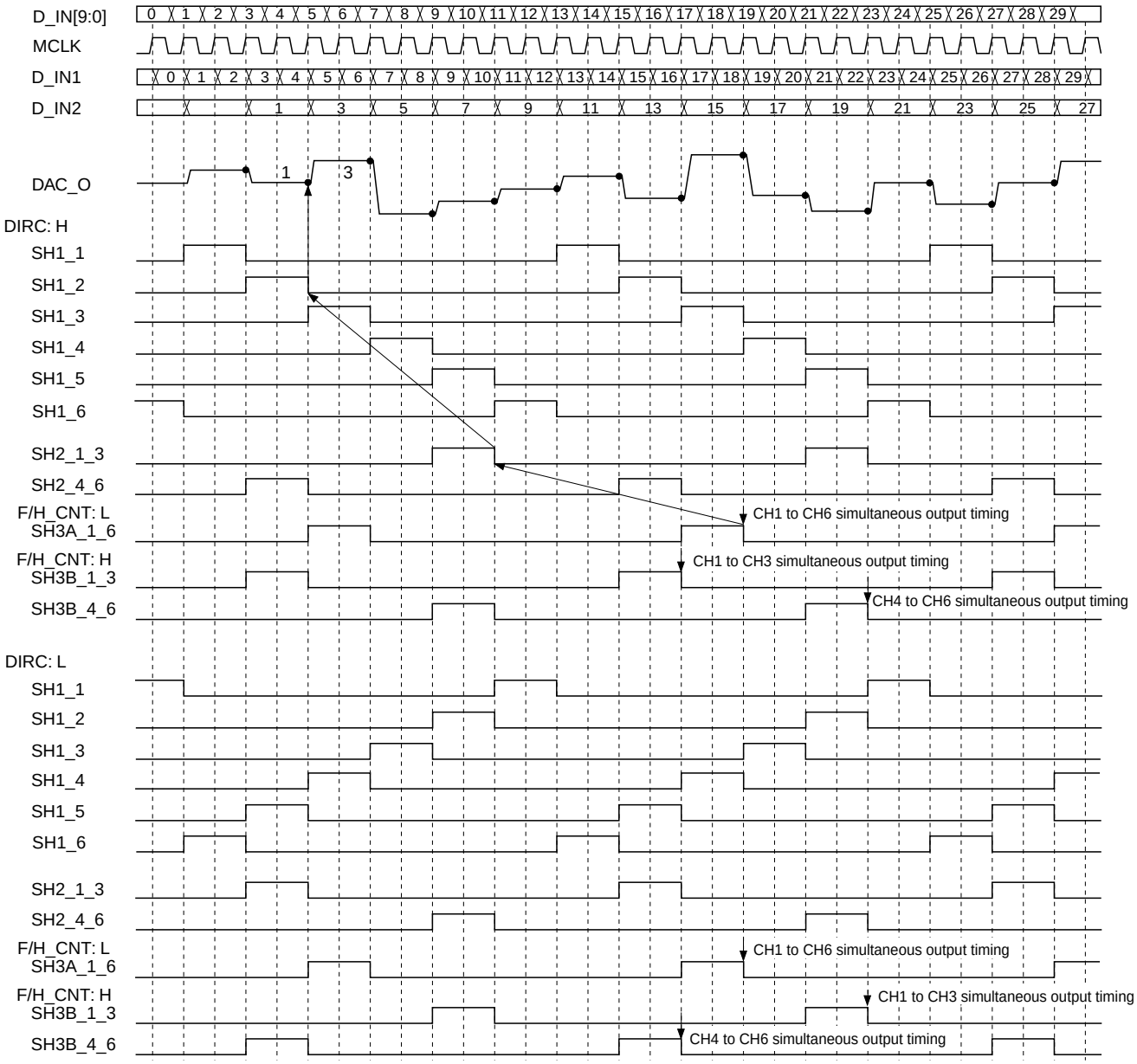
The internal D/A converter has two systems for odd-numbered and even-numbered outputs. The voltage input from VREF_I becomes the 100% white level potential of the analog converted signal, and this amplitude is a maximum 1.5Vp-p with respect to input data of 000h to 3FFh.

3. Sample-and-hold (S/H) block

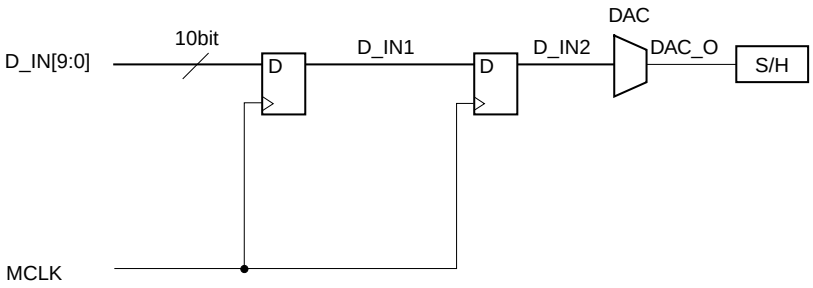
The D/A converter outputs are input to the sample-and-hold blocks, respectively. The signals are converted from time series signals into 6-phase cyclic parallel signals by the sample-and-hold group which is appropriately controlled by the internal timing generator. For forward scan, the signals are output in the ascending order of SH_OUT1, SH_OUT2, SH_OUT3 ... SH_OUT6. For reverse scan, this order is inverted and the signals are output in descending order. Connect the signals to the LCD panel according to the order used. The timing of each sample-and-hold pulse is shown on the following pages. These pulses are not output and are used only inside the IC.

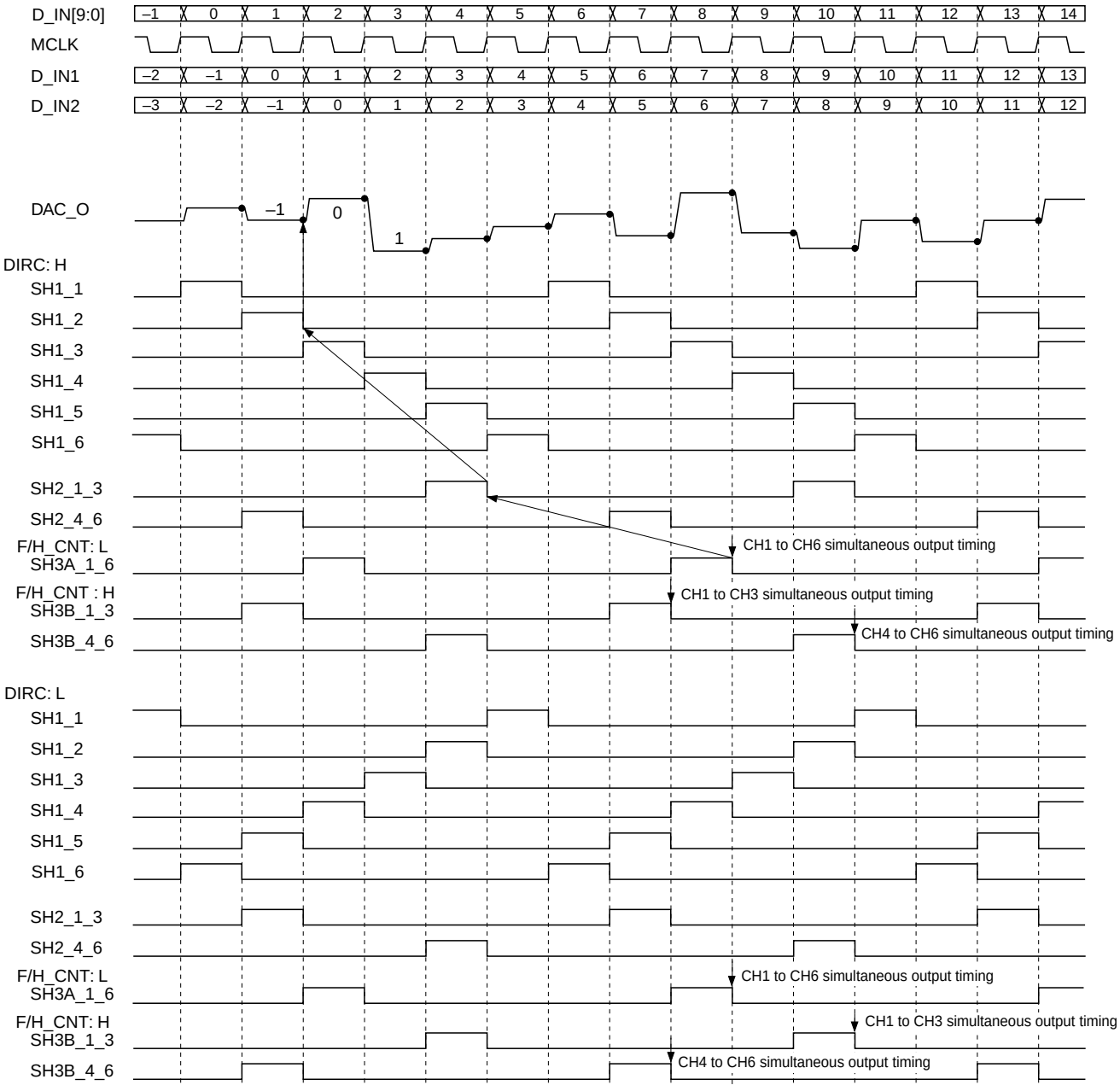
Master/slave mode





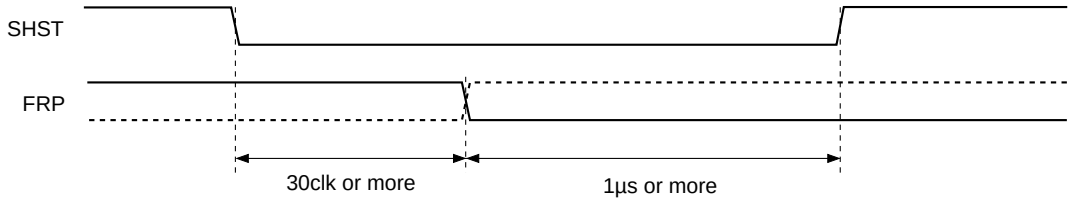
Single mode


D_IN[9:0]
10bit
D
D_IN1
D
D_IN2
DAC
DAC_O
S/H
MCLK


D_IN[9:0]
MCLK
D_IN1
D_IN2
DAC_O
DIRC: H
SH1_1
SH1_2
SH1_3
SH1_4
SH1_5
SH1_6
SH2_1_3
SH2_4_6
F/H_CNT: L
SH3A_1_6
F/H_CNT : H
SH3B_1_3
SH3B_4_6
CH1 to CH6 simultaneous output timing
CH1 to CH3 simultaneous output timing
CH4 to CH6 simultaneous output timing
DIRC: L
SH1_1
SH1_2
SH1_3
SH1_4
SH1_5
SH1_6
SH2_1_3
SH2_4_6
F/H_CNT: L
SH3A_1_6
F/H_CNT: H
SH3B_1_3
SH3B_4_6
CH1 to CH6 simultaneous output timing
CH1 to CH3 simultaneous output timing
CH4 to CH6 simultaneous output timing

4. Timing generator (TG) block

The internal timing generator operates by one pair of differential clock inputs (MCLK, MCLKX) and a horizontal sync signal input (SHST), and generates the timing pulses needed by the demultiplexer block, dot inversion control pulse and output deviation cancel circuit. The various operating modes can be designated by the pin settings.
The SHST and FRP inputs should satisfy the relationship shown in the figure below with the MCLK and MCLKX input period as 1clk.



The CXA7000R can select various operating modes according to the timing generator block settings. These settings are described below.

• SL_DAT (Pin 48)
Operation mode selection. Master/slave mode is selected which is common with digital input of two ICs when set to high level, and single mode is selected with one IC when set to low level. In case of the former, connect 10-bit input as short as possible between two ICs and select which data of odd or even is obtained by STATUS (Pin 50).

• DIRC (Pin 47)
Scan direction settings. Output is ascending order when DIRC is set to high level, and inverted to descending order (SH_OUT1 to SH_OUT6) when set to low level. Also, the output is varied as shown below in combination with STATUS (Pin 50).

D_IN[9:0] 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

SL_DAT: L

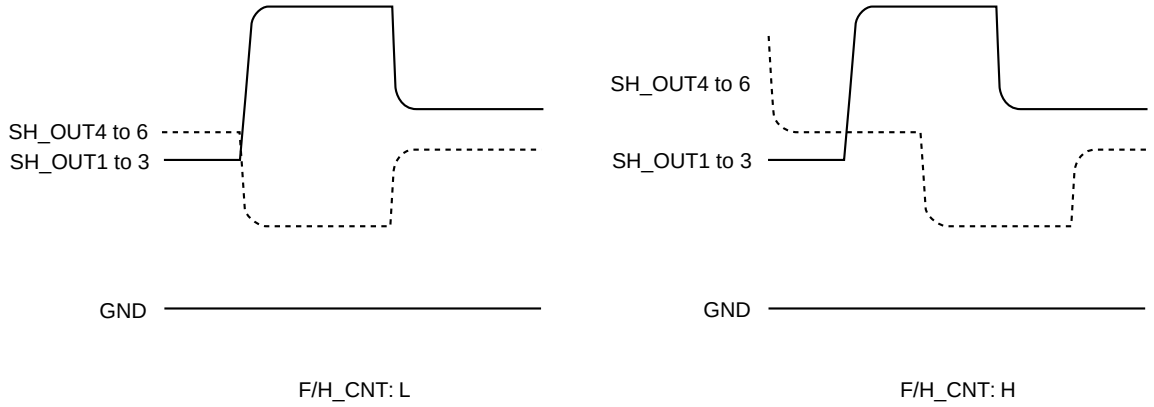
DIRC: L	DIRC: H
SH_OUT1: 6 SH_OUT2: 5 SH_OUT3: 4 SH_OUT4: 3 SH_OUT5: 2 SH_OUT6: 1	SH_OUT1: 1 SH_OUT2: 2 SH_OUT3: 3 SH_OUT4: 4 SH_OUT5: 5 SH_OUT6: 6

SL_DAT: H

	DIRC: L	DIRC: H
STATUS: L	SH_OUT1: 11 SH_OUT2: 9 SH_OUT3: 7 SH_OUT4: 5 SH_OUT5: 3 SH_OUT6: 1	SH_OUT1: 2 SH_OUT2: 4 SH_OUT3: 6 SH_OUT4: 8 SH_OUT5: 10 SH_OUT6: 12
STATUS: H	SH_OUT1: 12 SH_OUT2: 10 SH_OUT3: 8 SH_OUT4: 6 SH_OUT5: 4 SH_OUT6: 2	SH_OUT1: 1 SH_OUT2: 3 SH_OUT3: 5 SH_OUT4: 7 SH_OUT5: 9 SH_OUT6: 11

• F/H_CNT (Pin 46)

SH_OUT output timing phase setting. When set to low level, all SH_OUT outputs are output at the same timing. When set to high level, SH_OUT1 to SH_OUT3 and SH_OUT4 to SH_OUT6 are output at phases offset by 1/2 clock period from each other.

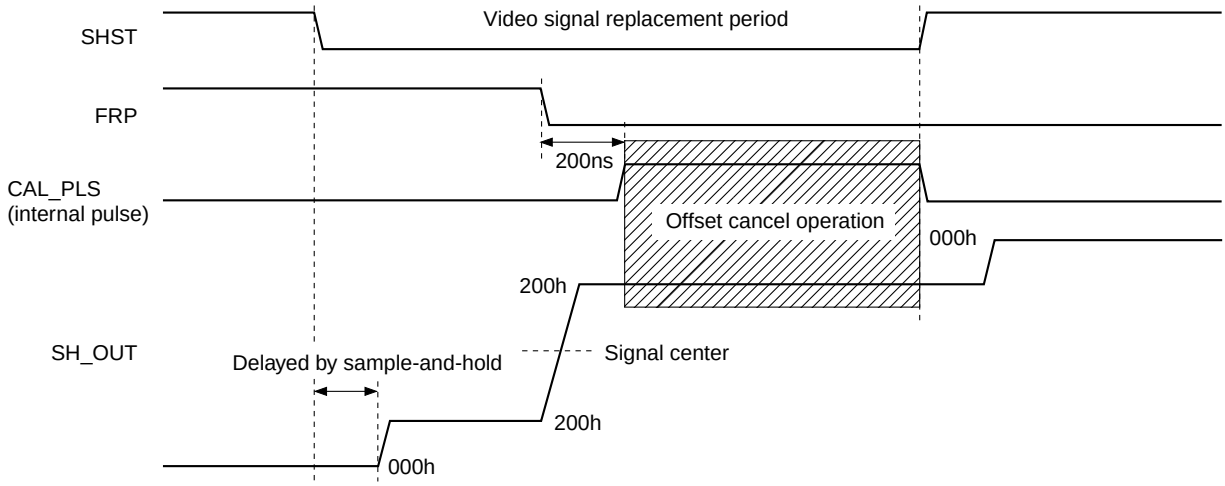


• Output phase setting

The phase of each SH_OUT output can be adjusted by POSCNT[3:0] (Pins 3 to 6). The phase can be set in 16 ways by 4-bit digital input. The output phase shifts backward by the clock period units when SL_DAT is high or 1/2 clock period units when SL_DAT is low each time this setting is increased by one bit.

5. Calibration level generator block

The CXA7000R has a built-in offset cancel circuit and generates the reference with a calibration level generator in order to minimize the deviation between channels at the center level.
The 200h output level is generated at both the AC output high and low sides respectively when STATUS (Pin 50) is high level, and these levels are DC output from CAL_H and CAL_L and at the same time, these are used internally. When STATUS (Pin 50) is low level, CAL_H and CAL_L are input pins and the external offset cancel level is input. The 200h data is forcibly inserted into the video signal while the video blanking period SHST pulse is low level, and feedback is applied so that the output levels of all SH_OUT channels conform to CAL_H and CAL_L during this period.



6. SID signal generator block

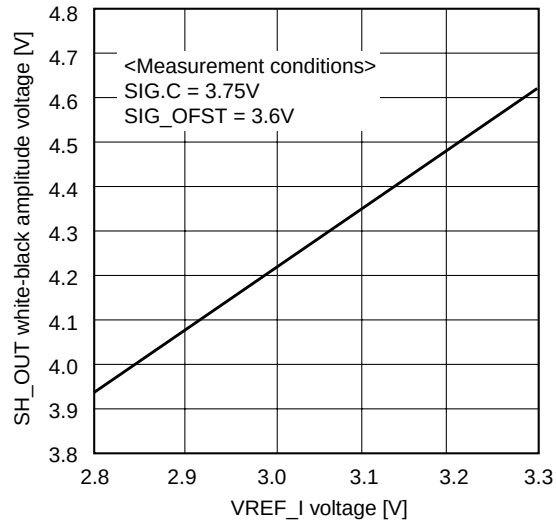
This circuit generates the precharge signal waveform used by the LCD panel.
The voltage input from PRG_LV (Pin 37) and SID_LV (Pin 38) is switched by the PRG pulse (Pin 39). The PRG_LV voltage is selected when PRG is high, and the SID_LV voltage is selected when PRG is low. This signal is then further amplified by a factor of two times and folded by the FRP pulse. The folded center voltage is the SH_OUT center voltage (voltage set by the SIG.C pin). SID_OUT (Pin 36) is inverted when FRP is high, and non-inverted when FRP is low.
SID_OUT cannot directly drive the precharge signal input of the LCD panel, so they should be connected via a buffer having sufficient current supply capability.

7. VCOM potential generator block

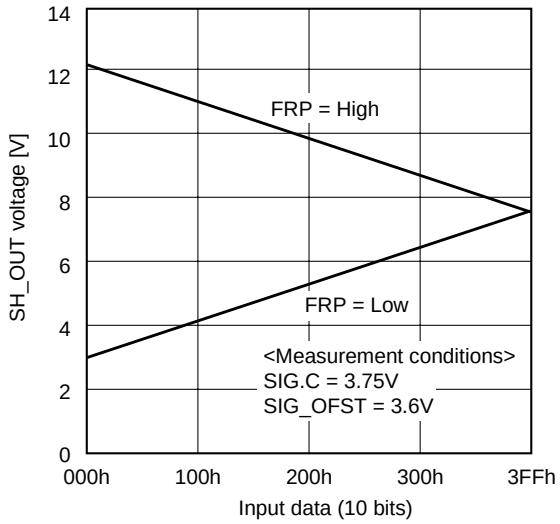
This block sets the DC common potential for the LCD panel.
VCOM_OFST (Pin 33) sets the deviation relative to the SH_OUT center potential, which is set by SIG.C.

Example of Representative Characteristics (V_{CC} = 15.5V, V_{DD} = 5.0V, Ta = 25°C)

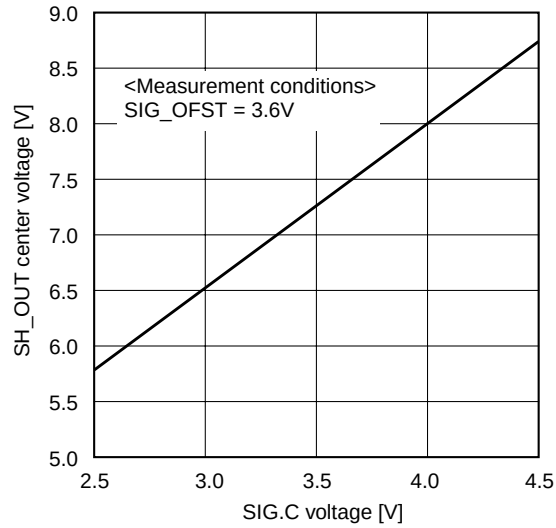
VREF_I voltage vs. SH_OUT voltage white-black amplitude



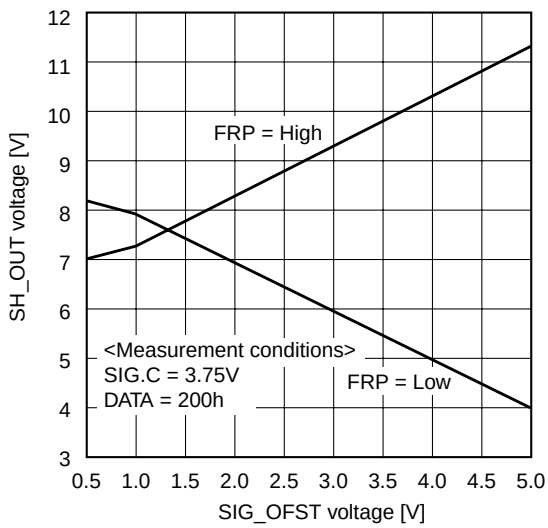
Input data vs. SH_OUT voltage



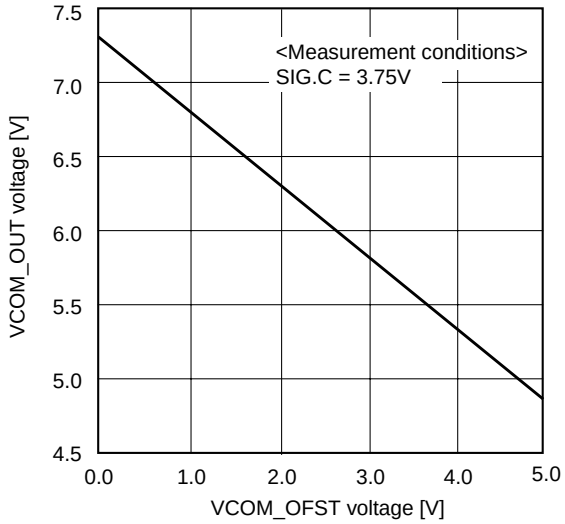
SIG.C voltage vs. SH_OUT center voltage



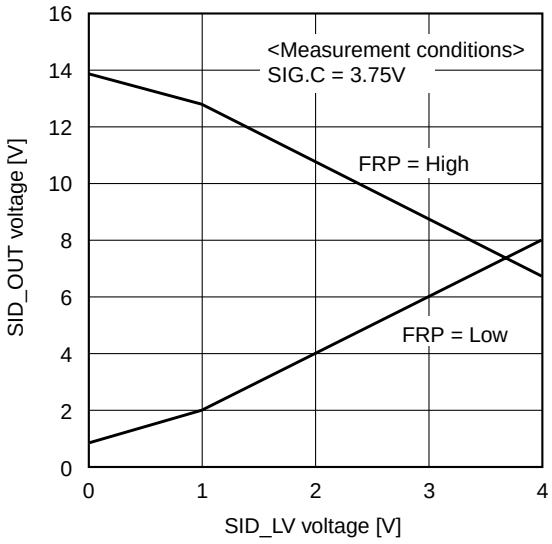
SIG_OFST voltage vs. SH_OUT voltage



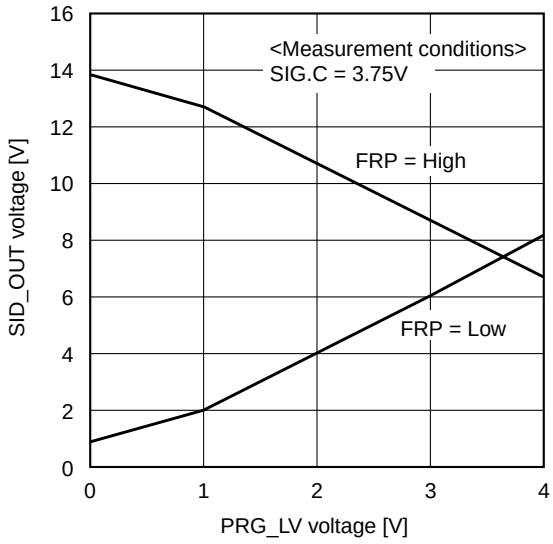
VCOM_OFST voltage vs. VCOM_OUT voltage



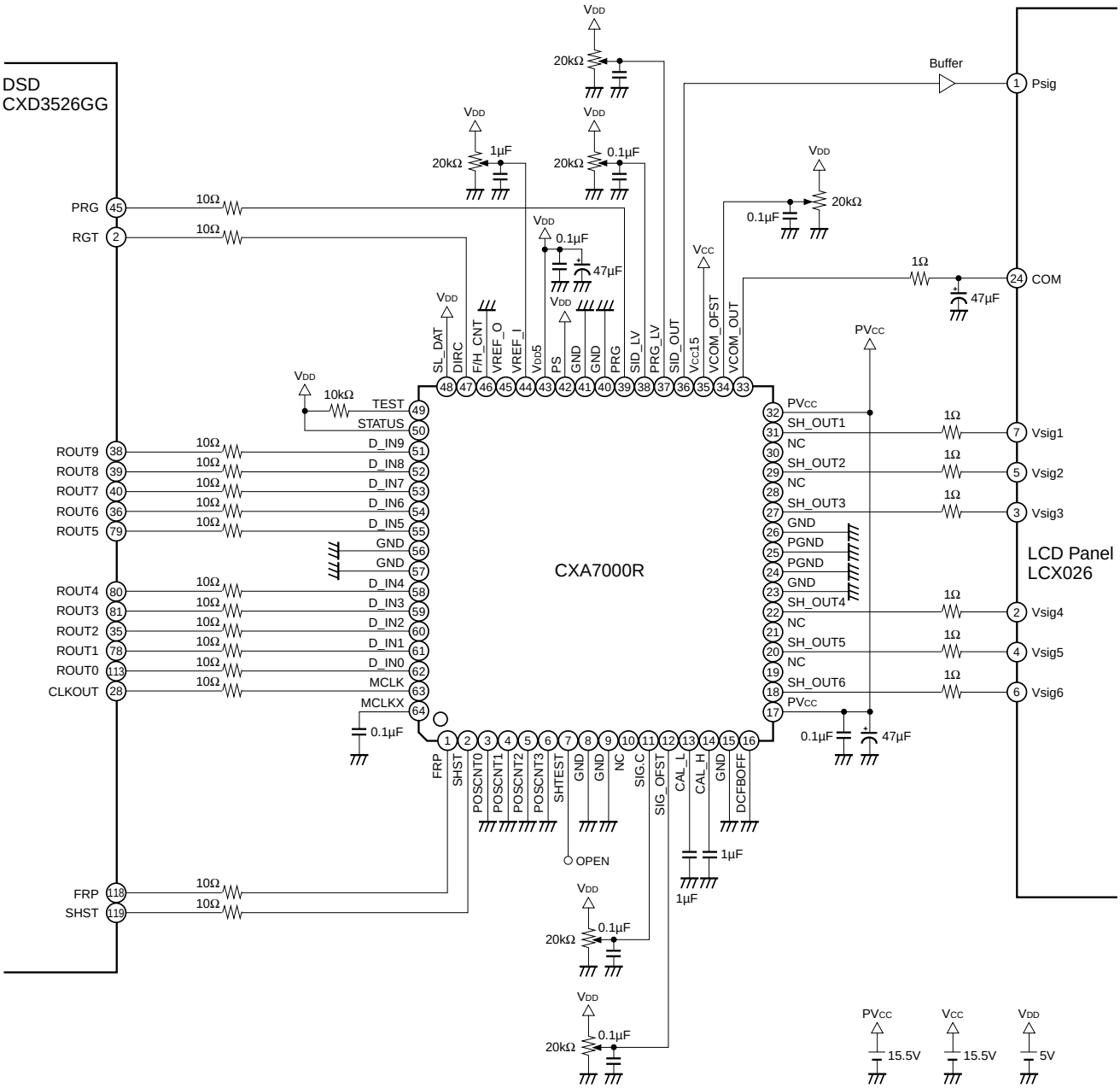
SID_LV voltage vs. SID_OUT voltage



PRG_LV voltage vs. SID_OUT voltage

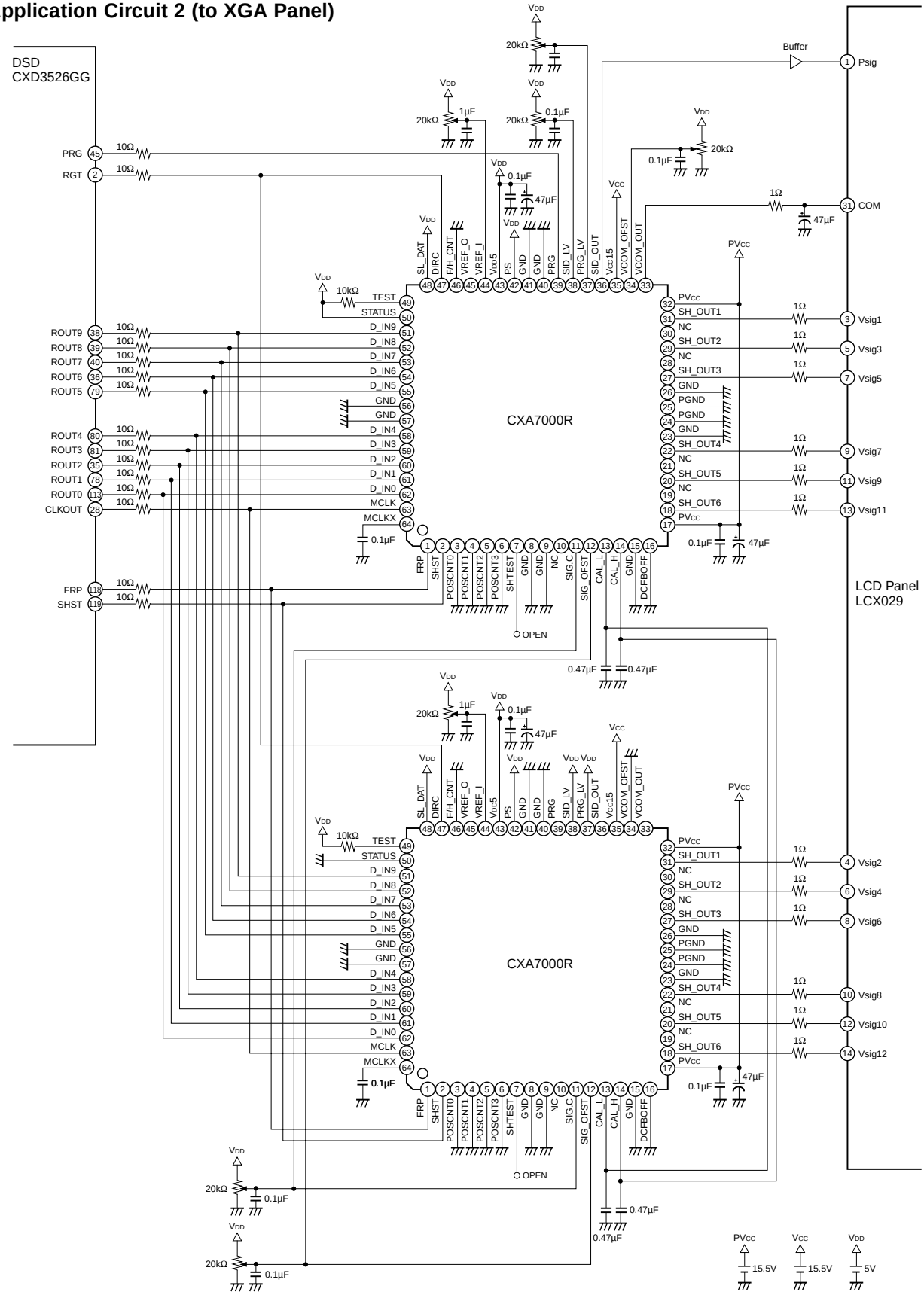


Application Circuit 1 (to SVGA Panel)



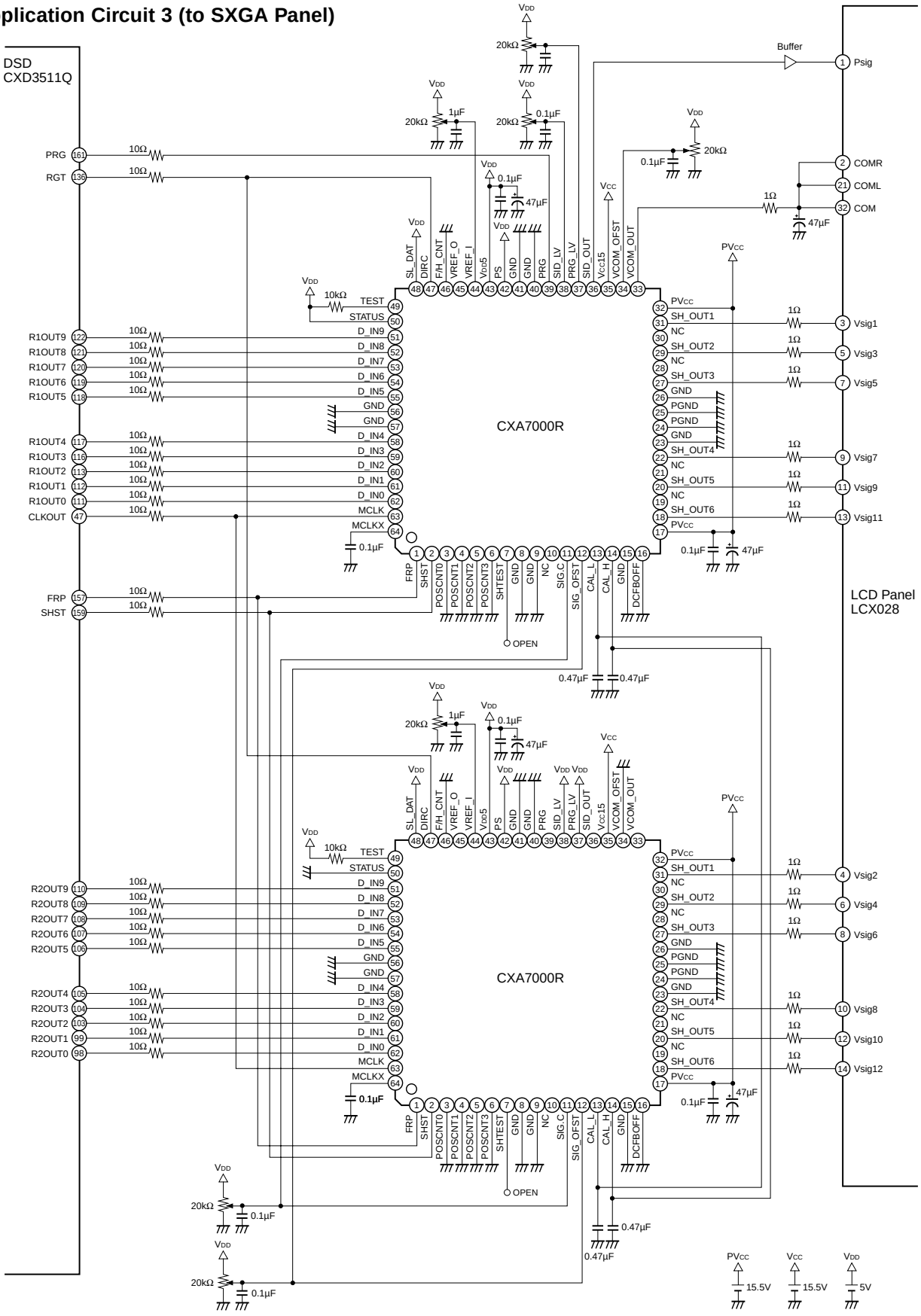
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 (to XGA Panel)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 3 (to SXGA Panel)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

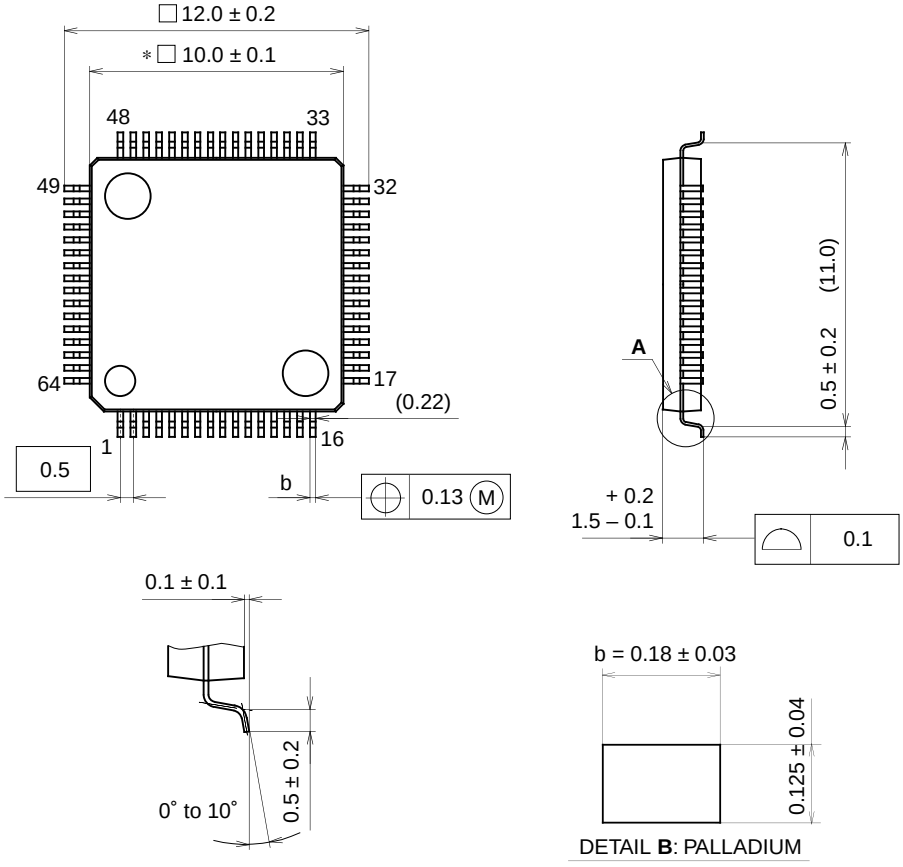
Notes on Operation

The CXA7000R has high power consumption, so be sure to take the following radiation measures.

- Use four-layer substrate.
- GND lines connected to Pins 8, 9, 24, 25, 40, 41, 56 and 57 should be as thick as possible.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	P-LQFP64-10x10-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g