XC7300 CMOS EPLD Family

Product Description

Features

- High-performance Erasable Programmable Logic Devices (EPLDs)
  - 5 / 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 167 MHz maximum clock frequency
- Advanced Dual-Block architecture
  - Fast Function Blocks
  - High-Density Function Blocks (XC7354, XC7372, XC73108, XC73144)
- 100% interconnect matrix
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 43 to 61 MHz 18-bit accumulators
- Multiple independent clocks
- Each input programmable as direct, latched, or registered
- High-drive 24 mA output
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- Supported by industry standard design and verification tools
- 100% PCI compliant

Description

The XC7300 family employs a unique Dual-Block architecture, which provides high speed operations via Fast Function Blocks and/or high density capability via High Density Function Blocks.

Fast Function Blocks (FFBs) provide fast, pin-to-pin speed and logic throughput for critical decoding and ultra-fast state machine applications. High-Density Function Blocks (FBs) provide maximum logic density and system-level features to implement complex functions with predictable timing for adders and accumulators, wide functions and state machines requiring large numbers of product terms, and other forms of complex logic.

In addition, the XC7300 architecture employs the Universal Interconnect Matrix (UIM) which guarantees 100% interconnect of all internal functions. This interconnect scheme provides constant, short interconnect delays for all routing paths through the UIM. Constant interconnect delays simplify device timing and guarantee design performance, regardless of logic placement within the chip.

All XC7300 devices are designed in 0.8µ CMOS EPROM technology.

All XC7300 EPLDs include programmable power management features to specify high-performance or low-power operation on an individual Macrocell-by-Macrocell basis. Unused Macrocells are automatically turned off to mini-

The XC7300 Family

	XC7318	XC7336	XC7354	XC7372	XC73108	XC73144
Typical 22V10 Equivalent	1.5 – 2	3 – 4	6	8	12	16
Number of Macrocells	18	36	54	72	108	144
Number of Function Blocks	2	4	6	8	12	16
Number of Flip-Flops	18	36	108	126	198	276
Number of Fast Inputs	12	12	12	12	12	12
Number of Signal Pins	38	38	58	84	120	156

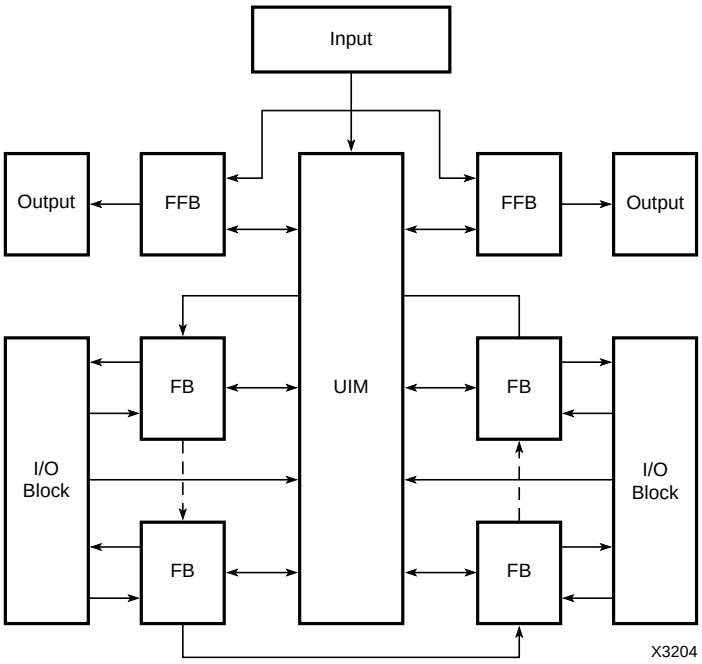

Figure 1. XC7300 Device Block Diagram

mize power dissipation. Designers can operate speed-critical paths at maximum performance, while non-critical paths dissipate less power.

Xilinx development software supports XC7300 EPLD design using third-party schematic entry tools, HDL compilers, or direct equation-based text files. Using a PC or a workstation and one of these design capture methods, designs are automatically mapped to an XC7300 EPLD in a matter of minutes.

The XC7300 devices are available in plastic and ceramic leaded chip carriers, pin-grid-array (PGA), ball-grid-array (BGA), and quad flat pack (QFP) packages. Package options include both windowed ceramic for design prototypes and one-time programmable plastic versions for cost-effective production volume.

Architecture

The XC7300 architecture consists of multiple programmable Function Blocks interconnected by a UIM as shown in Figure 1. The Dual-Block architecture contains two types of function blocks: Fast Function Blocks and High-Density Function Blocks. Both types of function blocks, and the I/O blocks, are interconnected through the UIM.

Fast Function Blocks

The Fast Function Block has 24 inputs which can be individually selected from the UIM, 12 fast input pins, or the nine Macrocell feedbacks from the Fast Function Block. The programmable AND array in each Fast Function Block generates 45 product terms to drive the nine Macrocells in each Fast Function Block. Each Macrocell can be configured for registered or combinatorial logic. See Figure 2.

Five product terms from the programmable AND array are allocated to each Macrocell. Four of these product terms are ORed together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active-High programmable Reset or Set Input to the Macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop, or transparent for combinatorial outputs.

Two fast function block Macrocell differences exist when comparing the XC7336 FFB to the XC7354, XC7372 and XC73108 FFBs.

In the XC7336, five product terms from the programmable AND array are allocated to each Macrocell. Four of these product-terms are OR'd together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product-term drives the asynchronous active High programmable Set or Reset input to the Macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop, or transparent for combinatorial outputs. See Figure 2.

In the XC7354, XC7372 and XC73108, five product terms from the programmable AND array are allocated to each Macrocell. Four of these product-terms are OR'd together, inverted and drive the input of a programmable D-type flip-flop. The fifth product-term drives the asynchronous active High programmable Set input to the Macrocell flip-flop. The flip-flop can be configured as a D-type flip-flop or transparent for combinatorial outputs. See Figure 3.

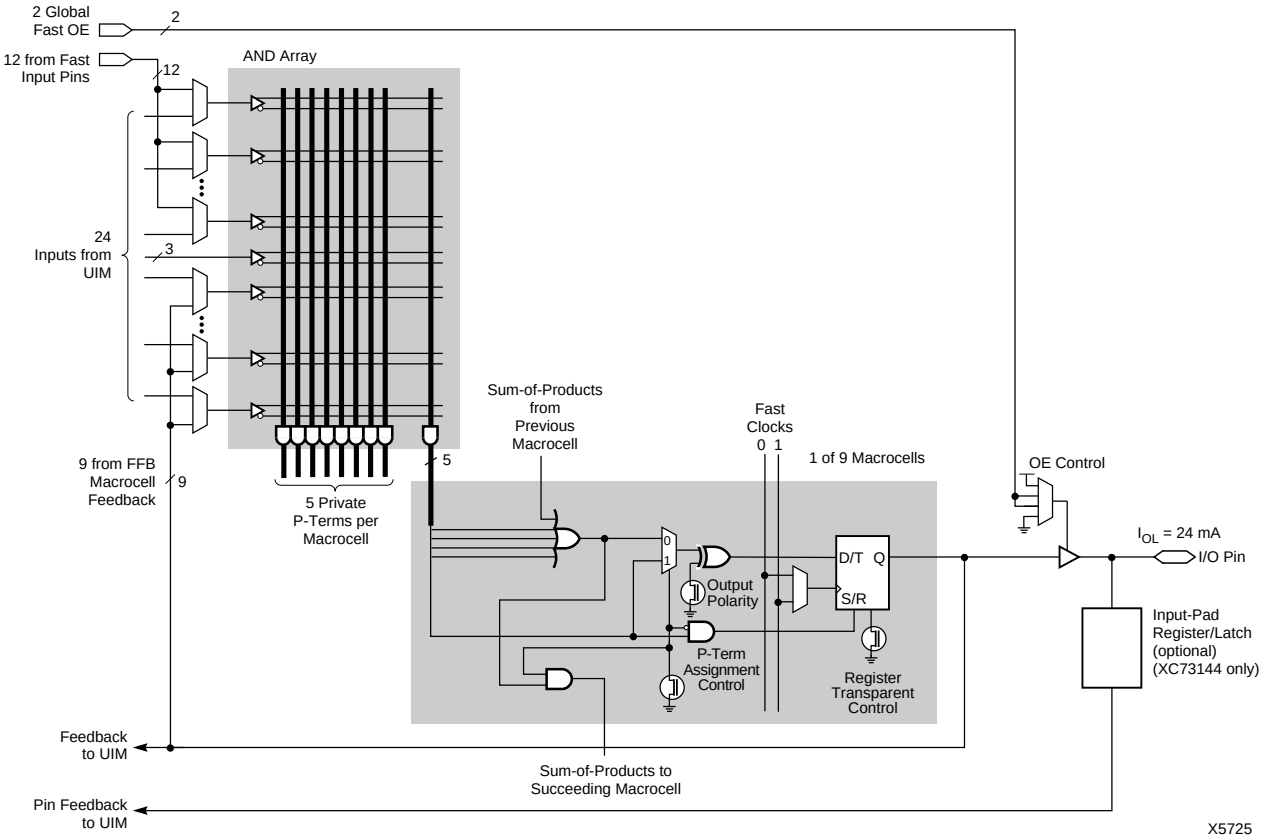

Figure 2. Fast Function Block and Macrocell Schematic for the XC7318, XC7336, and XC73144

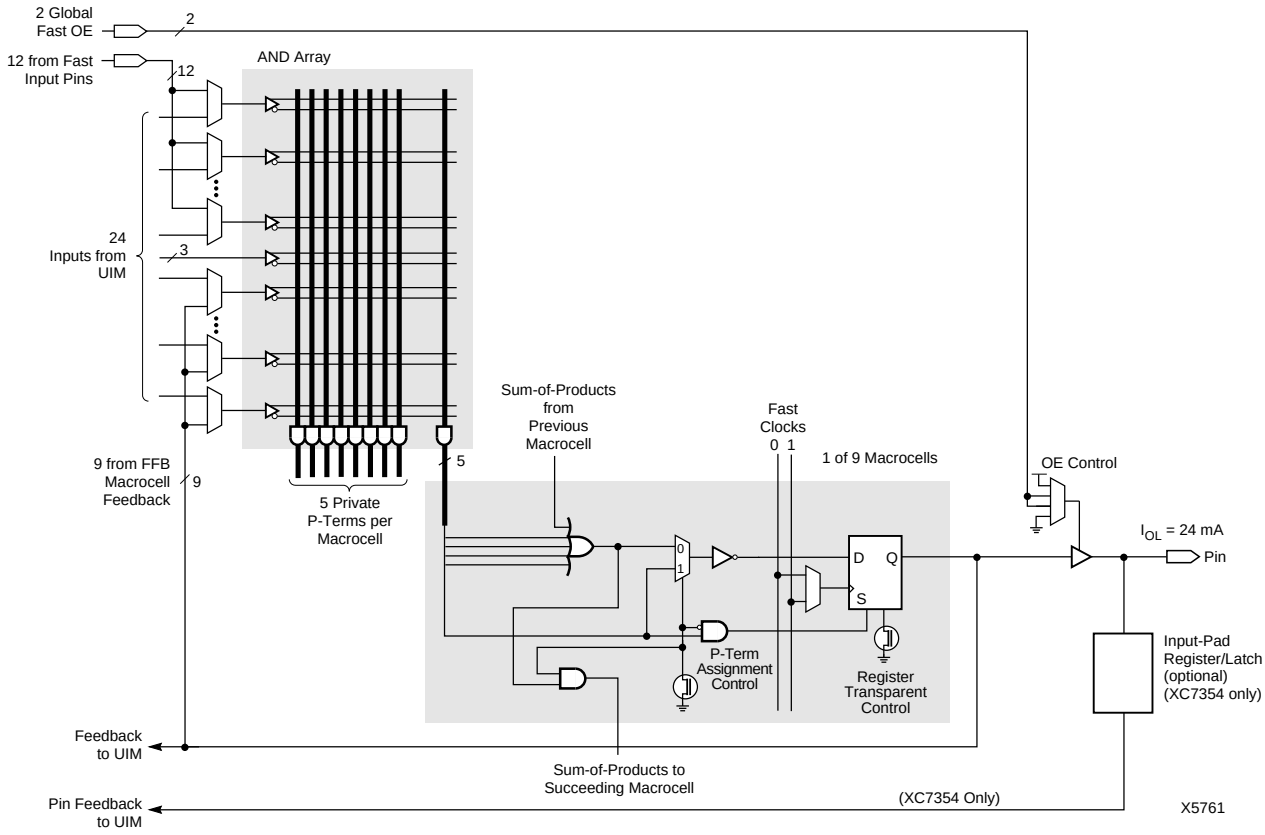

Figure 3. Fast Function Block and Macrocell Schematic for the XC7354, XC7372, and XC73108

The programmable clock source is one of two global Fast-Clock signals (FCLK0 or FCLK1) that are distributed with short delay and minimal skew over the entire chip.

The Fast Function Block Macrocells drive chip outputs directly through 3-state output buffers. Each output buffer can be individually controlled by one of two dedicated Fast Output Enable inputs or permanently enabled or disabled. The Macrocell output can also be routed back as an input to the Fast Function Block and the UIM.

Each Fast Function Block output is capable of sinking 24 mA when V_{CCIO} = 5 volts. These include all outputs on the XC7318 and XC7336 devices and all Fast Outputs (FOs) on the XC7354, XC7372, XC73108, and XC73144 devices.

Unlike other I/Os, the Fast Function Block inputs do not have an input register.

Product Term Assignment

Each Macrocell sum-of-product OR gates can be expanded using the Fast Function Block product term assignment scheme. Product-term assignment transfers product-terms in increments of four product-terms from one Macrocell to the neighboring Macrocell (Figure 4). Complex logic functions requiring up to 36 product-terms can be implemented using all nine Macrocells within the Fast Function Block. When product-terms are assigned to adjacent Macrocells, the product-term normally dedicated to the Set or Reset function becomes the input to the Macrocell register.

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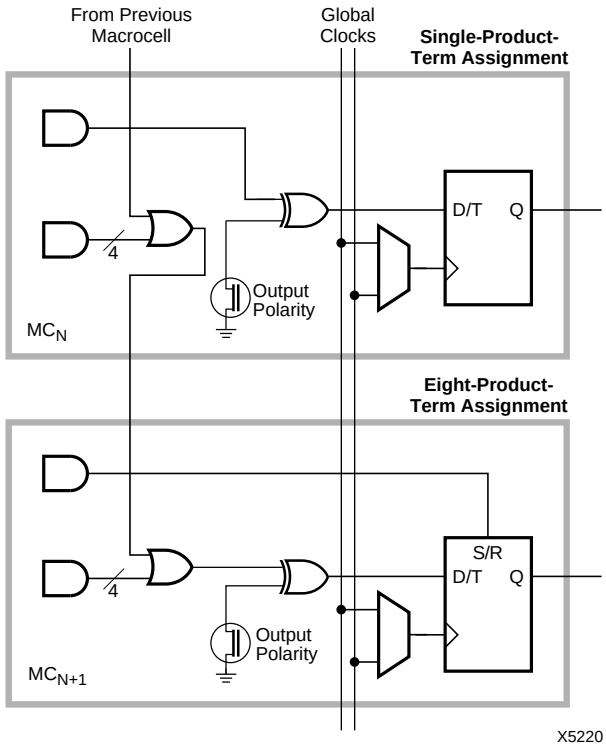


Figure 4. Fast Function Block Product-Term Assignment

High-Density Function Blocks

The XC7354, XC7372, XC73108 and XC73144 devices contain multiple, High-Density Function Blocks linked though the UIM. Each Function Block contains nine Macrocells. Each Macrocell can be configured for either registered or combinatorial logic. A detailed block diagram of the High-Density FB is shown in Figure 5.

Each FB receives 21 signals and their complements from the UIM and an additional three inputs from the Fast Input (FI) pins.

Shared and Private Product Terms

Each Macrocell contains five private product terms that can be used as the primary inputs for combinatorial functions implemented in the Arithmetic Logic Unit (ALU), or as individual Reset, Set, Output-Enable, and Clock logic functions for the flip-flop. Each Function Block also provides an additional 12 shared product terms, which are uncommitted product terms available for any of the nine Macrocells within the Function Block.

Four private product terms can be ORed together with up to four shared product terms to drive the D1 input to the ALU. The D2 input is driven by the OR of the fifth private product term and up to eight of the remaining shared product terms. The shared product terms add no logic delay, and each shared product term can be connected to one or all nine Macrocells in the Function Block.

Arithmetic Logic Unit

The functional versatility of each Macrocell in the High-Density Function Block is enhanced through additional gating and control functions available in the ALU. A detailed block diagram of the XC7300 ALU is shown in Figure 6.

The ALU has two programmable modes; *logic* and *arithmetic*. In logic mode, the ALU functions as a 2-input function generator using a 4-bit look-up table that can be programmed to generate any Boolean function of its D1 and D2 inputs as illustrated in Table 1.

The function generator can OR its inputs, widening the OR function to a maximum of 17 inputs. It can AND them, which means that one sum-of-products can be used to mask the other. It can also XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored.

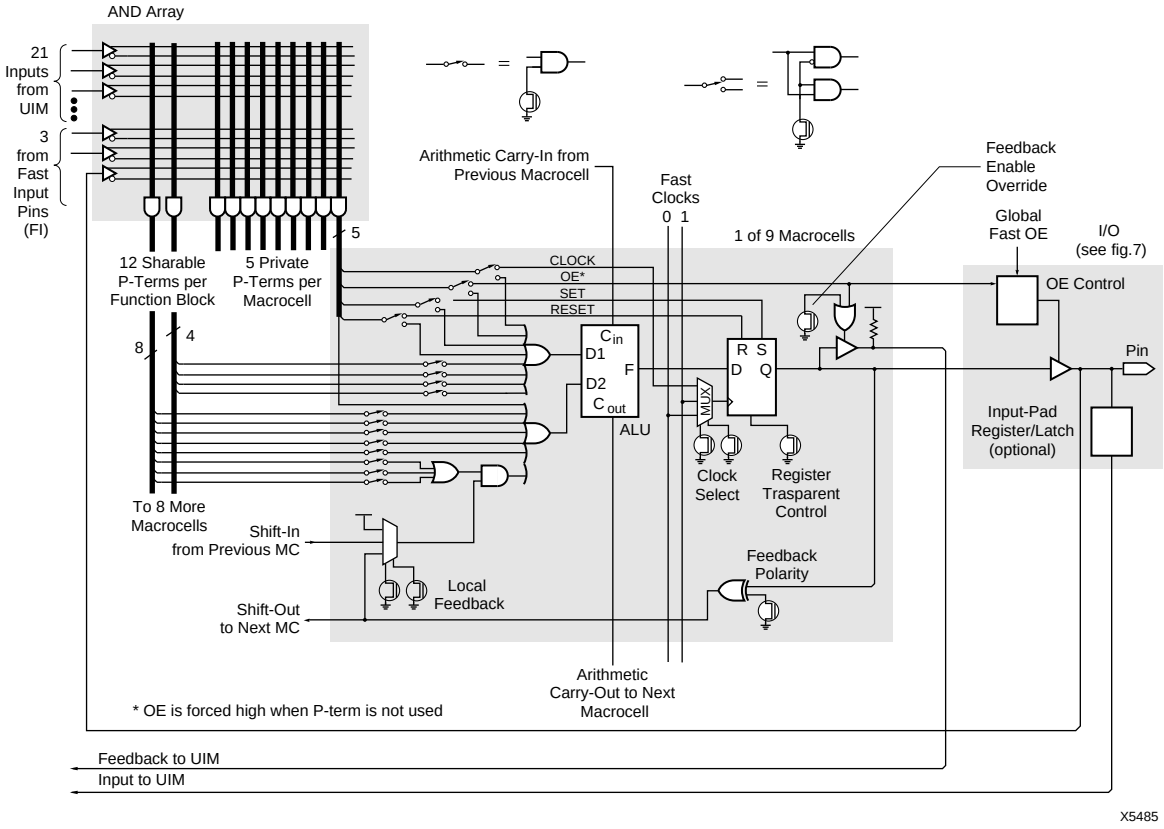


Figure 5. High-Density Function Block and Macrocell Schematic

Table 1. Function Generator Logic Operations

Function	
D1:+: D2	$\overline{D1:+:D2}$
D1 * D2	$\overline{D1 * D2}$
D1 + D2	$\overline{D1 + D2}$
D1	D2
$\overline{D1}$	$\overline{D2}$
D1 * $\overline{D2}$	$\overline{D1}$ * D2
D1 + $\overline{D2}$	$\overline{D1}$ + D2

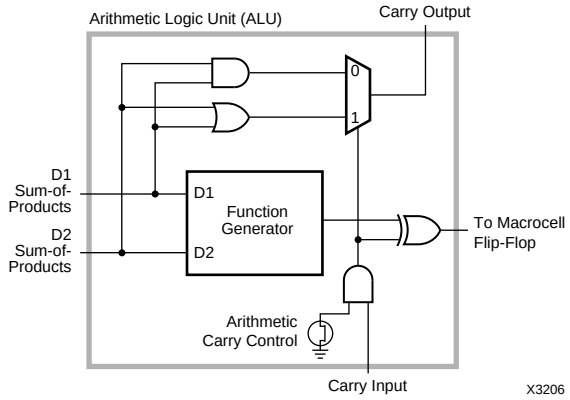


Figure 6. ALU Schematic

Therefore, the ALU can implement one additional layer of logic without any speed penalty.

In arithmetic mode, the ALU block can be programmed to generate the arithmetic sum or difference of the D1 and D2 inputs. Combined with the carry input from the next lower Macrocell, the ALU operates as a 1-bit full adder generating a carry output to the next higher Macrocell. The carry chain propagates between adjacent Macrocells and also crosses the boundaries between Function Blocks. This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture when trying to perform arithmetic functions.

Carry Lookahead

Each Function Block provides a carry lookahead generator capable of anticipating the carry across all nine Macrocells. The carry lookahead generator reduces the ripple-carry delay of wide arithmetic functions such as add, subtract, and magnitude compare to that of the first nine bits, plus the carry lookahead delay of the higher-order Function Blocks.

Macrocell Flip-Flop

The ALU block output drives the input of a programmable D-type flip-flop. The flip-flop is triggered by the rising edge of the clock input, but it can be configured as transparent,

making the Q output identical to the D input, independent of the clock, or as a conventional flip-flop.

The Macrocell clock source is programmable and can be one of the private product terms or one of two global FastCLK signals (FCLK0 and FCLK1). Global FastCLK signals are distributed to every Macrocell flip-flop with short delay and minimal skew.

The asynchronous Set and Reset product terms override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set.

In addition to driving the chip output buffer, the Macrocell output is routed back as an input to the UIM. One private product term can be configured to control the Output Enable of the output buffer and/or the feedback to the UIM. If it is configured to control UIM feedback, the Output Enable product term forces the UIM feedback line High when the Macrocell output is disabled.

Universal Interconnect Matrix

The UIM receives inputs from each Macrocell output, I/O pin, and dedicated input pin. Acting as an unrestricted crossbar switch, the UIM generates 21 output signals to each High-Density Function Block and 24 output signals to each Fast Function Block.

Each UIM input can be programmed to connect to any UIM output. The delay through the interconnect matrix is constant, regardless of the routing distance, fan-out, or fan-in.

When multiple inputs are programmed to be connected to the same output, this output produces the logical AND of the input signals. By choosing the appropriate signal inversions at the input pins, Macrocell outputs and Function Block AND-array input, this AND logic can also be used to implement wide NAND, OR or NOR functions. This offers an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Programming several such Macrocell outputs onto the same UIM output emulates a 3-state bus line. If one of the Macrocell outputs is enabled, the UIM output assumes the enabled output's level.

Input/Output Blocks

Macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. The Macrocell output can be inverted. An additional configuration option allows the output to be disabled permanently. Two dedicated FastOE inputs can also be configured to control any of the chip outputs instead of, or in conjunction with, the individual Output Enable product term. See Figure 7.

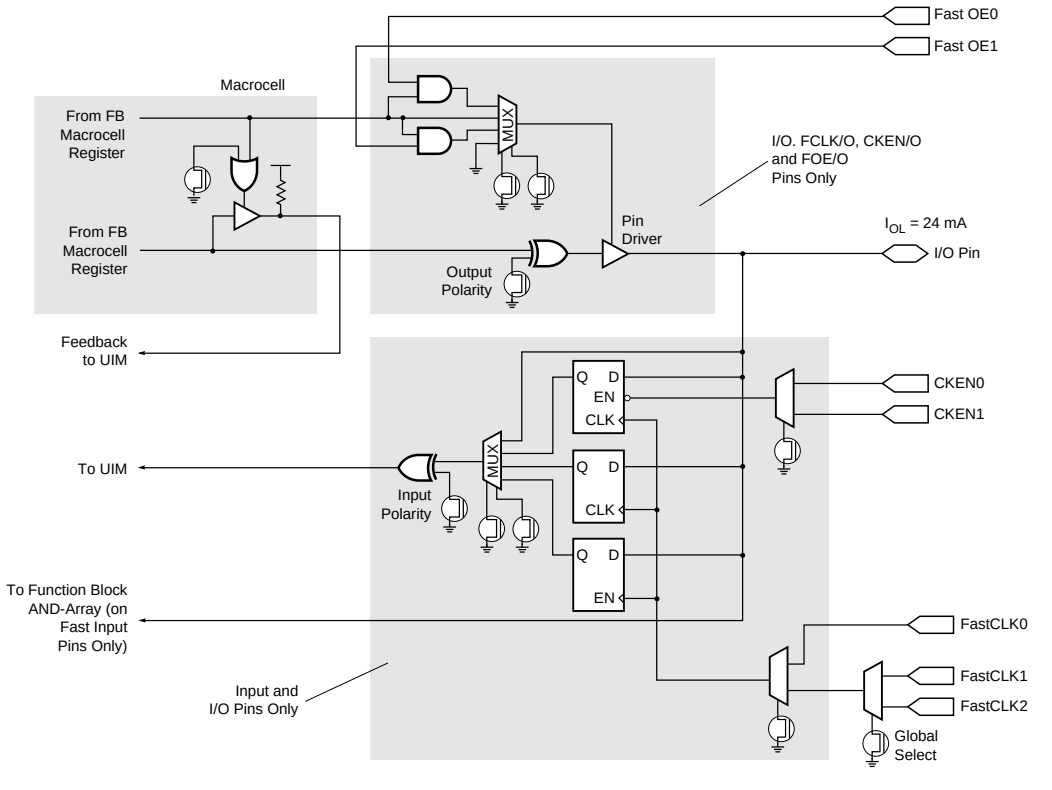


Figure 7. Input/Output Schematic (except XC7318/XC7336 which do not include I/O flip-flops)

Output buffers, except those connected to Fast Function Blocks, can sink 12 mA when V_{CCIO} = 5 V. Fast Function Block outputs can sink 24 mA when V_{CCIO} = 5 V. All outputs on the XC7318 and XC7336 devices connect to FFBs. Outputs listed as Fast Outputs (FO) on the XC7354, XC7372, XC73108 and XC73144 devices connect to FFBs.

Each signal input to the chip is connected to a programmable input structure that can be configured as direct, latched, or registered. The latch and flip-flop can use one of two FastCLK signals as latch enable or clock. The two FastCLK signals are FCLK0 and a global choice of either FCLK1 or FCLK2. Latches are transparent when FastCLK is High, and flip-flops clock on the rising edge of FastCLK. The flip-flop includes an active-low clock enable, which when High, holds the present state of the flip-flop and inhibits response to the input signal. The clock enable source is one of two global Clock Enable signals ($\overline{CE0}$ and $\overline{CE1}$). An additional configuration option is polarity inversion for each input signal.

3.3 V or 5 V Interface Configuration

XC7300 devices can be used in systems with two different supply voltages: 3.3 V and 5 V. Each XC7300 device has separate V_{CC} connections to the internal logic and input buffers (V_{CCINT}) and to the I/O drivers (V_{CCIO}). V_{CCINT} must always be connected to a nominal 5 V supply, while V_{CCIO} may be connected to either 3.3 V or 5 V, depending on the output interface requirement.

When V_{CCIO} is connected to 5 V, the input thresholds are TTL levels, and thus compatible with 3.3 V and 5 V logic. The output High levels are also TTL compatible. When V_{CCIO} is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V rail. This makes the XC7300 ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed so that the I/O can also safely interface to a mixed 3.3 V and 5 V bus.

Power-On Characteristics/Master Reset

The XC7300 device undergoes a short internal initialization sequence upon device powerup. During this time (t_{RESET}), the outputs remain 3-stated while the device is configured from its internal EPROM array and all registers are initialized. If the $\overline{MR}$ pin is tied to V_{CCINT}, the initialization sequence is completely transparent to the user and is completed in t_{RESET} after V_{CCINT} has reached 4.75 V. If $\overline{MR}$ is held low while the device is powering up, the internal initialization sequence begins and outputs will remain 3-stated until the sequence is complete and $\overline{MR}$ is brought High. V_{CC} rise must be monotonic to insure the initialization sequence is performed correctly.

For additional flexibility, the $\overline{MR}$ pin is provided so the EPLD can be reinitialized after power is applied. On the falling edge of $\overline{MR}$, all outputs become 3-stated and the initialization sequence is started. The outputs will remain 3-stated until the internal initialization sequence is complete and $\overline{MR}$ is brought High. The minimum $\overline{MR}$ pulse with is t_{WMR}. If $\overline{MR}$ is brought high after t_{WMR}, but before t_{RESET}, the outputs will become active after t_{RESET}.

During the initialization sequence, all input registers or latches are preloaded High and all FB and FFB Macrocell registers are preloaded to a known state. For FFB Macrocell registers where the Set/Reset product-term is defined, the preload is accomplished by asserting the product-term shortly before the end of the initialization sequence. When the Set/Reset product-term is defined and configured as Reset, the register preload value is Low. When the Set/Reset product-term is defined and configured as a Set, the register preload value is High. For FFB Macrocell registers where the Set/Reset product-term is not used, the register preload value is High.

For FB Macrocell registers, the preload value is defined by a separate preload configuration bit, independent of the Set and Reset product-terms. The value of this preload configuration bit is determined by the schematic capture library or in the user's design. If not specified, the register preload value is Low.

Power Management

The XC7300 family of devices feature a power-management scheme which permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a small part is speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To further reduce power dissipation, unused Function Blocks are turned off and unused Macrocells in used Function Blocks are configured for low power operation.

Erasure Characteristics

In windowed packages, the content of the EPROM array can be erased by exposure to ultraviolet light of wavelengths of approximately 4000 Å. The recommended erasure time is approximately 1 hr. when the device is placed within 1 in. of an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. To prevent unintentional exposure, place opaque labels over the device window.

When the device is exposed to high intensity UV light for much longer periods, permanent damage can occur. The

maximum integrated dose the XC7300 EPLD can be exposed to without damage is 7000 W • s/cm^2, or approximately one week at 12,000 μW/cm^2.

Design Recommendations

For proper operation, all unused input and I/O pins must be connected to a valid logic level (High or Low). The recommended decoupling for all V_{CC} pins should total 1 μF using high-speed (tantalum or ceramic) capacitors.

Use electrostatic discharge (ESD) handling procedures with the XC7300 EPLDs to prevent damage to the device during programming, assembly, and test.

Design Security

Each member of the XC7300 family has a multibit security system that controls access to the configuration programmed into the device. This security scheme uses multiple EPROM bits at various locations within the EPROM array to offer a higher degree of design security than other EPROM and fused-based devices. Programmed data within EPROM cells is invisible–even when examined under a microscope–and cannot be selectively erased. The EPROM security bits, and the device configuration data, reset when the device is erased.

High-Volume Production Programming

The XC7300 family offers flexibility for low-volume prototypes as well as cost-effectiveness for high-volume production. The designer can start with ceramic window package parts for prototypes, ramp up initial production using low-cost plastic parts programmed in-house, and then shift into high-volume production using Xilinx factory programmed and tested devices.

The Xilinx factory programmed concept offers significant advantages over competitive masked PLDs, or ASIC redesigns:

- No redesign is required – Even though masked devices are advertised as timing compatible, subtle differences in a chip layout can mean system failure.
- Devices are factory tested – Factory-programmed devices are tested as part of the manufacturing flow, insuring high-quality products.
- Shipments are delivered fast – Production shipments can begin within a few weeks, eliminating masking delays and qualification requirements.

For factory programming procedures, contact your local Xilinx representative.

XEPLD Development System

The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD Development System. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions, or as a mixture of both. The XEPLD translator maps the design quickly and automatically onto a chosen EPLD device, produces documentation for design analysis and creates a programming file to configure the device.

The following lists some of the XEPLD Development System features.

- Familiar design approach similar to TTL and PLD techniques
- Converts netlist to fuse map in minutes using a ’486 PC or workstation platform
- Interfaces to standard third-party CAE schematics, simulation tools, and behavioral languages
- Schematic library with familiar and powerful TTL-like components, including PLDs and ALUs
- Predictable timing even before design entry, using library components and Boolean equations

Timing simulation using Viewsim, OrCAD VST, and other tools controlled by the Xilinx Design Manager (XDM) program

Timing Model

Timing within the XC7300 EPLDs is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 8.

The timing model is based on the fixed internal delays of the XC7300 architecture which consists of four basic parts: I/O Blocks, the UIM, Fast Function Blocks and High-Density Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for a particular EPLD.

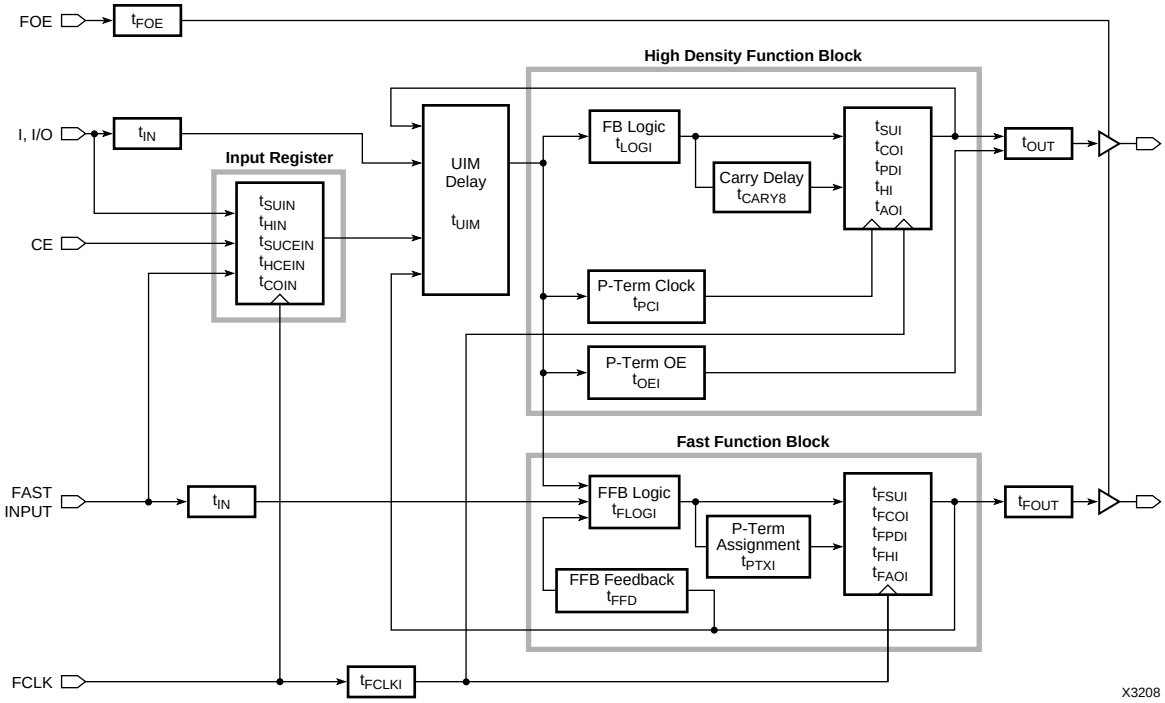
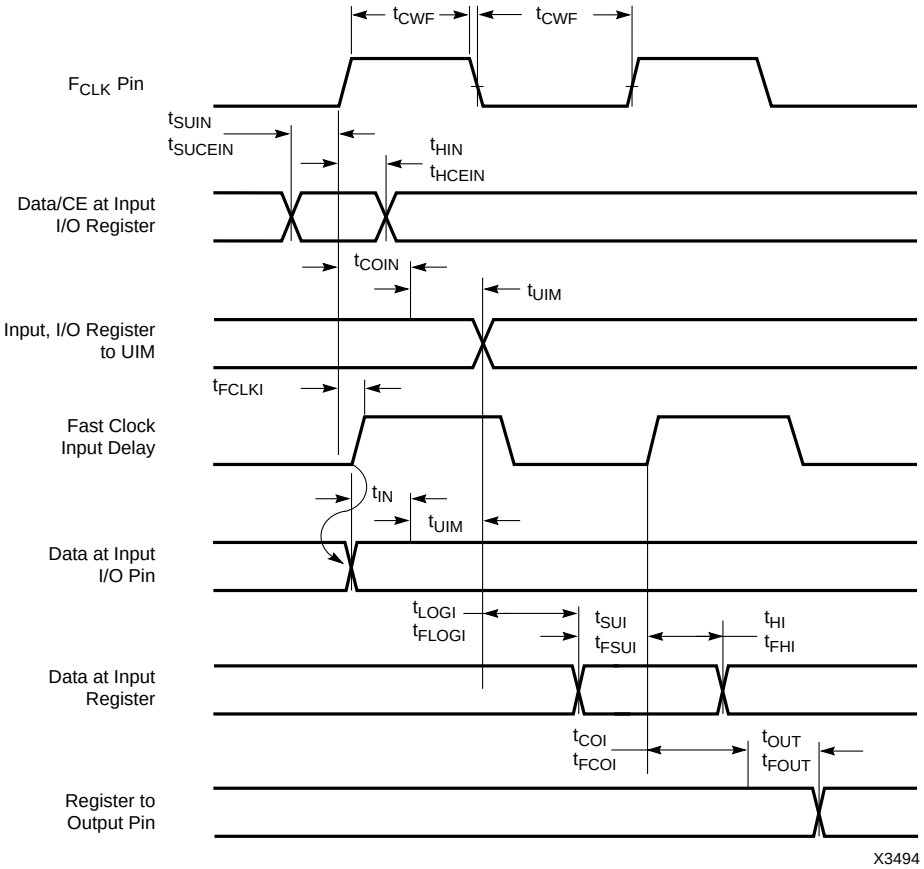
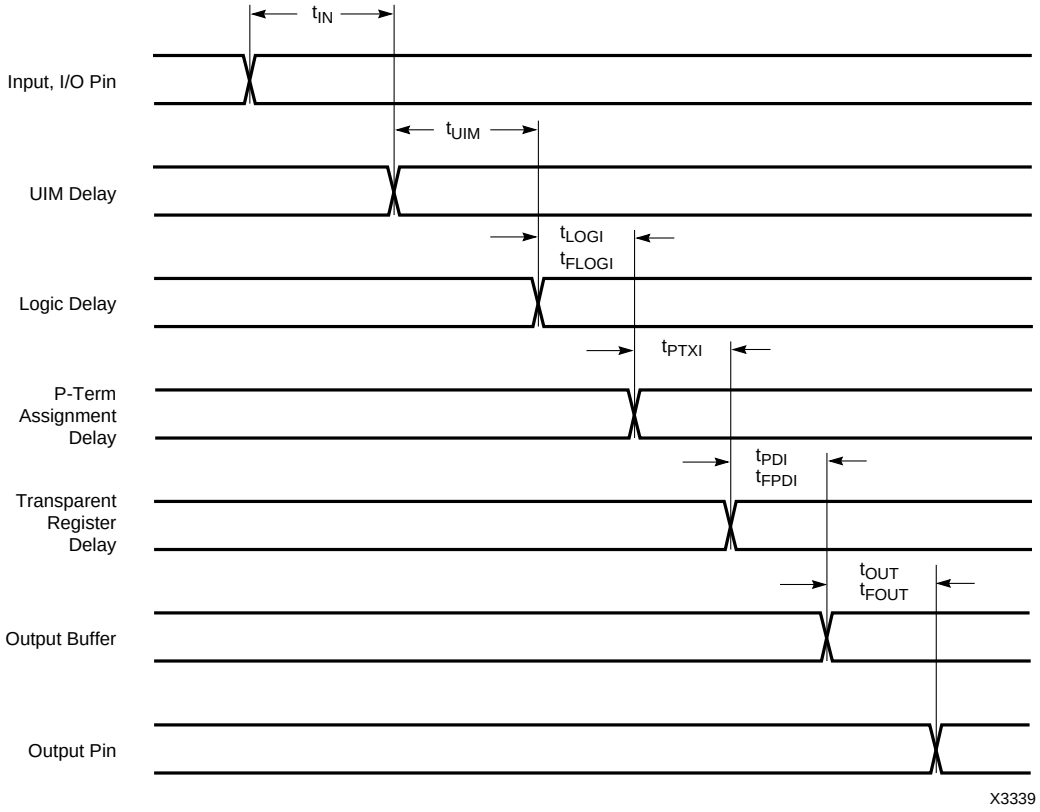


Figure 8. XC7300 Timing Model

Synchronous Clock Switching Characteristics



Combinatorial Switching Characteristics



Asynchronous Clock Switching Characteristics