



XCR3064XL 64 Macrocell CPLD

DS017 (v1.1) August 30, 2000

Preliminary Product Specification

Features

- 6.0 ns pin-to-pin logic delays
- System frequencies up to 145 MHz
- 64 macrocells with 1,500 usable gates
- Available in small footprint packages
 - 44-pin VQFP (36 user I/O pins)
 - 48-ball CS BGA (40 user I/O pins)
 - 56-ball CP BGA (48 user I/O pins)
 - 100-pin TQFP (68 user I/O pins)
- Optimized for 3.3V systems
 - Ultra-low power operation
 - 5V tolerant I/O pins with 3.3V core supply
 - Advanced 0.35 micron five metal layer reprogrammable process
 - FZP™ CMOS design technology
- Advanced system features
 - In-system programming
 - Input registers
 - Predictable timing model
 - Up to 23 available clocks per logic block
 - Excellent pin retention during design changes
 - Full IEEE Standard 1149.1 boundary-scan (JTAG)
 - Four global clocks
 - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for dual function of JTAG ISP pins
- 2.7V to 3.6V industrial temperature range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (DS012) for architecture description

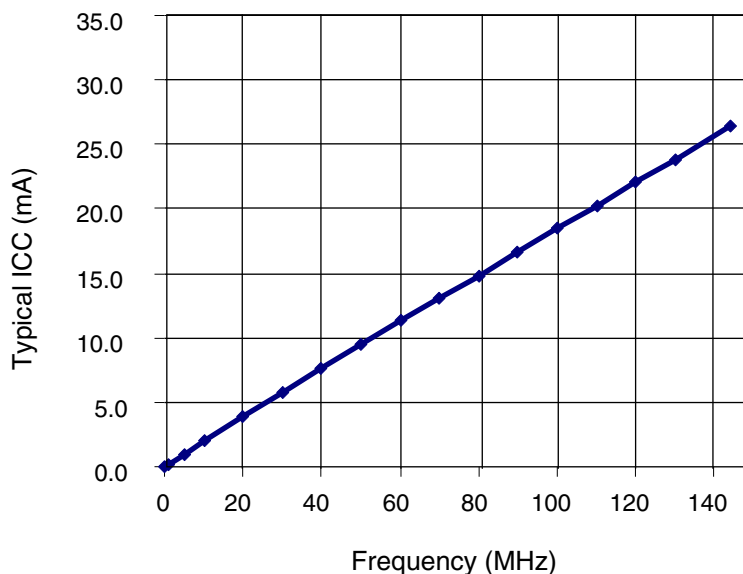
Description

The XCR3064XL is a 3.3V, 64-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of four logic blocks provide 1,500 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 145 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to [Figure 1](#) and [Table 1](#) showing the I_{CC} vs. Frequency of our XCR3064XL TotalCMOS CPLD (data taken with four up/down, loadable 16-bit counters at 3.3V, 25°C).





DS017_01_082800

Figure 1: I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°CTable 1: I_{CC} vs. Frequency (V_{CC} = 3.3V, 25°C)

Frequency (MHz)	0	1	5	10	20	40	60	80	100	120	140
Typical I _{CC} (mA)	0	0.2	1.0	2.0	3.9	7.6	11.3	14.8	18.5	22.1	25.6

DC Electrical Characteristics Over Recommended Operating Conditions⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output High voltage for 3.3V outputs	I _{OH} = -8 mA	2.4	-	V
V _{OL}	Output Low voltage for 3.3V outputs	I _{OL} = 8 mA	-	0.4	V
I _{IL}	Input leakage current	V _{IN} = GND or V _{CC}	-10	10	μA
I _{IH}	I/O High-Z leakage current	V _{IN} = GND or V _{CC}	-10	10	μA
I _{CCSB}	Standby current	V _{CC} = 3.6V	-	100	μA
I _{CC}	Dynamic current ^(2,3)	f = 1 MHz	-	0.5	mA
		f = 50 MHz	-	15	mA
C _{IN}	Input pin capacitance ⁽⁴⁾	f = 1 MHz	-	8	pF
C _{CLK}	Clock input capacitance ⁽⁴⁾	f = 1 MHz	-	12	pF
C _{I/O}	I/O pin capacitance ⁽⁴⁾	f = 1 MHz	-	10	pF

Notes:

1. See XPLA3 family data sheet (DS012) for recommended operating conditions.
2. See [Table 1](#), Figure1 for typical values.
3. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
4. Typical values not tested.

AC Electrical Characteristics Over Recommended Operating Conditions^(1,2)

Symbol	Parameter	-6		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T _{PD1}	Propagation delay time (single p-term)	-	5.5	-	7.0	-	9.1	ns
T _{PD2}	Propagation delay time (OR array) ⁽³⁾	-	6.0	-	7.5	-	10.0	ns
T _{CO}	Clock to output (global synchronous pin clock)	-	4.0		5.0	-	6.5	ns
T _{SUF}	Setup time fast	2.0	-	2.5	-	3.0	-	ns
T _{SU}	Setup time	4.0	-	4.8	-	6.3	-	ns
T _H	Hold time	0	-	0	-	0	-	ns
T _{WLH}	Global Clock pulse width (High or Low)	2.5	-	3.0	-	4.0	-	ns
T _{tPLH}	P-term clock pulse width	4.0	-	5.0	-	6.0	-	ns
T _R	Input rise time	-	20	-	20	-	20	ns
T _L	Input fall time	-	20	-	20	-	20	ns
f _{SYSTEM}	Maximum system frequency	-	145	-	119	-	95	MHz
T _{CONFIG}	Configuration time ⁽⁴⁾	-	20.0	-	20.0	-	20.0	μs
T _{POE}	P-term OE to output enabled	-	7.5	-	9.3	-	11.2	ns
T _{POD}	P-term OE to output disabled ⁽⁵⁾	-	7.5	-	9.3	-	11.2	ns
T _{PCO}	P-term clock to output	-	6.5	-	8.3	-	10.7	ns
T _{PAO}	P-term set/reset to output valid	-	8.0	-	9.3	-	11.2	ns

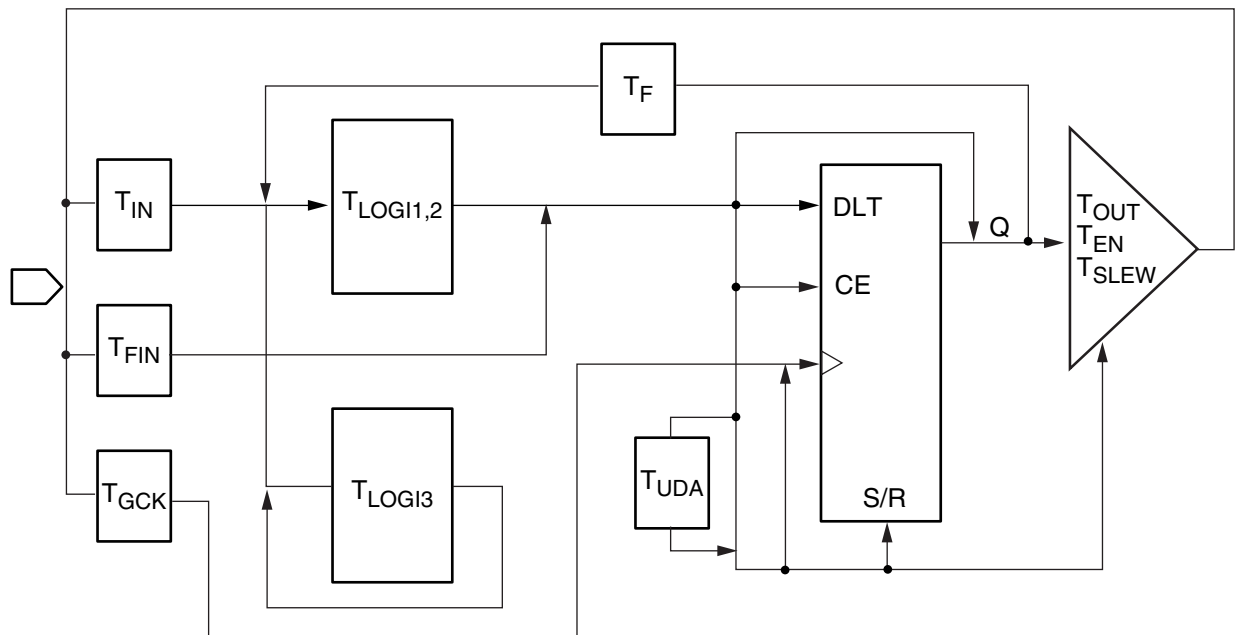
Notes:

1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (DS012) for recommended operating conditions.
3. See [Figure 4](#) for derating.
4. Typical current draw during configuration is 8 mA at 3.6V.
5. Output C_L = 5 pF.

Timing Model

The XPLA3 architecture follows a simple timing model that allows deterministic timing in design and redesign. The basic timing model is shown in **Figure 2**. One key feature of the XPLA3 CPLD is the ability to have up to 48 product term inputs into a single macrocell and maintain consistent timing. This is achieved through the use of a fully populated PLA (Programmable AND Programmable OR Array) which also has the ability to share product terms and only use the required amount of product terms per macrocell. There is a fast path (T_{LOGI1}) into the macrocell which is used if there is

a single product term. The T_{LOGI2} path is used for multiple product term timing. For optimization of logic, the XPLA3 CPLD architecture includes a Fold-back NAND path (T_{LOGI3}). There is a fast input path to each macrocell if used as an Input Register (T_{FIN}). XPLA3 also includes universal control terms (T_{UDA}) that can be used for synchronization of the macrocell registers in different logic blocks. There is also slew rate control and output enable control on a per macrocell basis.



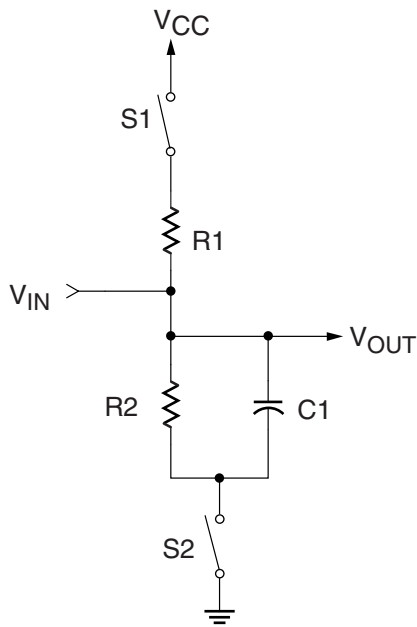
DS017_02_042800

Figure 2: XPLA3 Timing Model

Internal Timing Parameters

Symbol	Parameter	-6		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.3	-	1.6	-	2.2	ns
T_{FIN}	Fast Input buffer delay	-	1.8	-	2.5	-	3.1	ns
T_{GCK}	Global Clock buffer delay	-	0.8	-	1.0	-	1.3	ns
T_{OUT}	Output buffer delay	-	2.2	-	2.7	-	3.6	ns
T_{EN}	Output buffer enable/disable delay	-	4.2	-	5.0	-	5.7	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	
T_{SUI}	Register setup time	1.0	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	4.0	-	5.5	-	6.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.5	-	2.3	-	2.1	ns
T_{RAI}	Register async. recovery	-	4.0	-	5.0	-	6.0	ns
T_{LOG1}	Internal logic delay (single p-term)	-	2.0	-	2.7	-	3.3	ns
T_{LOG2}	Internal logic delay (PLA OR term)	-	2.5	-	3.2	-	4.2	ns
Feedback Delays								
T_F	ZIA delay	-	2.4	-	2.9	-	3.5	ns
Time Adders								
T_{LOG3}	Fold-back NAND delay	-	6.0	-	7.5	-	9.5	ns
T_{UDA}	Universal delay	-	1.5	-	2.0	-	2.5	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

Switching Characteristics



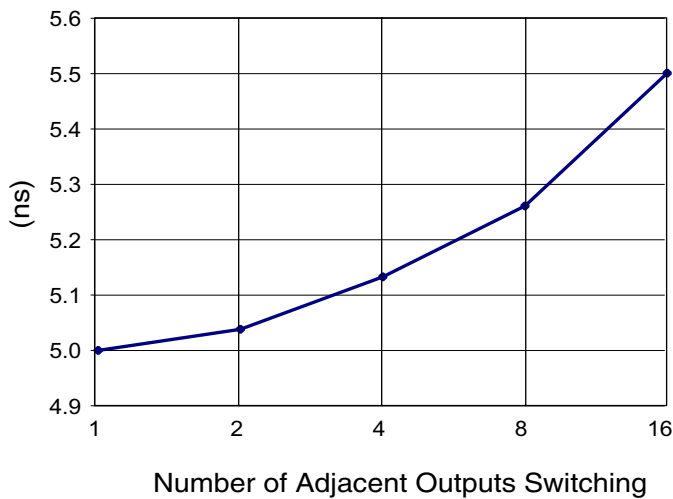
Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T _{POE} (High)	Open	Closed
T _{POE} (Low)	Closed	Open
T _P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF

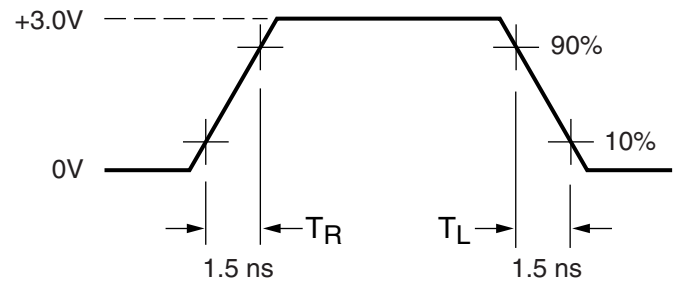
DS017_03_050200

Figure 3: AC Load Circuit



DS017_04_042800

Figure 4: Derating Curve for T_{PD2}



Measurements:

All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS017_05_042800

Figure 5: Voltage Waveform

Pin Descriptions

Table 2: XCR3064XL Pin Descriptions

Function Block	Macrocell	VQ44	CS48	CP56	VQ100
A	0	35	C5	C8	85
A	1	34	A6	A8	84
A	2	-	-	-	83
A	3	-	-	A9	81
A	4	-	-	A5	80
A	5	-	A7	A10	79
A	6	-	-	-	76
A	7	33	B6	B10	75
A	8	32 ⁽¹⁾	B7 ⁽¹⁾	C10 ⁽¹⁾	73 ⁽¹⁾
A	9	31	D4	D8	71
A	10	30	C6	E8	69
A	11	-	-	-	68
A	12	-	-	-	67
A	13	28	D6	F8	65
A	14	27	D7	E10	64
A	15	-	-	-	63
B	0	42	A2	C4	92
B	1	43	A1	C3	93
B	2	44	C4	A1	94
B	3	-	-	-	96
B	4	-	-	B1	97
B	5	-	-	-	98
B	6	-	-	A2	99
B	7	-	B2	A3	100
B	8	1 ⁽¹⁾	B1 ⁽¹⁾	C1 ⁽¹⁾	4 ⁽¹⁾
B	9	2	C2	D1	6
B	10	3	C1	D3	8
B	11	-	-	-	9
B	12	-	-	-	10
B	13	5	D3	E3	12
B	14	6	D1	F1	13
B	15	-	-	-	14
C	0	26 ⁽¹⁾	E5 ⁽¹⁾	F10 ⁽¹⁾	62 ⁽¹⁾

Table 2: XCR3064XL Pin Descriptions (Continued)

Function Block	Macrocell	VQ44	CS48	CP56	VQ100
C	1	25	E7	G8	61
C	2	-	-	-	60
C	3	23	F7	H10	58
C	4	-	-	-	57
C	5	-	-	-	56
C	6	-	F6	K8	54
C	7	-	-	K10	52
C	8	22	G7	K9	48
C	9	21	G6	J10	47
C	10	20	F5	H8	46
C	11	19	G5	H7	45
C	12	18	F4	H6	44
C	13	-	-	-	42
C	14	-	-	K7	41
C	15	-	-	-	40
D	0	40 ⁽¹⁾	D2 ⁽¹⁾	G1 ⁽¹⁾	15 ⁽¹⁾
D	1	8	E1	F3	16
D	2	-	-	-	17
D	3	10	F1	G3	19
D	4	11	G1	J1	20
D	5	-	-	-	21
D	6	-	-	-	23
D	7	-	-	K1	25
D	8	12	E4	K4	29
D	9	13	F2	K2	30
D	10	14	G2	K3	31
D	11	15	F3	H3	32
D	12	-	G3	H4	33
D	13	-	-	-	35
D	14	-	-	K5	36
D	15	-	-	-	37

Notes:

1. JTAG pins

Table 3: X36CR3064XL Global, JTAG, Port Enable, Power, and No connect Pins

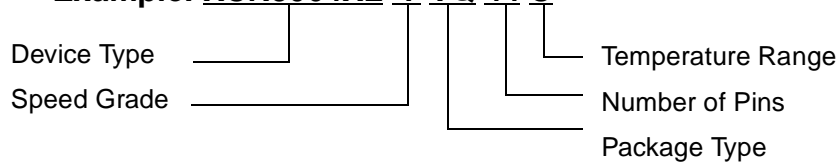
Pin Type	VQ44	CS48	CP56	VQ100
IN0 / CLK0	40	A3	C5	90
IN1 / CLK1	39	B4	C6	89
IN2 / CLK2	38	A4	C7	88
IN3 / CLK3	37	B5	A6	87
TCK	26	E5	F10	62
TDI	1	B1	C1	4
TDO	32	B7	C10	73
TMS	7	D2	G1	15
PORT_EN	4 ⁽¹⁾	C3 ⁽¹⁾	E1 ⁽¹⁾	11 ⁽¹⁾
V _{CC}	9, 17, 29, 41	B3, C7, E2, G4	A4, D10, H1, H5	3, 18, 34, 39, 51, 66, 82, 91
GND	16, 24, 36	A5, E3, E6	A7, G10, K6	26, 38, 43, 59, 74, 86, 95
No Connects	-	-	-	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78

Notes:

1. Port Enable is brought Low to enable JTAG pins when JTAG pins are used as I/O. See family data sheet for more information.

Ordering Information

Example: **XCR3064XL -7 VQ 44 C**



Speed Options

- 10: 10 ns pin-to-pin delay
- 7: 7.5 ns pin-to-pin delay
- 6: 6.0 ns pin-to-pin delay

Temperature Range

- C = Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$
- I = Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Packaging Options

- VQ100: 100-pin Very Thin Quad Flat Package
- VQ44: 44-pin Very Thin Quad Flat Package
- CS48: 48-ball Chip Scale Package
- CP56: 56-ball Chip Scale Package

Component Availability

Pins		100	56	48	44
Type		Plastic VQFP	Plastic BGA	Plastic BGA	Plastic VQFP
Code		TQ100	CP56	CS48	VQ44
XCR3064XL	-6	C	C	C	C
	-7, -10	C,I	C,I	C,I	C,I

Revision History

The following table shows the revision history for this document..

Date	Version	Revision
06/01/00	1.0	Initial Xilinx release.
08/30/00	1.1	Added 48-ball CS BGA package.