

DS119-1 (v1.1) October 18, 2004

Features

- Guaranteed to meet full electrical specifications over T_A = -40°C to +125°C
- Technology: 0.35 µm EEPROM process
- Full Boundary Scan Test (IEEE 1149.1) for flexible in-system device and system testing
- Fast program ming times in production saves time and money
 - Increases system reliability through reduced device handling
- High-speed pin-to-pin delays of 10 ns (100 MHz)
- Slew rate control per output to reduce EMI
- 100% routable which enables all device resources to be utilized
- Refer to XPLA3 Family data sheet (DS012) for architecture description
- Refer to XCR3064XL data sheet (DS017) for pin descriptions

Description

The CoolRunner[™] XCR3064XL-Q CPLD Automotive IQ product is targeted for low power systems that include portable, handheld, automotive, and power sensitive applications. This device includes Fast Zero Power[™] (FZP) design technology that combines low power and high speed. With this design technique, the XCR3064XL-Q delivers low standby current without the need for "turbo bits" or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any other CPLD. CoolRunner devices are the only TotalCMOS PLDs, as they use both a CMOS process technology and the patented full CMOS FZP design technique.

The CoolRunner XCR3064XL-Q employs a full PLA structure for logic allocation within a functon block. The PLA provides maximum flexibility and logic density, with superior pin locking capability, while maintaining deterministic timing.

Advance Product Specification

Automotive IQ CPLD

XCR3064XL 64 Macrocell

The CoolRunner XCR3064XL-Q is supported by Web-PACK[™] and WebFITTER[™] from Xilinx and industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, ViewLogic, and Synplicity), using text (ABEL, VHDL, Verilog) and schematic capture design entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms.

The XCR3064XL-Q features also include industry-standard, IEEE 1149.1, JTAG interface through which boundary-scan testing and In-System Programming (ISP) and reprogramming of the device can occur. This device is electrically reprogrammable using industry standard device programmers. .

Table 1: CoolRunner XCR3064XL-Q

	XCR3064XL-Q
Macrocells	64
Usable Gates	1,500
Registers	64
F _{SYSTEM} (MHz)	95
User I/O (44-pin VQFP)	36
User I/O (100-pin VQFP)	68

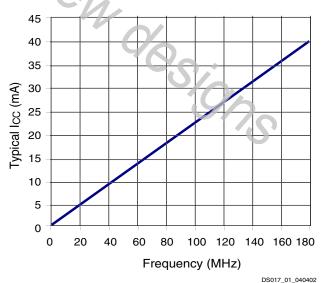


Figure 1: I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C

Table 2: I_{CC} vs. Frequency ($V_{CC} = 3.3V, 25^{\circ}C$)

Frequency (MHz)	0	1	5	10	20	40	60	80	100	120	140	160	180
Typical I _{CC} (mA)	0.02	0.24	1.09	2.15	4.28	8.50	12.85	16.80	20.80	25.72	29.89	33.53	36.27

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Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply voltage ⁽²⁾ relative to GND	-0.5	4.0	V
VI	Input voltage ⁽³⁾ relative to GND	-0.5	5.5 ⁽⁴⁾	V
I _{OUT}	Output current, per pin	-100	100	mA
TJ	Maximum junction temperature	-40	150	°C
T _{STR}	Storage temperature	-65	150	°C

Notes:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.

- 2. The chip supply voltage must rise monotonically.
- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the З. device pins may uncershoot to -2.0V or overshoot to 7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
- 4. External I/O voltage may not exceed V_{CC} by 4.0V.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
T _A	Ambient temperature	-40	+125	°C
V _{CC}	Supply voltage	3.0	3.6	V
V _{IL}	Low-level input voltage	0	0.8	V
V _{IH}	High-level input voltage	2.0	5.5	V
V _O	Output voltage	0	V _{CC}	V
T _R	Input rise time	1, -	20	ns
T _F	Input fall time	· · ·	20	ns
Quality	and Reliability Characteristics	29		

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T _{DR}	Data retention	20	97	Years
N _{PE}	Program/erase cycles (Endurance) @ T _A = 70°C	10,000	-	Cycles

DC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V _{OH} ⁽¹⁾	Output High voltage	$I_{OH} = -500 \ \mu A$ $V_{CC} = 3.0V, \ I_{OH} = -8 \ m A$		90%V _{CC} ⁽²⁾	-	V
				2.4	-	V
V _{OL}	Output Low voltage		I _{OL} = 8 mA	-	0.4	V
I _{IL} (3)	Input leakage current		$V_{IN} = GND \text{ or } V_{CC}$	-10	10	μA
I _{IH} (3)	I/O High-Z leakage current		$V_{IN} = GND \text{ or } V_{CC}$	-10	10	μA
I _{CCSB}	Standby current		V _{CC} = 3.6V	-	5.0	mA
I _{CC}	Dynamic current ⁽⁴⁾		f = 1 MHz	-	6.0	mA
		-	f = 50 MHz	-	20	mA
C _{IN}	Input pin capacitance ⁽⁵⁾		f = 1 MHz	-	8	pF
C _{CLK}	Clock input capacitance ⁽⁵⁾		f = 1 MHz	-	12	pF
C _{I/O}	I/O pin capacitance ⁽⁵⁾		f = 1 MHz	-	10	pF

Notes:

1. See Figure 2 for output drive characteristics of the XPLA3 family.

2. This parameter guaranteed by design and characterization, not by testing.

3. Typical leakage current is less than 1 µA.

4. This parameter measured with a 16-bit, rese able up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.

5. Typical values, not tested.

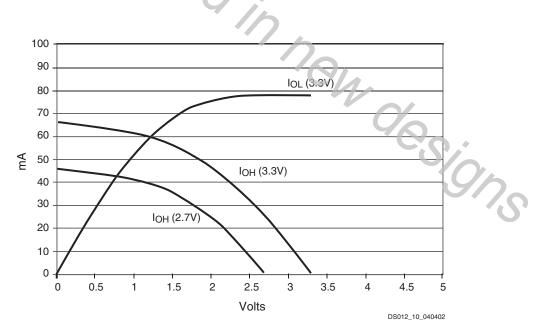


Figure 2: Typical I/V Curve for the XPLA3 Family, 3.3V, 25°C

AC Electrical Characteristics Over Recommended Operating Conditions⁽¹⁾

SymbolParameter T_{PD1} Propagation delay time (single p-term) T_{PD2} Propagation delay time (OR array) T_{CO} Clock to output (global synchronous pin clock) T_{SUF} Setup time (fast input register) $T_{SU1}^{(2)}$ Setup time (single p-term) T_{SU2} Setup time (OR array) $T_{H}^{(2)}$ Hold time $T_{WLH}^{(2)}$ Clobal Clock pulse width (High or Low) $T_{PLH}^{(2)}$ P-term clock pulse width $T_{R1}^{(2)}$ Input rise time $T_{L}^{(2)}$ Input rise time $T_{L}^{(2)}$ Input fall time $f_{SYSTEM}^{(2)}$ Configuration time ⁽³⁾ T_{NIT} ISP initialization time $T_{POE}^{(2)}$ P-term OE to output enabled $T_{POO}^{(2)}$ P-term Clock to output $T_{POC}^{(2)}$ P-term Clock to output $T_{POC}^{(2)}$ P-term OE to output validNotes:1. Specifications measured with one output switching.2. These parameters guaranteed by design and/or characterization, not testing.3. Typical current draw during configuration is 3 mA at 3.6V.4. Output $C_L = 5 pF.$	-	-10	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Min.	Max.	Unit
T_{CO}Clock to output (global synchronous pin clock)T_{SUF}Setup time (fast input register)T_{SU1}^{(2)}Setup time (single p-term)T_{SU2}Setup time (OR array)T_H^{(2)}Hold timeT_{WLH}^{(2)}Clobal Clock pulse width (High or Low)T_{PLH}^{(2)}P-term clock pulse width (High or Low)T_{R}^{(2)}Input rise timeT_{(2)}Input rise timeT_{(2)}Input fall timefsystem ⁽²⁾ Configuration time ⁽³⁾ T_INITISP initialization timeT_{POE}^{(2)}P-term OE to output disabled ⁽⁴⁾ T_{PCO}^{(2)}P-term clock to outputT_{PAO}^{(2)}P-term set/reset to output valid	-	9.1	ns
T_{SUF} Setup time (fast input register) $T_{SU1}^{(2)}$ Setup time (single p-term) T_{SU2} Setup time (OR array) $T_{H}^{(2)}$ Hold time $T_{WLH}^{(2)}$ Clobal Clock pulse width (High or Low) $T_{PLH}^{(2)}$ P-term clock pulse width $T_{R}^{(2)}$ Input rise time $T_{L}^{(2)}$ Input fall time $f_{SYSTEM}^{(2)}$ Maximum system frequency $T_{CONFIG}^{(2)}$ Configuration time (3) T_{NIT} ISP initialization time $T_{POE}^{(2)}$ P-term OE to output enabled $T_{POD}^{(2)}$ P-term clock to output $T_{PAO}^{(2)}$ P-term set/reset to output validNotes:Notes:	-	10.0	ns
$T_{SU1}^{(2)}$ Setup time (single p-term) T_{SU2} Setup time (OR array) $T_{H}^{(2)}$ Hold time $T_{WLH}^{(2)}$ Clobal Clock pulse width (High or Low) $T_{PLH}^{(2)}$ P-term clock pulse width $T_{R}^{(2)}$ Input rise time $T_{L}^{(2)}$ Input fall time $f_{SYSTEM}^{(2)}$ Maximum system frequency $T_{CONFIG}^{(2)}$ Configuration time ⁽³⁾ T_{INIT} ISP initialization time $T_{POE}^{(2)}$ P-term OE to output enabled $T_{POD}^{(2)}$ P-term OE to output disabled ⁽⁴⁾ $T_{PCO}^{(2)}$ P-term clock to output $T_{PAO}^{(2)}$ P-term set/reset to output validNotes:Notes:	-	6.5	ns
$\begin{array}{llllllllllllllllllllllllllllllllllll$	3.0	-	ns
$T_{H}^{(2)}$ Hold time $T_{WLH}^{(2)}$ C lobal Clock pulse width (High or Low) $T_{PLH}^{(2)}$ P-term clock pulse width $T_{R}^{(2)}$ Input rise time $T_{L}^{(2)}$ Input fall time $f_{SYSTEM}^{(2)}$ Maximum system frequency $T_{CONFIG}^{(2)}$ Configuration time ⁽³⁾ T_{INIT} ISP initialization time $T_{POE}^{(2)}$ P-term OE to output enabled $T_{POD}^{(2)}$ P-term OE to output disabled ⁽⁴⁾ $T_{PAO}^{(2)}$ P-term set/reset to output validNotes:Notes:	5.4	-	ns
$\begin{array}{c c c c c c c c } T_{H}(^{(2)} & \mbox{Hold time} \\ \hline T_{WLH}(^{(2)} & \mbox{Clock pulse width (High or Low)} \\ \hline T_{PLH}^{(2)} & \mbox{P-term clock pulse width} \\ \hline T_{R}^{(2)} & \mbox{Input rise time} \\ \hline T_{L}^{(2)} & \mbox{Input fall time} \\ \hline T_{L}^{(2)} & \mbox{Input fall time} \\ \hline T_{CONFIG}^{(2)} & \mbox{Maximum system frequency} \\ \hline T_{CONFIG}^{(2)} & \mbox{Configuration time} \\ \hline T_{POE}^{(2)} & \mbox{P-term OE to output enabled} \\ \hline T_{POD}^{(2)} & \mbox{P-term OE to output disabled}^{(4)} \\ \hline T_{PCO}^{(2)} & \mbox{P-term clock to output} \\ \hline T_{PAO}^{(2)} & \mbox{P-term set/reset to output valid} \\ \hline \end{array}$	6.3	-	ns
$\begin{array}{l lllllllllllllllllllllllllllllllllll$	0	-	ns
$\begin{array}{c c c c c c c } \hline T_R^{(2)} & \mbox{input rise time} \\ \hline T_L^{(2)} & \mbox{Input fall time} \\ \hline f_{SYSTEM}^{(2)} & \mbox{Maximum system frequency} \\ \hline T_{CONFIG}^{(2)} & \mbox{Configuration time}^{(3)} \\ \hline T_{INIT} & \mbox{ISP initialization time} \\ \hline T_{POE}^{(2)} & \mbox{P-term OE to output enabled} \\ \hline T_{PCO}^{(2)} & \mbox{P-term OE to output disabled}^{(4)} \\ \hline T_{PCO}^{(2)} & \mbox{P-term clock to output} \\ \hline T_{PAO}^{(2)} & \mbox{P-term set/reset to output valid} \\ \hline \hline Notes: \end{array}$	4.0	-	ns
$\begin{array}{llllllllllllllllllllllllllllllllllll$	6.0	-	ns
$ \begin{array}{c c} f_{\text{SYSTEM}}^{(2)} & \text{Maximum system frequency} \\ \hline f_{\text{CONFIG}}^{(2)} & \text{Configuration time}^{(3)} \\ \hline T_{\text{INIT}} & \text{ISP initialization time} \\ \hline T_{\text{POE}}^{(2)} & \text{P-term OE to output enabled} \\ \hline T_{\text{POD}}^{(2)} & \text{P-term OE to output disabled}^{(4)} \\ \hline T_{\text{PCO}}^{(2)} & \text{P-term clock to output} \\ \hline T_{\text{PAO}}^{(2)} & \text{P-term set/reset to output valid} \\ \hline \end{array} $	-	20	ns
$\begin{array}{llllllllllllllllllllllllllllllllllll$	-	20	ns
$\begin{array}{llllllllllllllllllllllllllllllllllll$	-	95	MHz
TPOE ⁽²⁾ P-term OE to output enabled TPOD ⁽²⁾ P-term OE to output disabled ⁽⁴⁾ TPCO ⁽²⁾ P-term clock to output TPAO ⁽²⁾ P-term set/reset to output valid	-	60	μs
T _{POD} ⁽²⁾ P-term OE to output disabled ⁽⁴⁾ T _{PCO} ⁽²⁾ P-term clock to output T _{PAO} ⁽²⁾ P-term set/reset to output valid Notes: Image: Comparison of the set/reset to output valid	-	60	μs
T _{POD} ⁽²⁾ P-term OE to output disabled ⁽⁴⁾ T _{PCO} ⁽²⁾ P-term clock to output T _{PAO} ⁽²⁾ P-term set/reset to output valid	-	11.2	ns
T _{PAO} ⁽²⁾ P-term set/reset to output valid Notes:	-	11.2	ns
T _{PAO} ⁽²⁾ P-term set/reset to output valid Notes:	-	10.7	ns
Notes:	-	11.2	ns
	Sig.	2.0	

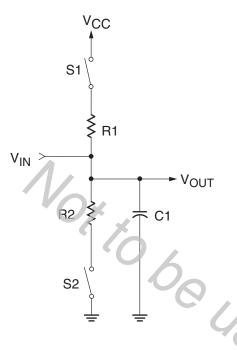
Internal Timing Parameters⁽¹⁾

			-10	
Symbol	Parameter	Min.	Max.	Unit
Buffer De	lays			
T _{IN}	Input buffer delay	-	2.2	ns
T _{FIN}	Fast Input buffer delay	-	3.1	ns
Т _{GCK}	Global Clock buffer delay	-	1.3	ns
T _{OUT}	Output buffer delay	-	3.6	ns
T _{EN}	Output buffer enable/disable delay	-	5.7	ns
Internal R	egister, Product Term, and Combinatorial Delays			
T _{LDI}	Latch transparent delay	-	2.0	ns
T _{SUI}	Register setup time	1.2	-	ns
T _{HI}	Register hold time	0.7	-	ns
T _{ECSU}	Register clock enable setup time	3.0	-	ns
T _{ECHO}	Register clock enable hold time	5.5	-	ns
T _{COI}	Register clock to output delay	-	1.6	ns
T _{AOI}	Register async. S/R to output delay	-	2.1	ns
T _{RAI}	Register async. recovery	-	6.0	ns
T _{PTCK}	Product term clock delay	-	3.3	ns
T _{LOGI1}	Internal logic delay (single p-term)	-	3.3	ns
T _{LOGI2}	Internal logic delay (PLA OR term)	-	4.2	ns
Feedback	Delays	O'		
Τ _F	ZIA delay	- 6	2.9	ns
Time Add	ers		0.	
T _{LOGI3}	Fold-back NAND delay	-	3.0	ns
T _{UDA}	Universal delay	-	2.5	ns
T _{SLEW}	Slew rate limited delay	-	6.0	ns

Notes:

1. These parameters guaranteed by design and characterization, not testing.

Switching Characteristics



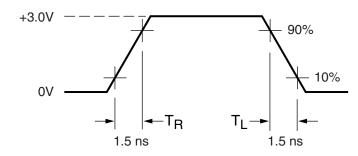
Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T _{POE} (High)	Open	Closed
T _{POE} (Low)	Closed	Open
TP	Closed	Closed

Note: For T_{POD} , C1 = 5 pF. Delay measured at output level of V_{OL} + 300 mV, V_{OH} - 300 mV.

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Figure 3: Typical AC Load Circuit



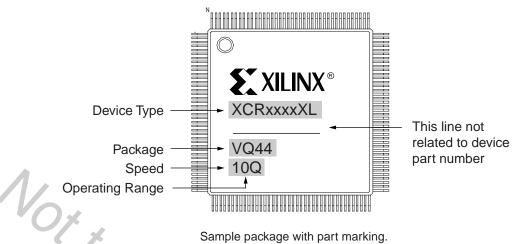
Measurements:

All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS023_06_042800



Device Part Marking



Ordering Combination Information

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range ⁽¹⁾
XCR3064XL-10VQ44Q	10 ns	VQ44	44	Very Thin Quad Flat Pack (VQFP)	Q
XCR3064XL-10VQ100Q	10 ns	VQ100	100	Very Thin Quad Flat Package (VQFP)	Q

Revision History

AGR3004AL-		To his VQTOC TO Very thin Quad Flat Fackage (VQFF) Q			
Notes: 1. $Q = Automotive: T_A = -40^\circ \text{ to } +125^\circ\text{C}$					
Revision I	-	e revision history for this document.			
Date	Version	Revision			
02/14/03	1.0	Initial Xilinx release.			
10/18/04	1.1	Added "Not to be used in new designs" watermark; moved to "Mature Products"			