SONY

CXP922032

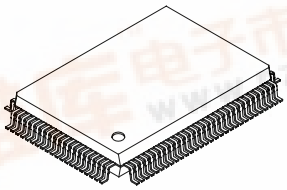
CMOS 16-bit Single Chip Microcomputer

Description

The CXP922032 is a CMOS 16-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer, remote control receive circuit, PWM output circuit, and as well as basic configurations like a 16-bit CPU, ROM, RAM, and I/O port.

This LSI also provides the sleep/stop functions that enable lower power consumption.

100 pin QFP (Plastic)



Features

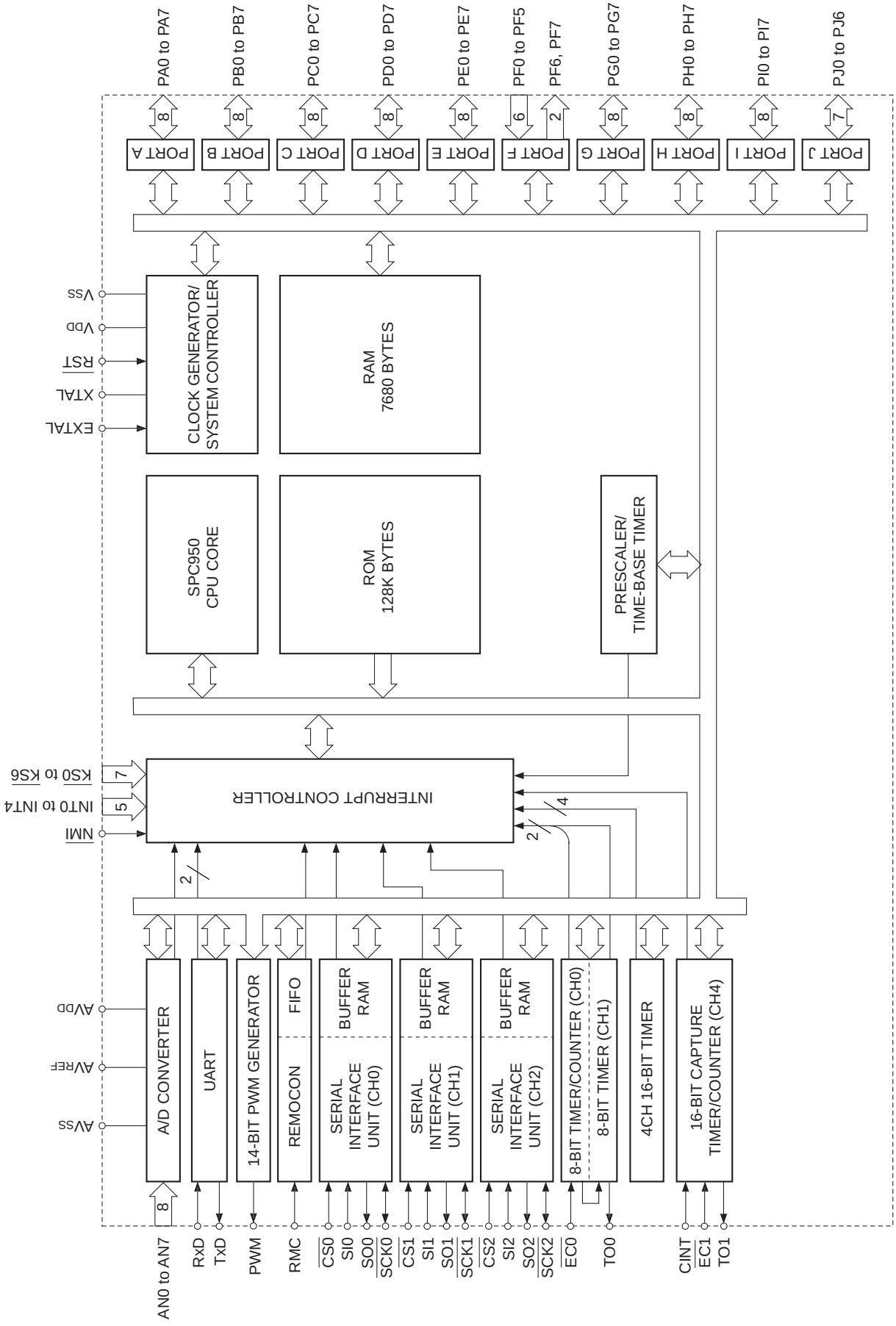
- An efficient instruction set as a controller
  - — Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
  - — Highly quadratic instruction system, general-purpose register of eight 16-bit × 16-bank configuration
- Minimum instruction cycle 100ns/20MHz operation (3.0 to 5.5V)
  167ns/12MHz operation (2.7 to 5.5V)
- Incorporated ROM capacity 128K bytes
- Incorporated RAM capacity 7680 bytes
- Peripheral functions
  - — A/D converter 8-bit 8 analog input, successive approximation system (Conversion time: 12.4µs at 20MHz)
  - — Serial interface Asynchronous serial interface (Simple UART)
    128-byte buffer RAM,3 channels
  - — Timers 8-bit timer/counter, 2 channels (with timing output)
    16-bit capture timer/counter (with timing output)
    16-bit timer, 4 channels
  - — Remote control receive circuit 8-bit pulse measurement counter, 8-stage FIFO
  - — PWM output circuit 14-bit, 1 channel
- Interruption 24 factors, 24 vectors, multi-interruption and priority selection possible
- Standby mode Sleep/stop
- Package 100-pin plastic QFP
- Piggy/evaluation chip CXP922000
- One-time PROM incorporated version CXP922P032

Structure

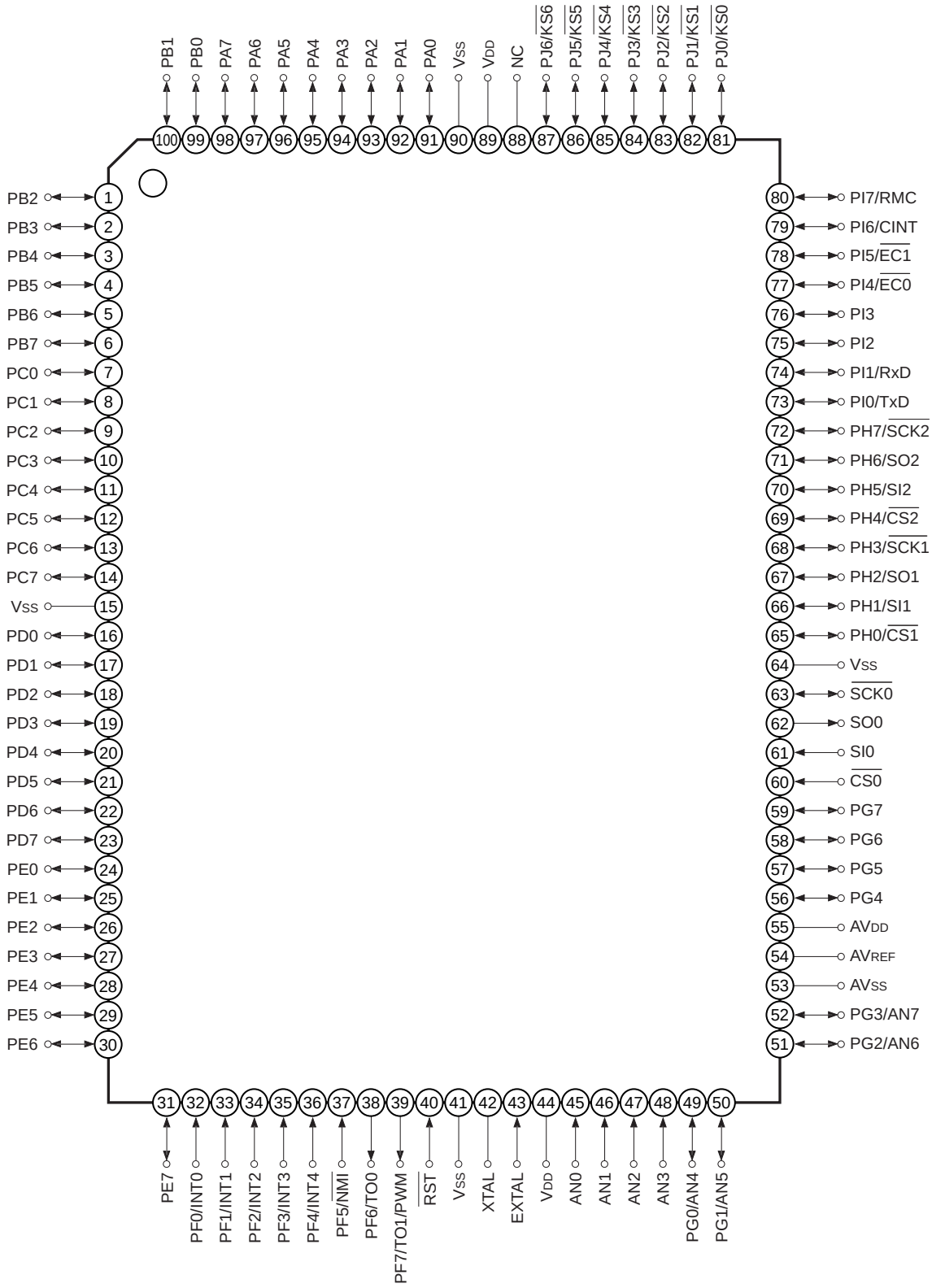
Silicon gate CMOS IC

E98Y43-PS

Block Diagram



Pin Assignment (Top View) 100-pin QFP package



Notes) 1. Do not make any connections to NC (Pin 88).

2. V_{SS} (Pins 15, 41, 64 and 90) must be connected to GND.

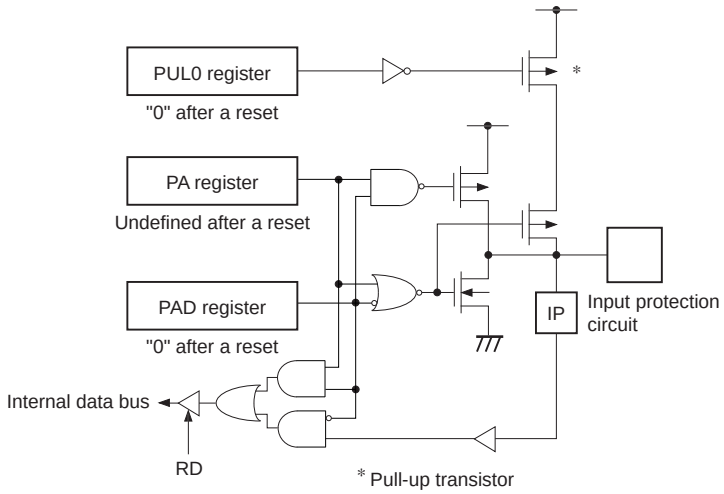
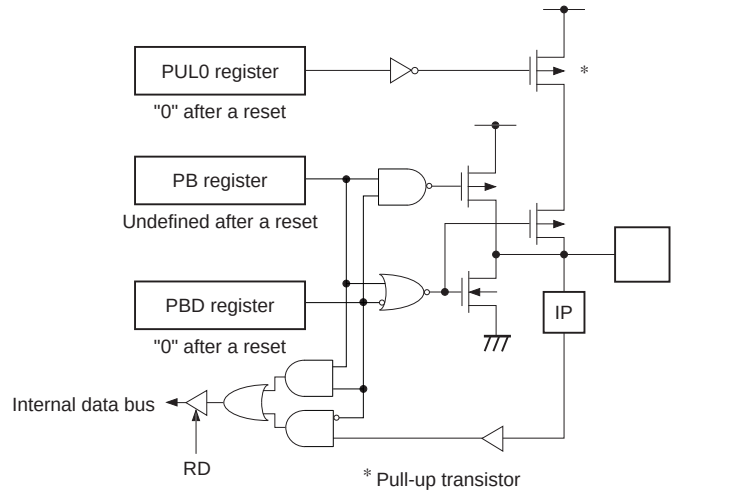
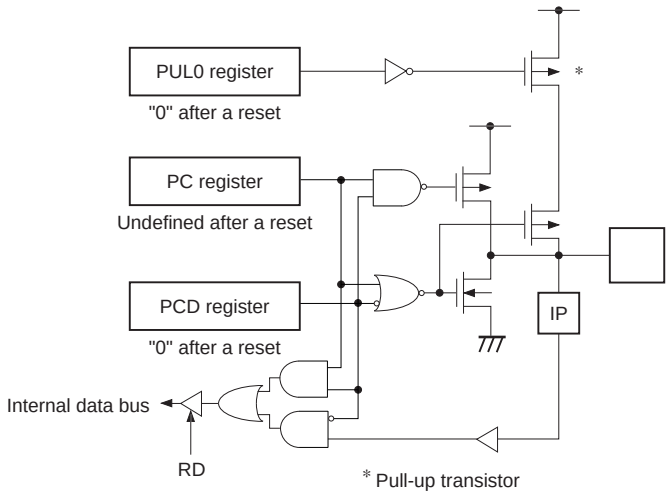
3. V_{DD} (Pins 44 and 89) must be connected to V_{DD}.

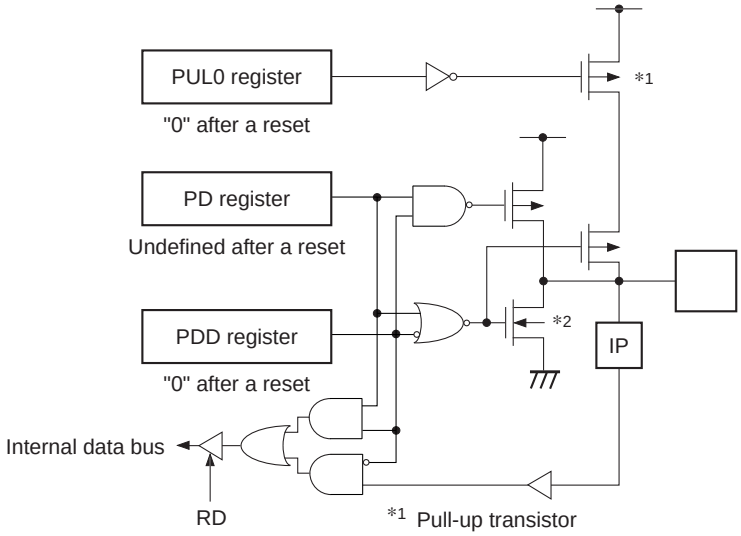
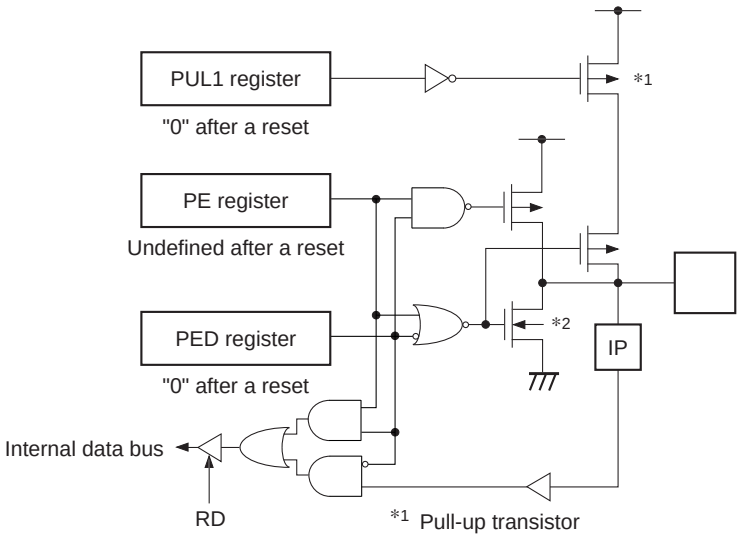
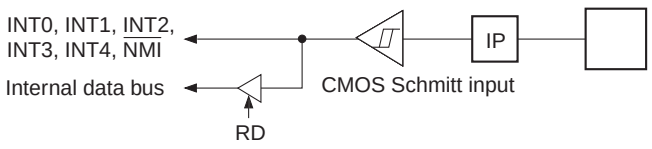
Pin Functions

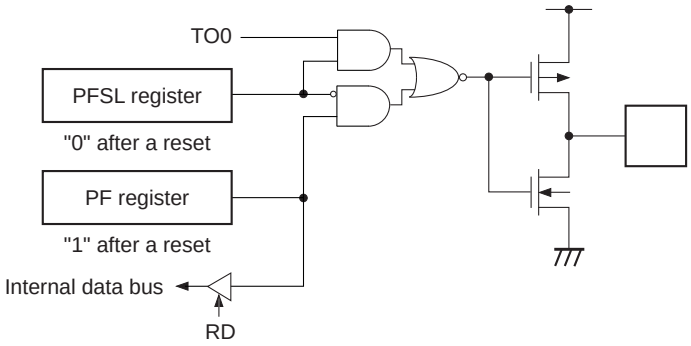
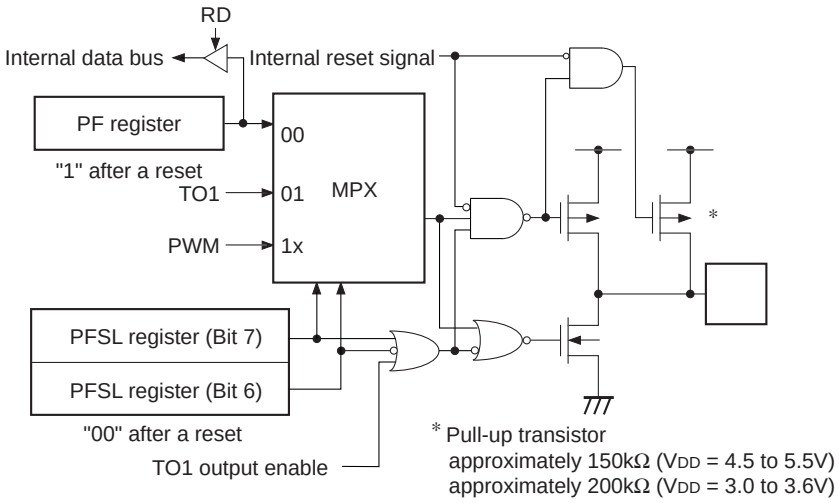
Symbol	I/O	Functions		
PA0 to PA7	I/O	(Port A) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. (8 pins)		
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. (8 pins)		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. (8 pins)		
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. Can drive 12mA sink current (V_{DD} = 4.5 to 5.5V). (8 pins)		
PE0 to PE7	I/O	(Port E) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. Can drive 12mA sink current (V_{DD} = 4.5 to 5.5V). (8 pins)		
PF0/INT0 to PF4/INT4	Input / Input	(Port F) 8-bit port. Lower 6 bits are for input; upper 2 bits are for output. (6 pins)	External interrupt inputs. (4 pins)	
PF5/$\overline{\text{NMI}}$	Input / Input		Non-maskable interrupt input.	
PF6/TO0	Output / Output		8-bit timer/counter output.	
PF7/TO1/ PWM	Output / Output / Output		16-bit capture timer/ counter output.	14-bit PWM output.
AN0 to AN3	Input	Analog input for A/D converter. (4 pins)		
PG0/AN4 to PG3/AN7	I/O / Input	(Port G) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. (8 pins)		Analog input for A/D converter. (4 pins)
PG4 to PG7	I/O			
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input.		
SI0	Input	Serial data (CH0) input.		
SO0	Output	Serial data (CH0) output.		
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O.		

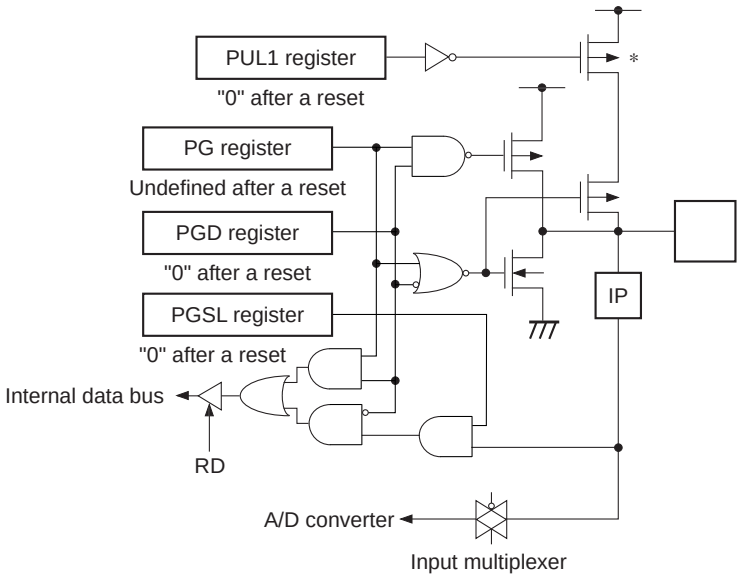
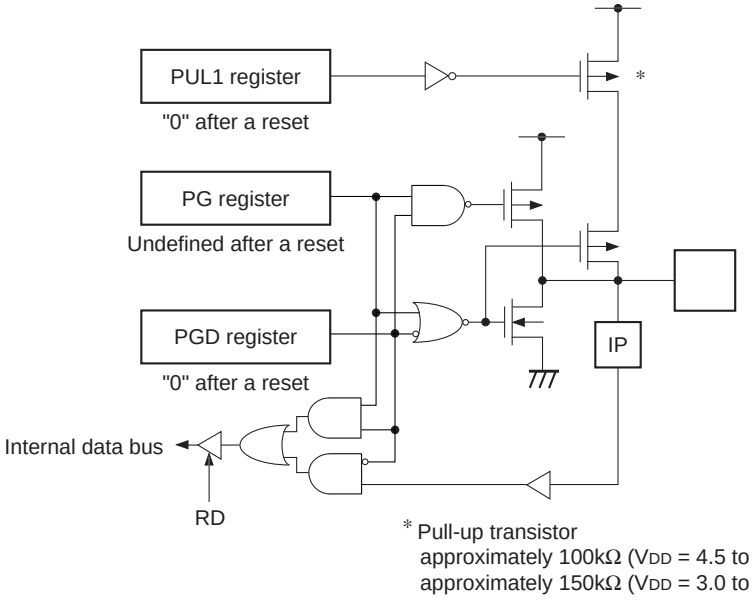
Symbol	I/O	Functions	
PH0/$\overline{CS1}$	I/O / Input	(Port H) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. (8 pins)	Serial chip select (CH1) input.
PH1/SI1	I/O / Input		Serial data (CH1) input.
PH2/SO1	I/O / Output		Serial data (CH1) output.
PH3/$\overline{SCK1}$	I/O / I/O		Serial clock (CH1) I/O.
PH4/$\overline{CS2}$	I/O / Input		Serial chip select (CH2) input.
PH5/SI2	I/O / Input		Serial data (CH2) input.
PH6/SO2	I/O / Output		Serial data (CH2) output.
PH7/$\overline{SCK2}$	I/O / I/O		Serial clock (CH2) I/O.
PI0/TxD	I/O / Output	(Port I) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 4-bit units. (8 pins)	UART transmission data output.
PI1/RxD	I/O / Input		UART reception data input.
PI2 to PI3	I/O		
PI4/$\overline{EC0}$	I/O / Input		External event input for 8-bit timer/counter.
PI5/$\overline{EC1}$	I/O / Input		External event input for 16-bit capture timer/ counter.
PI6/CINT	I/O / Input		External capture input for 16-bit capture timer/ counter.
PI7/RMC	I/O / Input		Remote control receive circuit input.
PJ0/$\overline{KS0}$ to PJ6/$\overline{KS6}$	I/O / Input	(Port J) 7-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in lower 4-bit units and upper 3-bit units. (7 pins)	Standby release input function can be specified in 1-bit units. (7 pins)
EXTAL	Input	Connects a crystal for system clock oscillation. (When the clock is supplied externally, input it to EXTAL and input an opposite phase clock to XTAL.)	
XTAL			
$\overline{RST}$	Input	System reset. Active at "L" level.	
AV_{DD}		Positive power supply for A/D converter.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AV_{SS}		GND for A/D converter.	
V_{DD}		Positive power supply. (Connect both V_{DD} pins to positive power supply.)	
V_{SS}		GND (Connect all four V_{SS} pins to GND.)	
NC		NC. (Do not make any cunnection to NC.)	

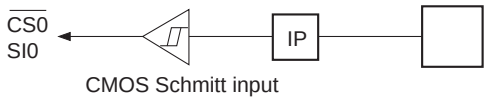
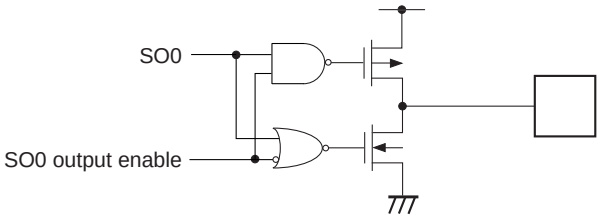
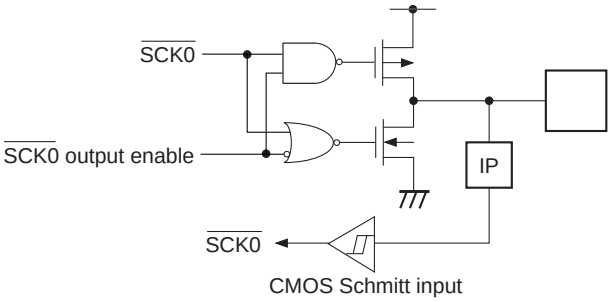
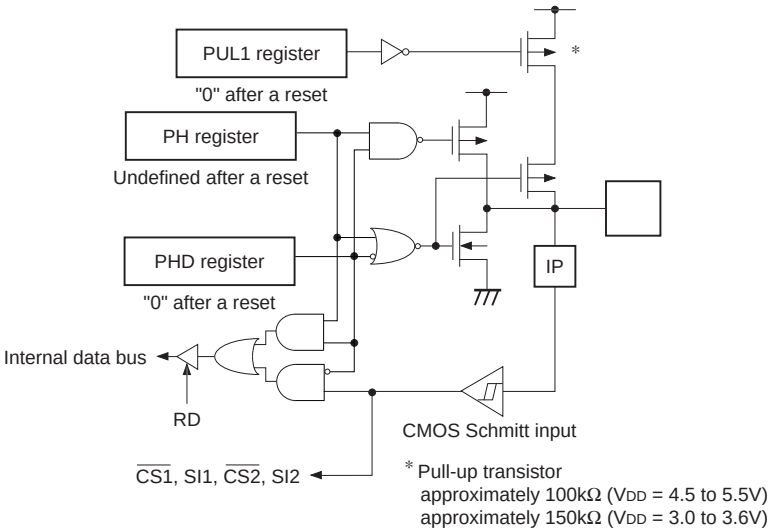
I/O Circuit Format for Pins

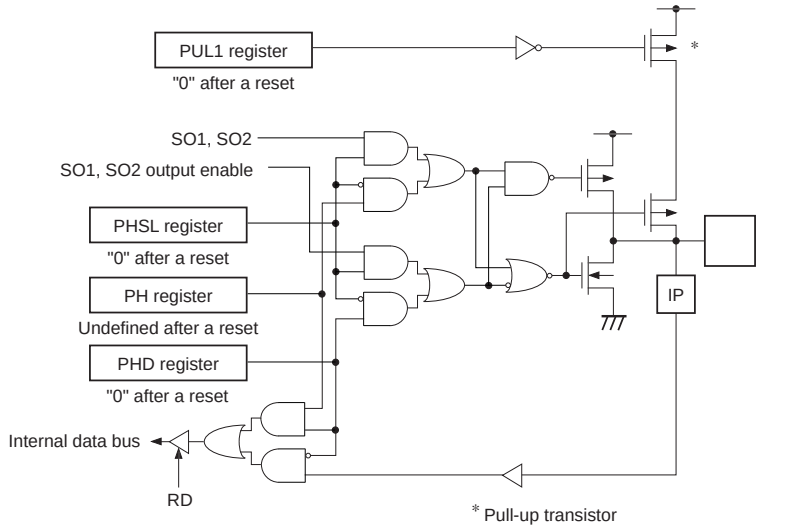
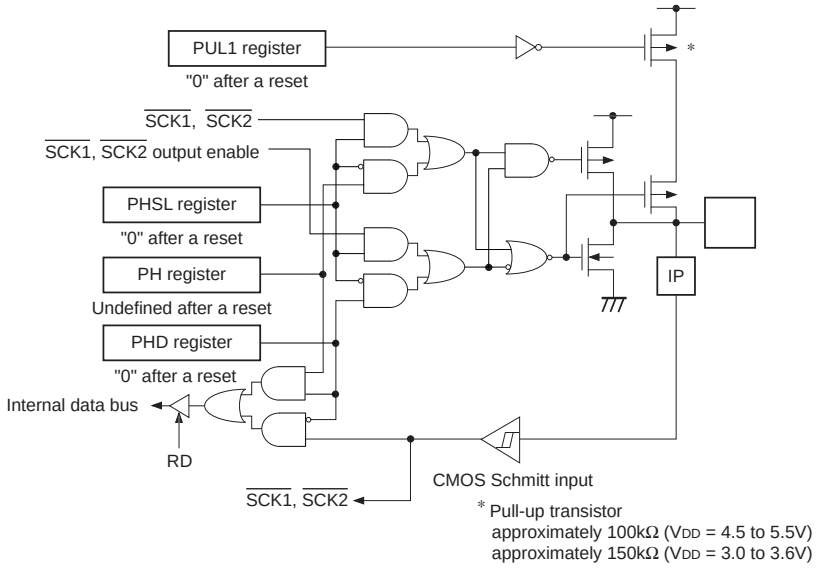
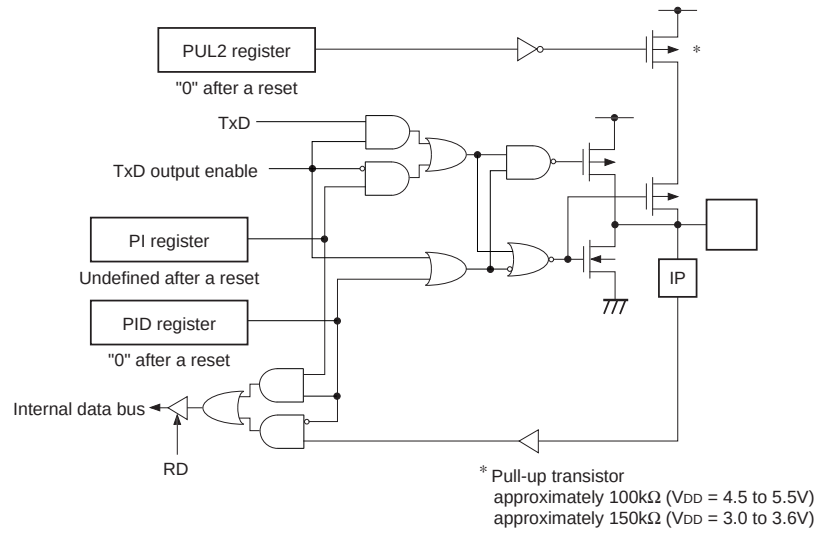
Pin	Circuit format	After a reset
PA0 to PA7		Hi-Z
PB0 to PB7		Hi-Z
PC0 to PC7		Hi-Z

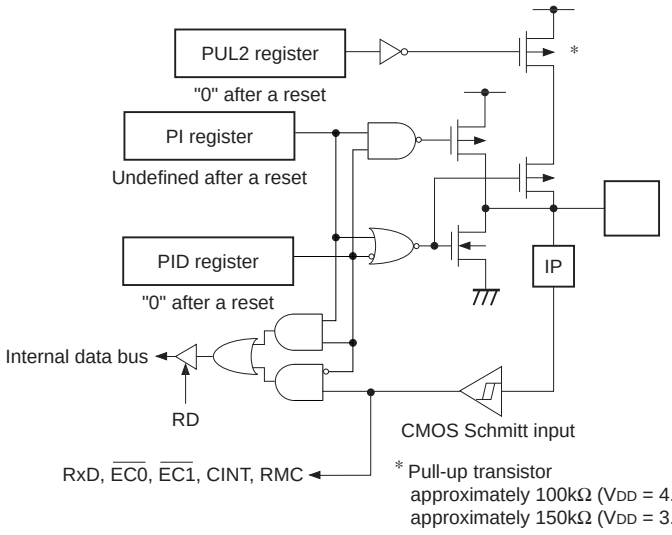
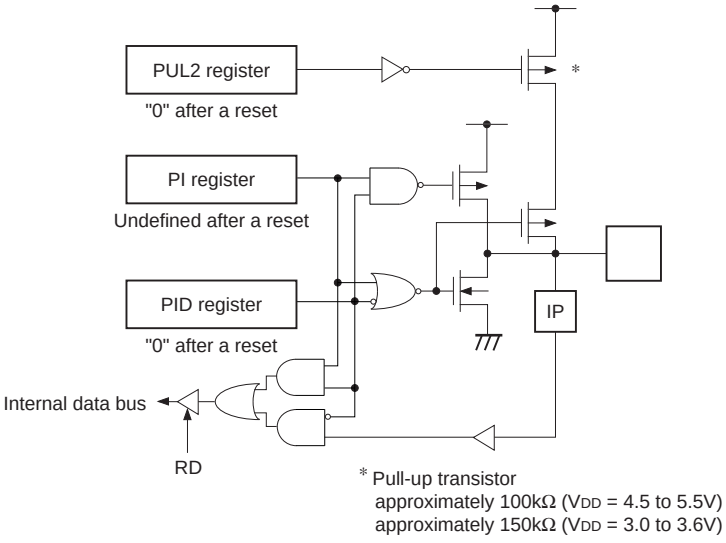
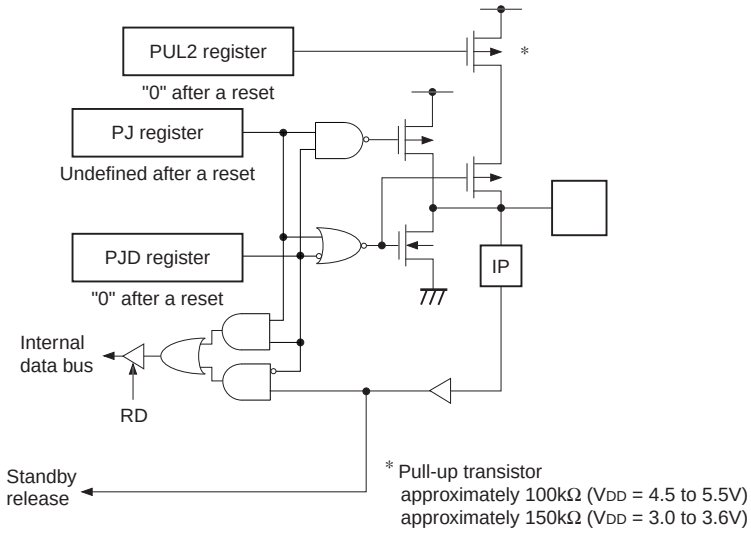
Pin	Circuit format	After a reset
PD0 to PD7	 *1 Pull-up transistor approximately 100kΩ (V_{DD} = 4.5 to 5.5V) approximately 150kΩ (V_{DD} = 3.0 to 3.6V) *2 Large current drive 12mA (V_{DD} = 4.5 to 5.5V) 4.5mA (V_{DD} = 3.0 to 3.6V)	Hi-Z
PE0 to PE7	 *1 Pull-up transistor approximately 100kΩ (V_{DD} = 4.5 to 5.5V) approximately 150kΩ (V_{DD} = 3.0 to 3.6V) *2 Large current drive 12mA (V_{DD} = 4.5 to 5.5V) 4.5mA (V_{DD} = 3.0 to 3.6V)	Hi-Z
PF0/INT0 to PF4/INT4 PF5/NMI		Hi-Z

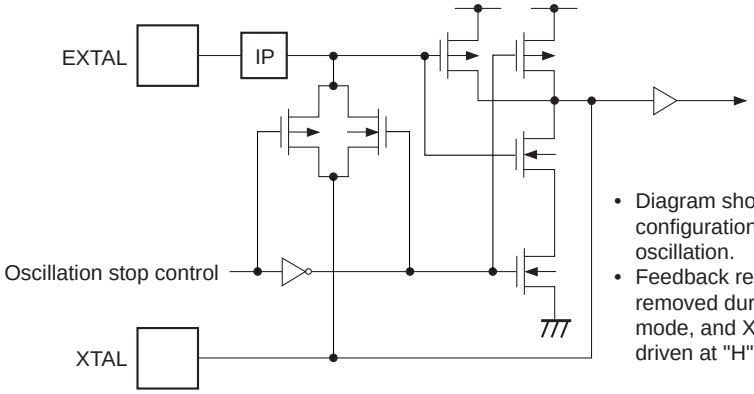
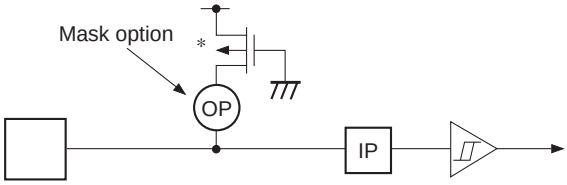
Pin	Circuit format	After a reset
PF6/TO0		"H" level
PF7/TO1/ PWM		"H" level ("H" level at ON resistance of pull-up transistor during a reset.)
AN0 to AN3		Hi-Z

Pin	Circuit format	After a reset
PG0/AN4 to PG3/AN7		Hi-Z
PG4 to PG7		Hi-Z

Pin	Circuit format	After a reset
$\overline{CS0}$ SI0		Hi-Z
SO0		Hi-Z
$\overline{SCK0}$		"H" level (Hi-Z during a reset)
PH0/$\overline{CS1}$ PH1/$\overline{SI1}$ PH4/$\overline{CS2}$ PH5/SI2		Hi-Z

Pin	Circuit format	After a reset
PH2/SO1 PH6/SO2		Hi-Z
PH3/$\overline{\text{SCK1}}$ PH7/SCK2		Hi-Z
PI0/TxD		Hi-Z

Pin	Circuit format	After a reset
PI1/RxD PI4/EC0 PI5/EC1 PI6/CINT PI7/RMC		Hi-Z
PI2 to PI3		Hi-Z
PJ0/KS0 to PJ6/KS6		Hi-Z

Pin	Circuit format	After a reset
EXTAL XTAL	 • Diagram shows circuit configuration during oscillation. • Feedback resistor is removed during stop mode, and XTAL is driven at "H" level.	Oscillation
$\overline{\text{RST}}$	 CMOS Schmitt input * Pull-up transistor approximately 300kΩ (V_{DD} = 4.5 to 5.5V) approximately 500kΩ (V_{DD} = 3.0 to 3.6V)	"L" level (during a reset)

Absolute Maximum Ratings (V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{DD}	AV_{SS} to +7.0*1	V	
	AV_{REF}	AV_{SS} to +7.0	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	All pins excluding large current output pins (value per pin)
	I_{OLC}	20	mA	Large current output pins*3 (value per pin)
Low level total output current	$\sum I_{OL}$	130	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP-100P-L01

*1 AV_{DD} must be the same voltage.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*3 The large current drive transistor is N-ch transistor of PD and PE.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V_{DD}	3.0	5.5	V	f_{EX} = 20MHz or less	Guaranteed operation range for 2, 4 and 8 frequency dividing clocks
		2.7	5.5	V	f_{EX} = 12MHz or less	
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode	
		2.5	5.5	V	Guaranteed data hold range during stop mode	
	AV_{DD}	2.7	5.5	V	*1	
	AV_{REF}	2.7	5.5	V		
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2, *4	
		0.8V_{DD}	V_{DD}	V	*2, *5	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS Schmitt input*3	
	V_{IHEX}	0.7V_{DD}	V_{DD} + 0.3	V	EXTAL	
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2, *4	
		0	0.2V_{DD}	V	*2, *5	
	V_{ILS}	0	0.2V_{DD}	V	CMOS Schmitt input*3	
	V_{ILEX}	–0.3	0.3V_{DD}	V	EXTAL*4	
		–0.3	0.2V_{DD}	V	EXTAL*5	
Operating temperature	Topr	–20	+75	°C		

*1 AV_{DD} and V_{DD} must be the same voltage.

*2 PA, PB, PC, PD, PE, PG, PH2, PH6, PI0, PI2, PI3, PJ for normal input port.

*3 PF0 to PF5, PH0, PH1, PH3 to PH5, PH7, PI1, PI4 to PI7, $\overline{CS0}$, SI0, $\overline{SCK0}$, $\overline{RST}$.

*4 When the supply voltage (V_{DD}) is within the range of 4.5 to 5.5V.

*5 When the supply voltage (V_{DD}) is within the range of 2.7 to 5.5V.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Topr = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF6, PF7, PG to PJ, SO0, SCK0	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PE, PF6, PF7, PG to PJ, SO0, SCK0	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PE	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IL}	PA to PE*2, PG to PJ*2	V_{DD} = 5.5V, V_{IL} = 0.4V			–45	µA
			V_{DD} = 4.5V, V_{IH} = 4.0V	–2.78			µA
I/O leakage current	I_{IZ}	PA to PE*2, PF0 to PF5, PF7, PG to PJ*2, AN0 to AN3, CS0, SI0, SO0, SCK0, RST*1	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Supply current*3	I_{DD}*4	V_{DD}, V_{SS}	V_{DD} = 5 ± 0.5V, 20MHz crystal oscillation (C_1 = C_2 = 10pF)		40	65	mA
	I_{DDS1}		V_{DD} = 5 ± 0.5V, 20MHz crystal oscillation (C_1 = C_2 = 10pF), sleep mode		8	14	mA
	I_{DDS2}		V_{DD} = 5.5V, stop mode			10	µA
Input capacitance	C_{IN}	PA to PE, PF0 to PF5, PG to PJ, AN0 to AN3, CS0, SI0, SCK0, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*2 PA to PE and PG to PJ specify the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*3 When all output pins are open.

*4 When the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (2 frequency dividing clock).

DC Characteristics (V_{DD} = 3.0 to 3.6V) (Topr = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF6, PF7, PG to PJ, SO0, SCK0	V_{DD} = 3.0V, I_{OH} = –0.15mA	2.7			V
			V_{DD} = 3.0V, I_{OH} = –0.5mA	2.3			V
Low level output voltage	V_{OL}	PA to PE, PF6, PF7, PG to PJ, SO0, SCK0	V_{DD} = 3.0V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 1.6mA			0.5	V
		PD, PE	V_{DD} = 3.0V, I_{OL} = 5.0mA			1.0	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 3.6V, V_{IL} = 0.3V	–0.7		–200	µA
	I_{IL}	PA to PE*2, PG to PJ*2	V_{DD} = 3.6V, V_{IL} = 0.3V			–30	µA
			V_{DD} = 3.0V, V_{IH} = 2.7V	–1.0			µA
I/O leakage current	I_{IZ}	PA to PE*2, PF0 to PF5, PF7, PG to PJ*2, AN0 to AN3, CS0, SI0, SO0, SCK0, $\overline{RST}$*1	V_{DD} = 3.6V, V_I = 0, 3.6V			±10	µA
Supply current*3	I_{DD}*4	V_{DD}, V_{SS}	V_{DD} = 3.3 ± 0.3V, 20MHz crystal oscillation (C_1 = C_2 = 10pF)		22	40	mA
	I_{DDS1}		V_{DD} = 3.3 ± 0.3V, 20MHz crystal oscillation (C_1 = C_2 = 10pF), sleep mode		4.5	8	mA
	I_{DDS2}		V_{DD} = 3.6V, stop mode			10	µA
Input capacitance	C_{IN}	PA to PE, PF0 to PF5, PG to PJ, AN0 to AN3, CS0, SI0, SCK0, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*2 PA to PE and PG to PJ specify the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*3 When all output pins are open.

*4 When the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (2 frequency dividing clock).

AC Characteristics

(1) Clock timing (Topr = –20 to +75°C, V_{DD} = 2.7 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Typ.	Max.	Unit
Main clock base oscillation frequency	f_{EX}	XTAL EXTAL	Fig.1, Fig.2	V_{DD} = 3.0 to 5.5V	1		20	MHz
					1		12	
Main clock base oscillation input pulse width	t_{XL}, t_{XH}	EXTAL	Fig.1, Fig.2 External clock drive	V_{DD} = 3.0 to 5.5V	23			ns
					37.5			
Main clock base oscillation input rise time, fall time	t_{XR}, t_{XF}	EXTAL	Fig.1, Fig.2 External clock drive				100	ns

Note) tsys indicates the four values below according to the upper two bits (PCK1,PCK0) of the clock control register (CLC: 0002FEh).
tsys [ns] = 2/f_{EX}(PCK1, PCK0 = 00), 4/f_{EX}(PCK1, PCK0 = 01), 8/f_{EX} (PCK1, PCK0 = 10), 16/f_{EX}(PCK1, PCK0 = 11)

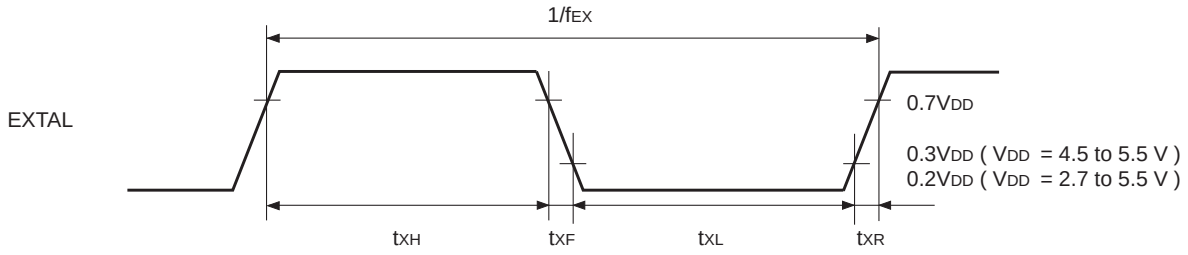


Fig.1. Clock timing

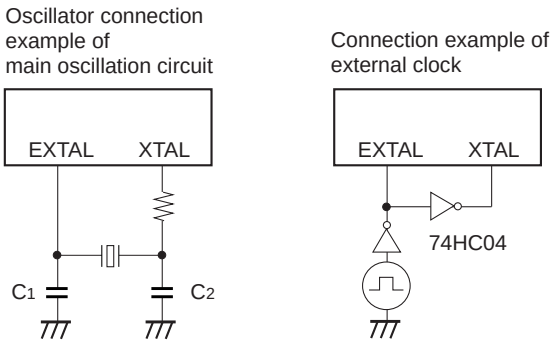


Fig.2. Oscillator connection and clock applied conditions

(2) Event count input (Topr = –20 to +75°C, V_{DD} = 2.7 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$, $\overline{EC1}$	Fig.3	tsys + 100		ns

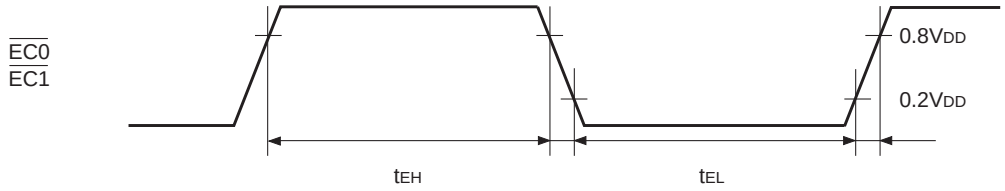


Fig.3. Event count input timing

(3) Interruption and reset input (Topr = –20 to +75°C, V_{DD} = 2.7 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
External interruption high, low level width	t_{IH}, t_{IL}	$\overline{NMI}$ INT0 to INT4 KS0 to KS6	Main mode		tsys + 100		ns
			Sleep mode Stop mode		1		µs
		INT0, INT1, INT4	Noise filter selected	ϕ	2tsys + 100		ns
				PS4	32/f_{EX} + 100		
				PS6	128/f_{EX} + 100		
Reset input low level width	t_{RST}	$\overline{RST}$	Fig.5		3tsys + 200		ns

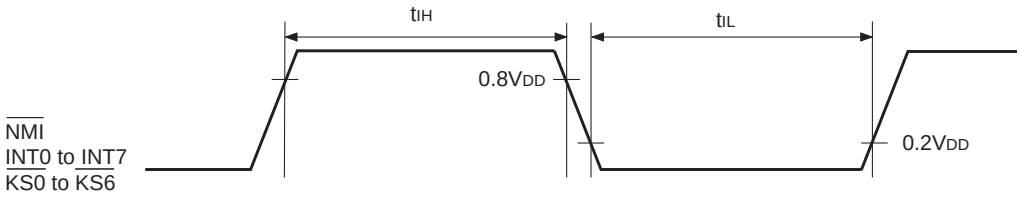


Fig.4. Interruption input timing

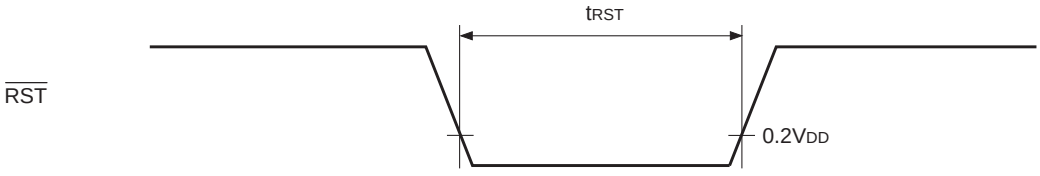


Fig.5. Reset input timing

(4) A/D converter characteristics

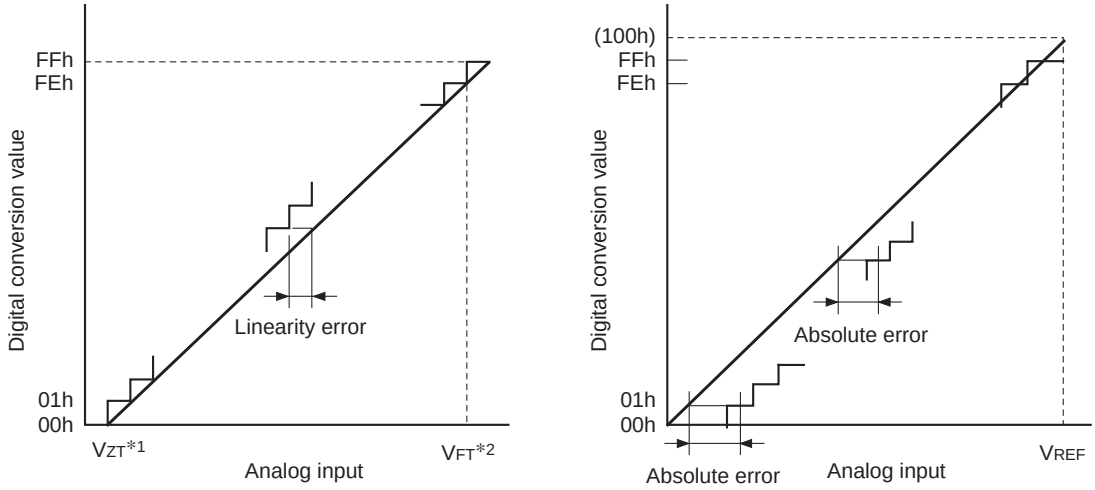
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			V_{DD} = AV_{DD} = AV_{REF} = 5.0V			±2	LSB
Absolute error						±3	LSB
Conversion time	t_{CONV}			31/f_{ADC}*			µs
Sampling time	t_{SAMP}			10/f_{ADC}*			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} – 0.5			V
Analog input voltage	V_{IAN}	AN0 to AN7		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Main mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode			10	µA

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.0 to 3.6V, AV_{REF} = 2.7 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			V_{DD} = AV_{DD} = AV_{REF} = 3.3V			±2	LSB
Absolute error						±3	LSB
Conversion time	t_{CONV}			31/f_{ADC}*			µs
Sampling time	t_{SAMP}			10/f_{ADC}*			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} – 0.3			V
Analog input voltage	V_{IAN}	AN0 to AN7		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Main mode		0.4	0.7	mA
	I_{REFS}		Sleep mode Stop mode			10	µA

* f_{ADC} indicates the below values due to the contents of Bit 6 (CKS) of the A/D control register (ADC: 000131h).
When PS3 is selected, $f_{ADC} = f_{EX}/8$
When PS4 is selected, $f_{ADC} = f_{EX}/16$
However, when PS3 is selected, f_{EX} is 12MHz or less.



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.
*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

Fig.6. Definition of A/D converter terms

(5) Serial transfer (CH0, CH1, CH2) (Topr = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 100	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 100	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1 SO2	External start transfer mode		1.5tsys + 100	ns
$\overline{CS} \uparrow \rightarrow$ SO float delay time	t_{DCSOF}	SO0 SO1 SO2	External start transfer mode		1.5tsys + 100	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$ $\overline{CS2}$	External start transfer mode	tsys + 100		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	2tsys + 150		ns
			Output mode	8/f_{EX}		ns
$\overline{SCK}$ high, low pulse width	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	tsys + 60		ns
			Output mode	4/f_{EX} – 25		ns
SI input data setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0 SI1 SI2	$\overline{SCK}$ input mode	50		ns
			$\overline{SCK}$ output mode	100		ns
SI input data hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0 SI1 SI2	$\overline{SCK}$ input mode	tsys + 100		ns
			$\overline{SCK}$ output mode	50		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1 SO2	$\overline{SCK}$ input mode		tsys + 100	ns
			$\overline{SCK}$ output mode		50	ns
Minimum interval time	t_{INT}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	$\overline{SCK}$ input mode	3tsys + 100		ns
			$\overline{SCK}$ output mode	8/f_{EX}		ns

Note) The load condition for the $\overline{SCK}$ output mode and SO output delay time is 50pF+1TTL.

(Topr = –20 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1 SO2	External start transfer mode		1.5tsys + 200	ns
$\overline{CS} \uparrow \rightarrow$ SO float delay time	t_{DCSOF}	SO0 SO1 SO2	External start transfer mode		1.5tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$ $\overline{CS2}$	External start transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	2tsys + 200		ns
			Output mode	8/f_{EX}		ns
$\overline{SCK}$ high, low pulse width	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	tsys + 80		ns
			Output mode	4/f_{EX} – 50		ns
SI input data setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0 SI1 SI2	$\overline{SCK}$ input mode	80		ns
			$\overline{SCK}$ output mode	150		ns
SI input data hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0 SI1 SI2	$\overline{SCK}$ input mode	tsys + 120		ns
			$\overline{SCK}$ output mode	70		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1 SO2	$\overline{SCK}$ input mode		tsys + 200	ns
			$\overline{SCK}$ output mode		80	ns
Minimum interval time	t_{INT}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	$\overline{SCK}$ input mode	3tsys + 150		ns
			$\overline{SCK}$ output mode	8/f_{EX}		ns

Note) The load condition for the $\overline{SCK}$ output mode and SO output delay time is 50pF.

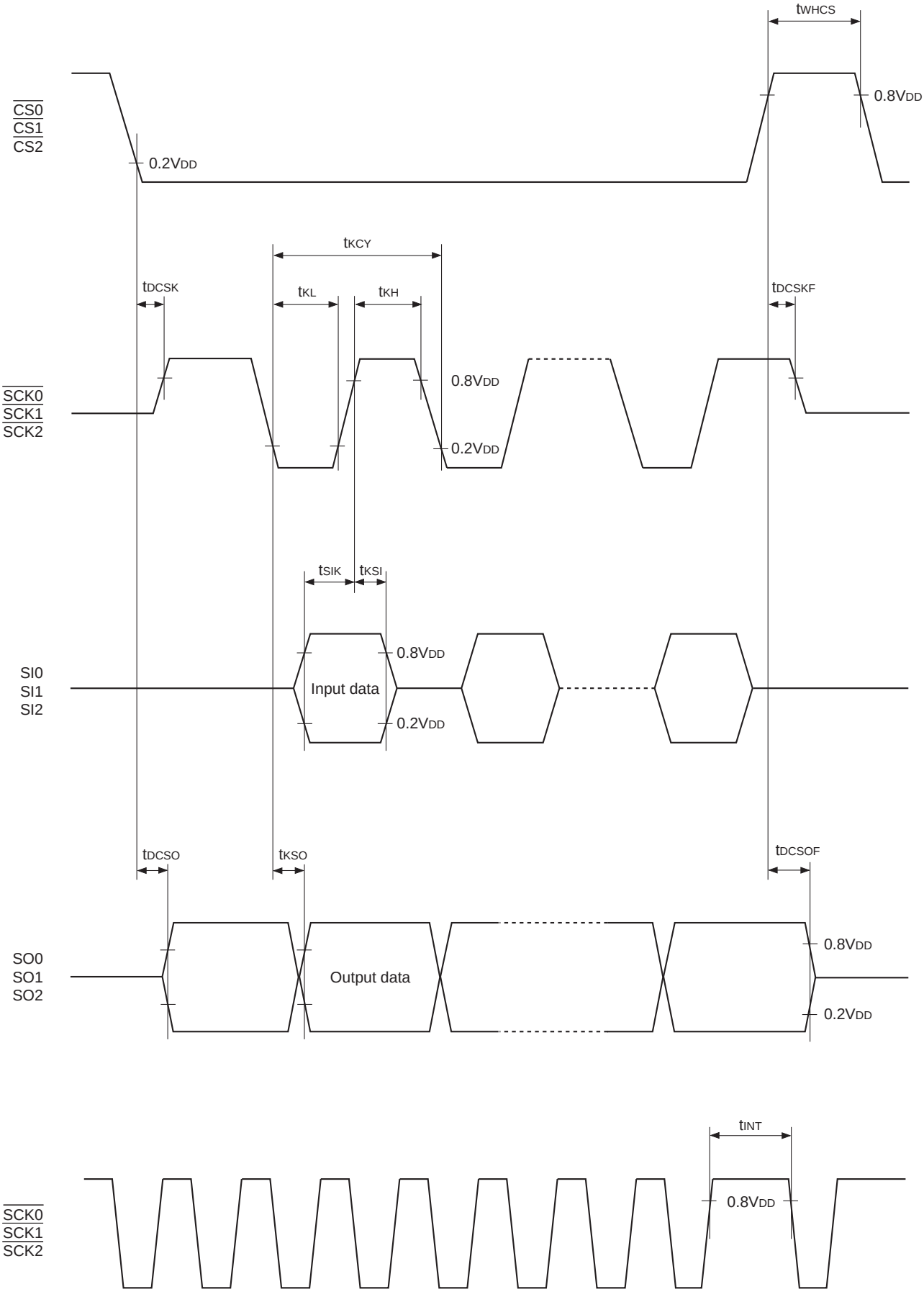


Fig.7. Serial transfer CH0, CH1, CH2 timing

(6) Remote control reception (Topr = –20 to +75°C, V_{DD} = 2.7 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
Remote control receive high, low level width	t_{RMC}	RMC	Main mode Sleep mode	PS5 selected	128/f_{EX} + 100		ns
				PS6 selected	256/f_{EX} + 100		
				PS8 selected	1024/f_{EX}+ 100		

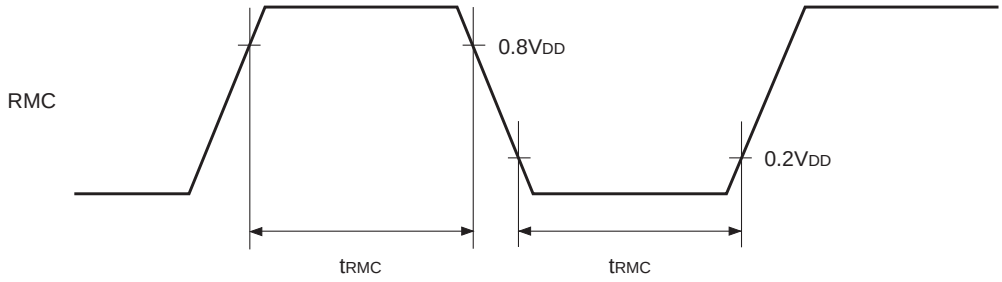


Fig.8. Remote control signal input timing

Appendix

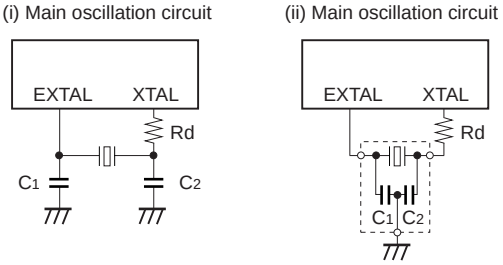


Fig.9. Recommended oscillation circuit

Manufacturer	Model	f_{EX} (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA4.00MG	4	30	30	0	(i)	
	CSA8.00MTZ093	8					
	CSA10.0MTZ093	10					
	CSA12.0MTZ093	12					
	CST4.00MGW*	4				(ii)	
	CST8.00MTW093*	8					
	CST10.0MTW093*	10					
	CST12.0MTW093*	12					
	CSA16.00MXZ040	16	5	5	0	(i)	V_{DD} = 4.0 to 5.5V
	CST16.00MXW0C1*	16				(ii)	
	CSA20.00MXZ040	20				(i)	
	CST20.00MXW0H1*	20				(ii)	
RIVER ELETEC CO., LTD.	HC-49/U03	4	27	27	560	(i)	CL = 18.5pF
		8	15	15	330		CL = 13.0pF
		10	10	10	330		CL = 10.5pF
		12	10	10	180		CL = 10.5pF
		16	8	8	0		CL = 10.0pF
		20	6	6	0		CL = 8.5pF
KINSEKI LTD.	HC49/U-S	4	22	22	2.2k	(i)	CL = 16pF V_{DD} = 3.0 to 5.5V
		8	10	10	0		CL = 12pF V_{DD} = 3.5 to 5.5V
		10					
		12					
		16					
		20					
TDK Corporation	CCR4.0MC3*	4	38 (±20%)	38 (±20%)	0	(ii)	
	CCR8.0MC5*	8	20 (±20%)	20 (±20%)	0		
	CCR10.0MC5*	10	20 (±20%)	20 (±20%)	0		
	CCR12.0MC5*	12	20 (±20%)	20 (±20%)	0		
	CCR16.0MC6*	16	10 (±20%)	10 (±20%)	0		V_{DD} = 3.5 to 5.5V
	CCR20.0MC6*	20	10 (±20%)	10 (±20%)	0		

* Indicates types with on-chip grounding capacitor (C_1, C_2). CCR*** : Surface mounted type ceramic oscillator.
CL : Load capacitor

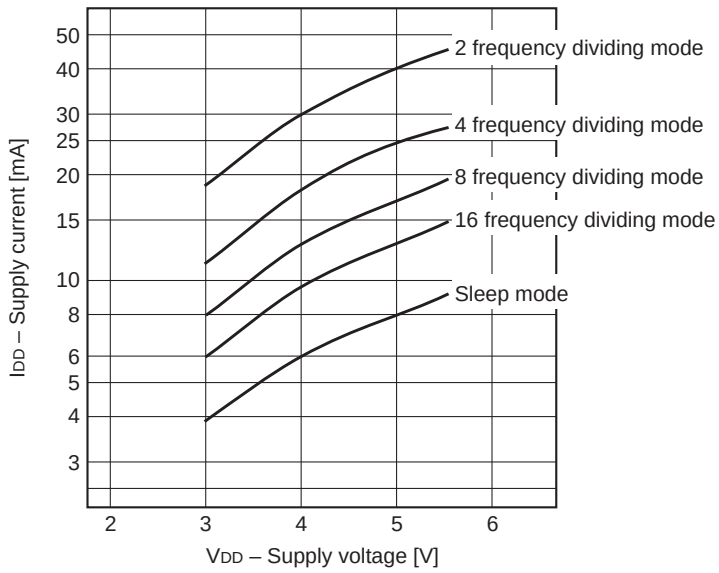
Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Characteristics Curve

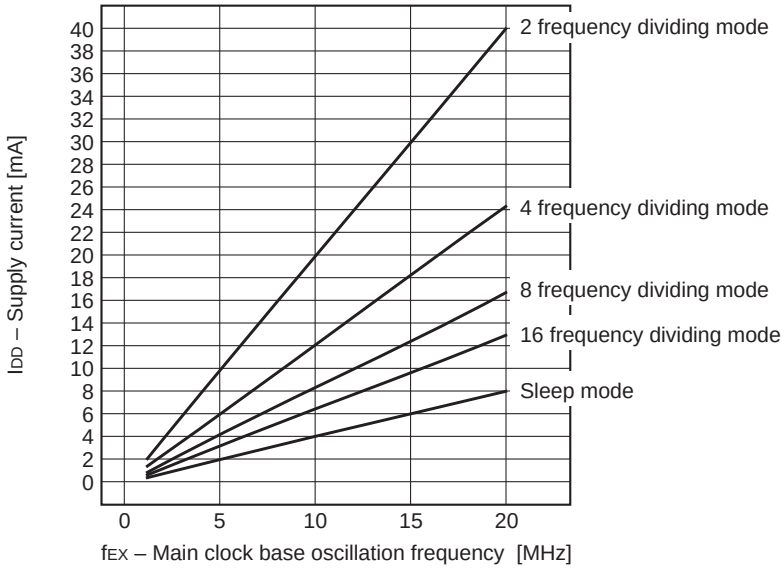
IDD vs. VDD

(fEX = 20MHz, Topr = 25°C, Typical)



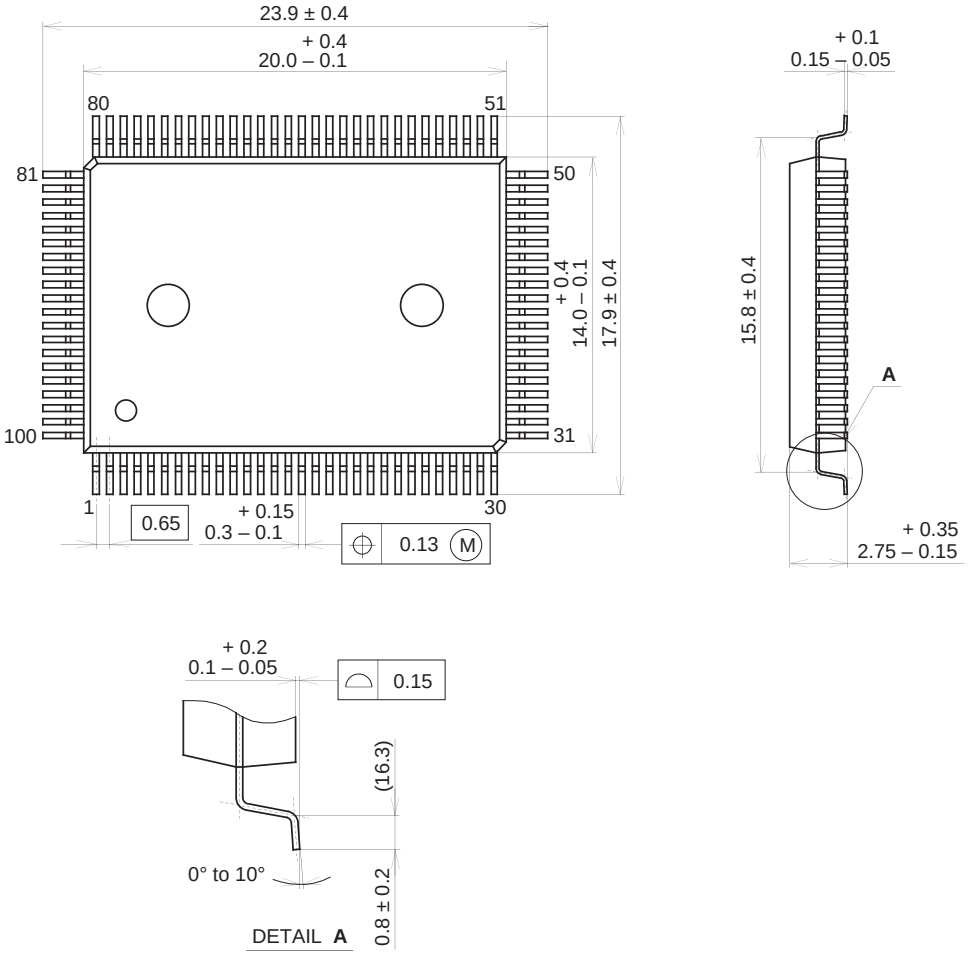
IDD vs. fEX

(VDD = 5V, Topr= 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g