Preliminary

EXAR

# XRD9829

## 10-Bit Linear CIS/CCD Sensor Signal Processor with Serial Control

March 1998-2

### FEATURES

- 10-Bit 6MSPS Pixel Rate
- 6-Bit Programmable Gain Amplifier
- 8–Bit Programmable Offset Adjustment
- 4:1 Analog Multiplexer
- CIS or CCD Compatibility
- Internal Clamp for CIS or CCD AC Coupled Modes
- 3.3V or 5V Operation & I/O Compatibility
- Serial Load Control Registers
- Low Power CMOS: 150mW
- Low Cost 20-Lead SOIC Package
- Monotonic

### APPLICATIONS

- Color and Grayscale Flatbed Scanners
- Color and Grayscale Sheetfed Scanners
- Multifunction Peripherals
- Digital Color Copiers
- General Purpose CIS or CCD Imaging
- Low Cost Data Acquisition

### GENERAL DESCRIPTION

The XRD9829 is a complete linear CIS or CCD sensor signal processor on a single monolithic chip. The XRD9829 includes a high speed 10–bit ADC, a 6-bit Programmable Gain Amplifier with gain adjustment of 1 to 10, and 8-bit programmable input referred offset calibration range of 800mV.

In the CCD mode the input signal is AC coupled with an external capacitor. An internal clamp sets the black level. In the CIS mode the input can also be AC coupled similar to the CCD mode. This enables CIS signals with black levels to be referenced to ground and then level shifted internally to correspond to VRB. For CIS sensors without black references the clamp switch can be disabled in DC Coupled mode. The CIS signal is level shifted to VRB in order to use the full range of the ADC.

The CIS DC Coupled mode can also be used in other applications that do not require a CDS function but require programmable gain and offset such as low cost data acquisition.

### ORDERING INFORMATION

| Part No. | Package | Operating Temperature Range |
|---|---|---|
| XRD9829ACD | 20-Lead SOIC | 0°C to +70°C |





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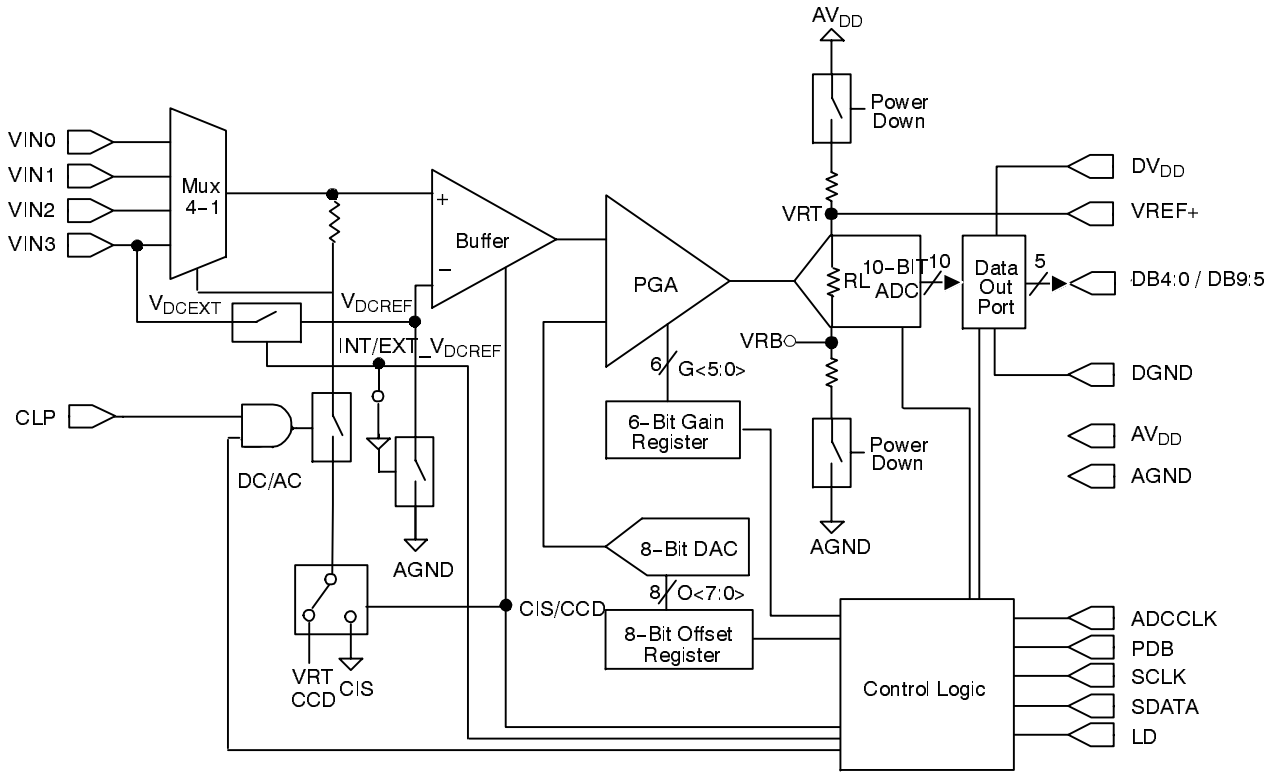
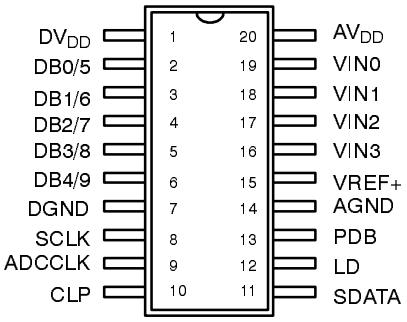



**Figure 1. Functional Block Diagram**

## PIN CONFIGURATION




**20 Lead SOIC (Jedec, 0.300")**

## PIN DESCRIPTION

| Pin # | Symbol | Description |
|---|---|---|
| 1 | $DV_{DD}$ | Digital $V_{DD}$ (for Output Drivers) |
| 2 | DB0/5 | Data Output Bit 0/5 |
| 3 | DB1/6 | Data Output Bit 1/6 |
| 4 | DB2/7 | Data Output Bit 2/7 |
| 5 | DB3/8 | Data Output Bit 3/8 |
| 6 | DB4/9 | Data Output Bit 4/9 |
| 7 | DGND | Digital Ground (for Output Drivers) |
| 8 | SCLK | Serial Data Clock for Write Operation |
| 9 | ADCCLK | A/D Converter Clock |
| 10 | CLP | Black Level Clock for Internal Clamp |
| 11 | SDATA | Serial Data for Write Operation |
| 12 | LD | Serial Data Load for Write Operation |
| 13 | PDB | Active Low Power Down Signal |
| 14 | AGND | Analog Ground |
| 15 | VREF+ | A/D Positive Reference for Decoupling Cap |
| 16 | VIN3 | Analog Input 3 |
| 17 | VIN2 | Analog Input 2 |
| 18 | VIN1 | Analog Input 1 |
| 19 | VIN0 | Analog Input 0 |
| 20 | $AV_{DD}$ | Analog Power Supply |

## DC ELECTRICAL CHARACTERISTICS

**Test Conditions: $AV_{DD}$=$DV_{DD}$=3.3V / 5V, ADCCLK=6MHz, 50% Duty Cycle, $T_A$=25°C unless otherwise specified.**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | |
| $AV_{DD}$ | Analog Power Supply | 3.0 | 3.3 | 5.5 | V | |
| $DV_{DD}$ | Digital I/O Power Supply | 3.0 | 3.3 | 5.5 | V | $DV_{DD} \leq AV_{DD}$ |
| $I_{DD}$ | Supply Current | | 30 | | mA | $V_{DD}$=5V |
| $IDD_{PD}$ | Power Down Power Supply Current | | | TBD | µA | $V_{DD}$=5V |
| **ADC Specifications** | | | | | | |
| RES | Resolution | 10 | | | Bits | |
| $F_s$ | Maximum Sampling Rate | 10 | | | MSPS | TEST1 mode enabled. (Refer to Control Register 'Mode & Test'.) |
| DNL | Differential Non-Linearity | | ±0.5 | | LSB | |
| INL | Integral Non-Linearity | | ±1.0 | | LSB | |
| MON | Monotonicity | | Yes | | | No Missing Codes Guaranteed |
| $V_{RT}$ | Top Reference Voltage | | $AV_{DD}$/1.3 | | V | |
| $V_{RB}$ | Bottom Reference Voltage | | $AV_{DD}$/10 | | V | |
| $\Delta V_{REF}$ | Differential Reference Voltage ($V_{RT}$ - $V_{RB}$) | | 0.67 $AV_{DD}$ | | V | |
| $R_L$ | Ladder Resistance | 360 | 600 | 780 | Ω | |
| **PGA & Offset DAC Specifications** | | | | | | |
| PGARES | PGA Resolution | 6 | | | Bits | |
| $PGAG_{MIN}$ | Minimum Gain | | 1.0 | | V/V | |
| $PGAG_{MAX}$ | Maximum Gain | | 10.0 | | V/V | |
| $PGAG_{\Delta}$ | Gain Adjustment Step Size | | 0.14 | | V/V | |
| $V_{BLACK}$ | Black Level Input Range | -100 | | 500 | mV | DC Mode |
| DACRES | Offset DAC Resolution | 8 | | | Bits | |
| $OFF_{MIN}$ | Minimum Offset Adjustment | | -200 | | mV | [1] |
| $OFF_{MAX}$ | Maximum Offset Adjustment | | +600 | | mV | [1] |
| $OFF_{\Delta}$ | Offset Adjustment Step Size | | 3.14 | | mV | |

***Note:***

*[1] The additional ±100 mV of adjustment with respect to the black level input range is needed to compensate for any additional offset introduced by the XRD9829 Buffer/PGA internally.*

**Specifications are subject to change without notice**

## ELECTRICAL CHARACTERISTICS

**Test Conditions: $AV_{DD}$=$DV_{DD}$=3.3V / 5V, ADCCLK=6MHz, 50% Duty Cycle, $T_A$=25°C unless otherwise specified.**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Buffer Specifications** | | | | | | |
| $I_{IL}$ | Input Leakage Current | | | 100 | nA | |
| CIN | Input Capacitance | | 10 | | pF | |
| $VIN_{PP}$ | AC Input Voltage Range | 0 | | $AV_{DD}$-1.4 | V | CIS AC; INT $V_{DCREF}$<br>Mode Reg<br>=> XXX010XX<br>Gain=1 [1] |
| | AC Input Voltage Range | 0 | | $\Delta V_{REF}$ | V | CCD AC; INT $V_{DCREF}$<br>Mode Reg<br>=> XXX011XX<br>Gain=1 [1] |
| VIN | DC Input Voltage Range | -0.1 | | $AV_{DD}$-1.4 | V | CIS DC; INT $V_{DCREF}$<br>Mode Reg<br>=> XXX000XX<br>Gain=1 [2] |
| | DC Input Voltage Range | $V_{DCEXT}$ -0.1 | | $V_{DCEXT}$ +$\Delta V_{REF}$ | V | CIS DC; EXT $V_{DCREF}$<br>Mode Reg<br>=> XXX100XX<br>Gain=1 [3]<br>$V_{DCEXT}+\Delta V_{REF} \le AV_{DD}$ |
| $V_{DCEXT}$ | External DC Reference | 0.3 | | $AV_{DD}$/2 | V | CIS DC; EXT $V_{DCREF}$<br>Mode Reg<br>=> XXX100XX |
| $VIN_{BW}$ | Input Bandwidth | 10 | | | MHz | |
| $VIN_{CT}$ | Channel to Channel Crosstalk | | -60 | | dB | |
| **Internal Clamp Specifications** | | | | | | |
| $V_{CLAMP}$ | Clamp Voltage | | AGND | | V | CIS (AC) Mode |
| | Clamp Voltage | | $V_{RT}$ | | V | CCD (AC) Mode |
| $R_{INT}$ | Clamp Switch On Resistance | | 100 | 150 | Ω | |
| $R_{OFF}$ | Clamp Switch Off Resistance | 10 | | | MΩ | |

***Note:***

1 *$VIN_{PP}$ is the signal swing before the external capacitor tied to the MUX inputs.*

2 *The -0.1V minimum is specified in order to accommodate black level signals lower than the external DC reference (clamp) voltage.*

3 *The $V_{DCEXT}$-0.1V minimum is specified in order to accommodate black level signals lower than the external DC reference voltage.*

## ELECTRICAL CHARACTERISTICS

**Test Conditions: $AV_{DD}$=$DV_{DD}$=3.3V / 5V, ADCCLK=6MHz, 50% Duty Cycle, $T_A$=25°C unless otherwise specified.**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **System Specifications (MUX + Buffer + PGA + ADC)[1]** | | | | | | |
| $SYS_{DNL}$ | System DNL | | ±0.5 | | LSB | |
| $SYS_{LIN}$ | System Linearity | | ±1.0 | | % | |
| $SYS_{GE}$ | System Gain Error | -5.0 | | +5.0 | % | |
| IRN | Input Referred Noise | | TBD | | $\mu V_{rms}$ | Gain=1 |
| | Input Referred Noise | | TBD | | $\mu V_{rms}$ | Gain=10 |
| **System Timing Specifications** | | | | | | |
| tcklw | ADCCLK Low Pulse Width | 50 | 83 | | ns | |
| tckhw | ADCCLK High Pulse Width | 70 | 83 | | ns | |
| tckpd | ADCCLK Period | 120 | 166 | | ns | |
| tclpw | CLP Pulse Width | 30 | | | ns | [2] |

***Notes:***

1 *System performance is specified for typical digital system timing specifications.*

2 *The actual minimum 'tclpw' is dependent on the external capacitor value, the CIS output impedance, the Internal Clamp $R_{INT}$, and the maximum voltage across the external capacitor.*

*During 'clamp' operation, sufficient time needs to be allowed for the external capacitor to charge up to the correct operating level. Refer to the description in Theory of Operation, CIS Mode.*

### System Transfer Function

$$DB9{:}0_{CODE} = (2^{10} - 1)\ \frac{G\left\{ V_{SIG} + V_{BLK} + V_{ERREXT} + V_{ERRINT} - \left[ 0.8\left(\frac{DAC7{:}0_{CODE}}{255}\right) - 0.2\right]\right\}}{0.67\ A\ V_{DD}}$$

$$G = \left[1 + \left(\frac{9}{63}\right) GAIN5{:}0_{CODE}\right],$$

where
- $DB9{:}0_{CODE}$ => Numerical Representation of the Digital Output Between 0 and 1023;
- G => PGA Gain;
- $V_{SIG}$ => Signal Level;
- $V_{BLK}$ => Black Level, ($V_{IN}$=$V_{SIG}$ + $V_{BLK}$);
- $V_{ERREXT}$ => Difference between External Clamp Level and Black Level (±100 mV min/max);
- $V_{ERRINT}$ => Internal Offset Error (±100 mV min/max);
- $DAC7{:}0_{CODE}$ => Numerical Representation of the DAC Offset Adjustment Between 0 and 255.
- $GAIN5{:}0_{CODE}$ => Numerical Representation of the Gain Adjustment Between 0 and 63.

## ELECTRICAL CHARACTERISTICS

**Test Conditions: $AV_{DD}$=$DV_{DD}$=3.3V / 5V, ADCCLK=6MHz, 50% Duty Cycle, $T_A$=25°C unless otherwise specified.**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Write Timing Specifications** | | | | | | |
| tsclkw | SCLK Pulse Width | 40 | | | ns | |
| tds | Input Data Set-up Time | 20 | | | ns | |
| tdh | Input Data Hold Time | 0 | | | ns | |
| tdl | SCLK High to LD High | 50 | | | ns | |
| tdz | LD Low to SCLK High | 20 | | | ns | |
| **ADC Digital Output Specifications** | | | | | | |
| tap | Aperture Delay | | 10 | | ns | |
| tdv | Output Data Valid | | | 40 | ns | |
| tlat | Latency | | 3 | | cycles | |
| **Digital Input Specifications** | | | | | | |
| $V_{IH}$ | Input High Voltage | $AV_{DD}$-1 | | | V | |
| $V_{IL}$ | Input Low Voltage | | | 1 | V | |
| $I_{IH}$ | High Voltage Input Current | | 5 | | µA | |
| $I_{IL}$ | Low Voltage Input Current | | 5 | | µA | |
| $C_{IN}$ | Input Capacitance | | 10 | | pF | |
| **Digital Output Specifications** | | | | | | |
| $V_{OH}$ | Output High Voltage | 80 | | | (%) $DV_{DD}$ | $I_L$=1mA |
| $V_{OL}$ | Output Low Voltage | | | 20 | (%) $DV_{DD}$ | $I_L$=-1mA |
| $I_{OZ}$ | Output High-Z Leakage Current | -10 | | 10 | µA | |
| $C_{OUT}$ | Output Capacitance | | 10 | | pF | |
| $t_{SR}$ | Slew Rate (10% to 90% $DV_{DD}$) | 2 | | 15 | ns | $C_L$=10pF, $DV_{DD}$=3.3V |
| | Slew Rate (10% to 90% $DV_{DD}$) | TBD | | TBD | ns | $C_L$=10pF, $DV_{DD}$=5.0V |

## THEORY OF OPERATION

### CIS Mode (Contact Image Sensor)

The XRD9829 has two modes of operation for CIS applications. Each mode is set by the control registers accessed through the serial port.

**Mode 1. DC Coupled (Control Register D4:D3:D2, 000)**

If the CIS does not have leading or trailing black pixels as shown in Figure 1. then DC couple the CIS output to the XRD9829 input.

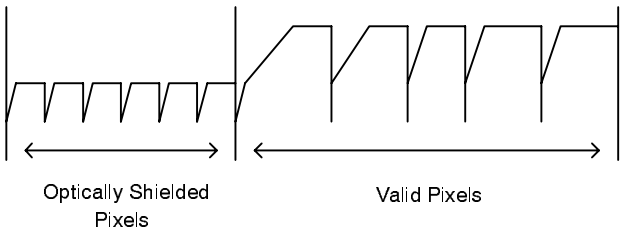



**Figure 1. Typical CIS Output**

Adjust the offset of the CIS (-100mV to 500mV) by setting the internal registers of the XRD9829 to set the black pixel value when the LEDs of the CIS are off. When the LEDs are on use the XRD9829 Programmable Gain to maximize the ADCs dynamic range. Figure 2. shows a typical application for a CIS with an offset of -100 mV to 500mV.

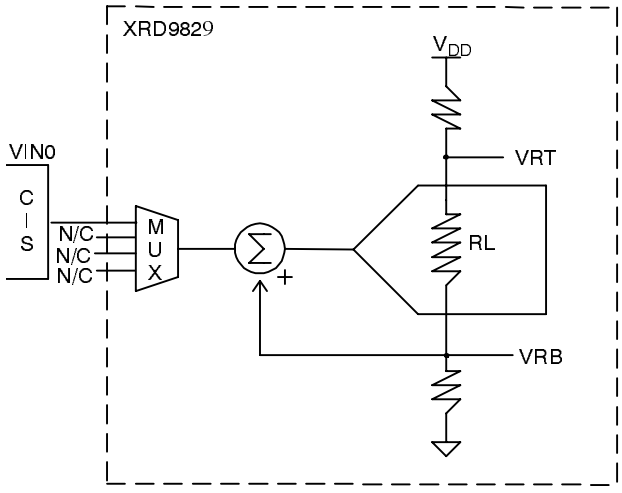



**Figure 2. Application With Offset in the Range (-100 mv to 500mv)**

The input is added to VRB before the signal passes through the ADC. If the CIS output is zero, then the output of the ADC will be zero code. This enables the CIS to be referenced to the bottom ladder reference voltage to use the full range of the ADC.

Some CIS sensors have an output with an offset voltage of greater than 500 mV. If the CIS output is beyond the offset range of the XRD9829 (see Offset Control DAC, Pg. 15) set the internal mode registers to external reference (Control Register D4:D3:D2, 100). An external reference voltage equal to the value of the CIS offset voltage can be applied to VIN3 (Figure 3.) in order to meet the dynamic range of the XRD9829. Figure 3. is a diagram of the XRD9829 in the external reference mode for CIS, DC Coupled applications.

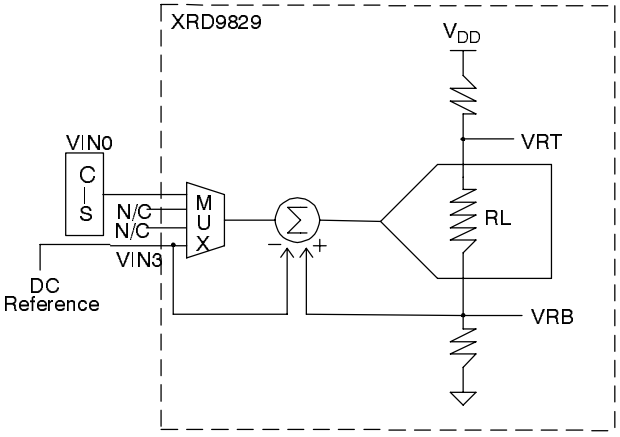



**Figure 3. Application with Offset Greater Than (-100mv to 500mv)**

The DC reference voltage applied to VIN3 does not have to be accurate. The internal offset DAC voltage is still used in this mode for fine adjustment. VIN3 cannot be used as an input from the CIS. Any signal applied to VIN3 will be subtracted from the output signal of the multiplexer.

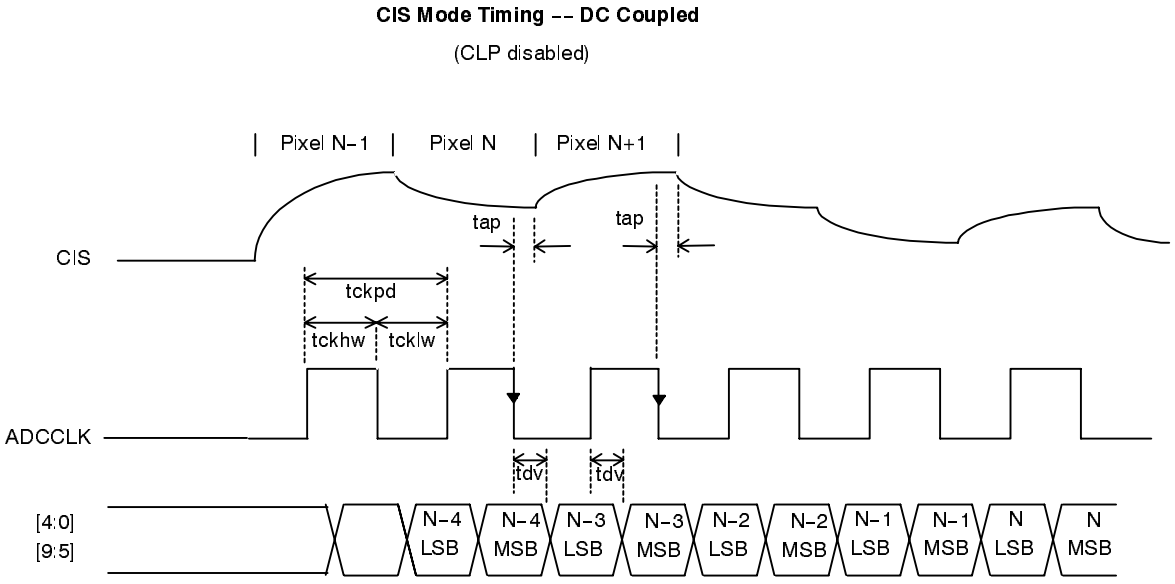



**Figure 4. Timing Diagram for Figure 2. and Figure 3.**

| CLK | Events |
|---|---|
| ↓ | ADC Sample & PGA Start Tracking next Pixel<br>LSB Data Out |
| ↑ | MSB Data Out |
| HI | ADC Track PGA Output |
| LO | ADC Hold/Convert |

**Mode 2. AC Coupled (Control Register D4:D3:D2, 010)**

If the CIS signal has a black reference for the video signal, an external capacitor $C_{EXT}$ is used. When CLP (clamp) pin is set high an internal switch allows one side of the external capacitor to be set to ground. It then is level shifted to correspond to the bottom ladder reference voltage of the ADC (Figure 5.).

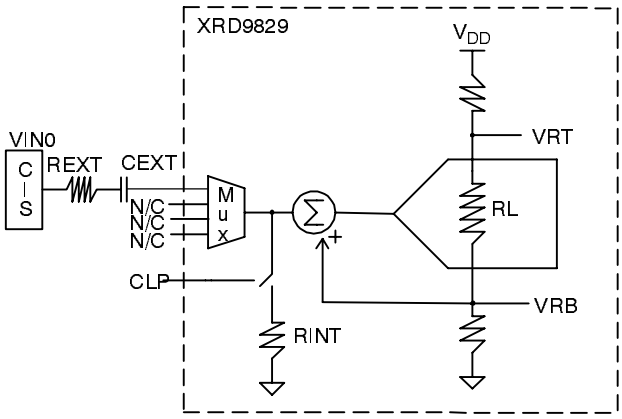



**Figure 5. CIS AC Coupled Application**

This value corresponds to the black reference of the image sensor. When the CLP pin is set back to low the ADC samples the video signal with respect to the black reference. The typical value for the external capacitor is 100pF. This value should be adjusted according to the time constant (Tc) needed in a particular application. The CLP pin has an internal 150 ohm impedance ($R_{INT}$) which is in series with the external capacitor ($C_{EXT}$).

Therefore, $Tc = 1/R_{INT}C_{EXT}$

If the input to the external capacitor has a load impedance ($R_{EXT}$), then

$T_c = 1/(R_{INT}+R_{EXT})C_{EXT}$

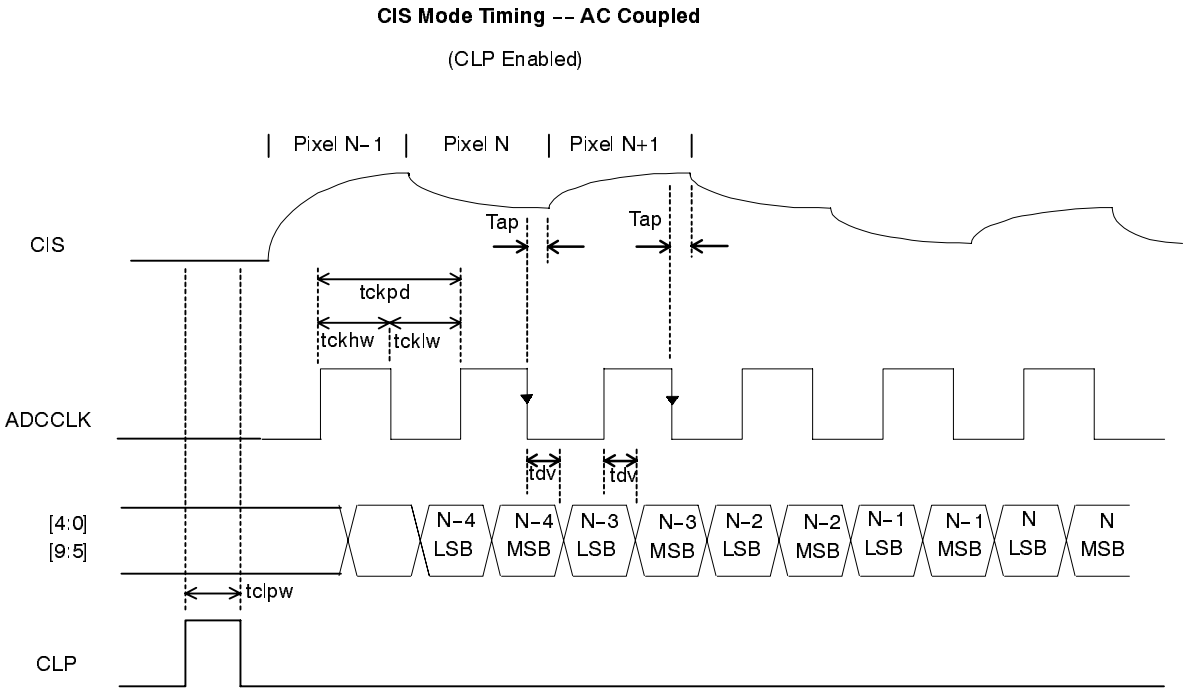



**Figure 6. Timing Diagram for Figure 5.**

| CLK | Events |
|---|---|
| ↓ | ADC Sample & PGA Start Track of next Pixel<br>LSB Data Out |
| ↑ | MSB Data Out |
| HI | ADC Track PGA Output |
| LO | ADC Hold/Convert |

| CLP | Events |
|---|---|
| HI | PGA Tracks $V_{CLAMP}$ & $C_{EXT}$ is Charged to $V_{BLACK} - V_{CLAMP}$ which is equal to $V_{BLACK}$ |
| LO | PGA Tracks $VIN_{PP}$ |

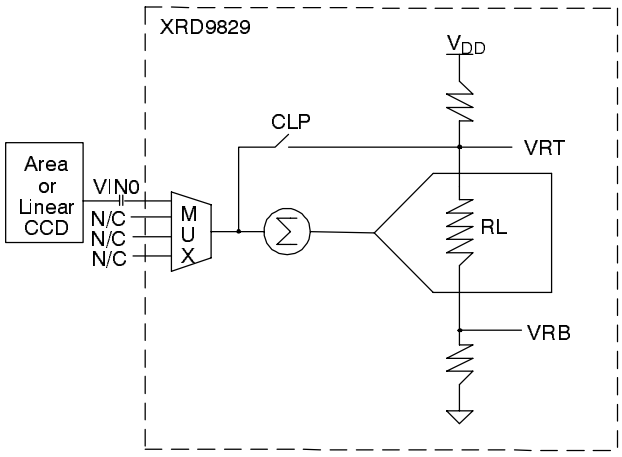



**Figure 7. CCD AC Coupled Application**

## CCD Mode (Charge Coupled Device)

### Mode 1. AC Coupled (Control Register D4:D3:D2, 011)

In the CCD mode of operation, an external capacitor needs to be chosen according to the equations below. The typical value for the external capacitor is 100pF. This value should be adjusted according to the time constant (Tc) needed in a particular application. The CLP pin has an internal 150 ohm impedance ($R_{INT}$) which is in series with the external capacitor ($C_{EXT}$).

Therefore, $Tc = 1/R_{INT}C_{EXT}$

If the input to the external capacitor has a load impedance ($R_{EXT}$), then

$T_c = 1/(R_{INT}+R_{EXT})C_{EXT}$

When CLP (clamp) pin is set high an internal switch allows one side of the external capacitor to be set to VRT (Figure 7.). This value corresponds to the black reference of the CCD. When the CLP pin is set back to low the ADC samples the video signal with respect to the black reference. The difference between the black reference and the video signal is the actual pixel value of the video content. Since this value is referenced to the top ladder reference voltage of the ADC a zero input signal would yield a full scale output code. Therefore, the output of the conversion is inverted (internally) to correspond to zero scale output code.

### Area or Linear CCD Applications

Figure 7. is a block diagram for applications with Area or Linear CCDs (The timing for Area CCDs and B/W CCDs is the same). For Area or Linear CCD applications a global offset is loaded into the serial port at the beginning of a line. The gain is set to adjust for the highest color intensity of the CCD output. Once the pixel values have been sampled the gain and offset are adjusted at the beginning of the next line. For example, if there is a line to line variation between the black reference pixels the offset is adjusted. The gain is always adjusted for the highest color intensity.

### Triple Channel CCD Application

Figure 8. is a block diagram for applications with triple channel CCDs. During the optically shielded section of a pixel CLP must go high three times to store the black reference on each capacitor to the input. In between the CLP pulses the MUX is internally programmed to the next input selection along with the required offset. Accordingly, the time constant will be higher for this application. Once the black reference is stored on the external capacitors the ADC samples the selected output channel. The MUX is internally programmed to the next input selection along with the gain and offset adjustments associated with the new color pixel being sampled. The ADC samples the new output, and this process is repeated until all three CCD outputs have been sampled. As before, the LSBs are available on the output bus on the

falling edge of ADCCLK. The MSBs are available on the rising edge of ADCCL

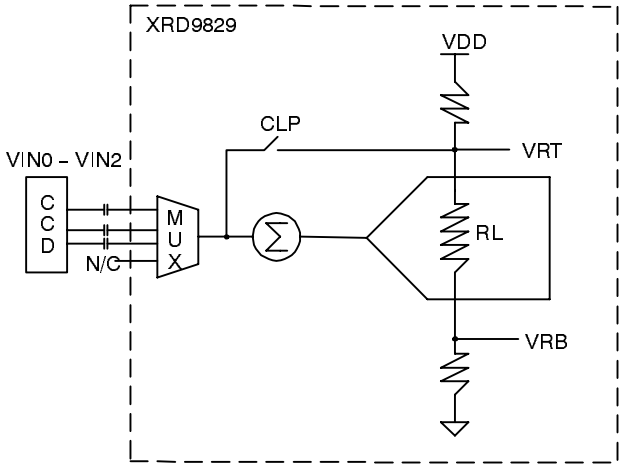



**Figure 8. CCD AC Coupled Application**

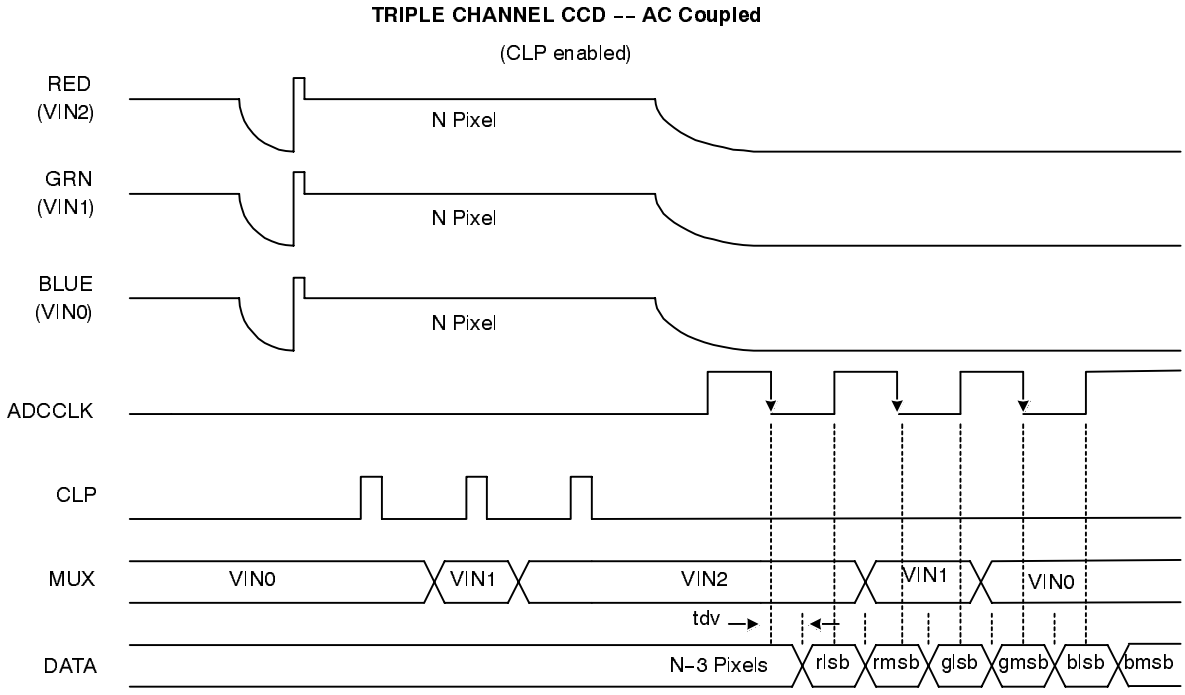



**Figure 9. Timing Diagram for Figure 8.**

| CLK | Events |
|---|---|
| ↓ | ADC Sample & PGA Start Track of next Pixel $V_{CLAMP}$<br>LSB Data Out |
| ↑ | MSB Data Out |
| HI | ADC Track PGA Output |
| LO | ADC Hold/Convert |
| **CLP** | **Events** |
| HI | PGA Tracks $V_{CLAMP}$ & $C_{EXT}$ is Charged to $V_{BLACK}$ – $V_{CLAMP}$, which is equal to $V_{BLACK}$ – $V_{RT}$ |
| LO | PGA Tracks $VIN_{PP}$ |

**Mode 2. DC Coupled (Control Register D4:D3:D2, 001)**

Typical CCDs have outputs with black references. Therefore, DC Coupled is not recommended for CCD applications.

**Offset Control DAC**

The offset DAC is controlled by 8 bits. The offset range is 800mV ranging from -200mV to +600mV. Therefore, the resolution of the 8-bit offset DAC is 3.14mV. However, the XRD9829 has +/-100mV reserved for internal offsets. Therefore the effective range for adjusting for CIS offsets or black reference is -100mV to +500mV. The offset adjustment is used primarily to correct for the difference between the black level of the image sensor and the bottom ladder reference voltage (VRB) of the ADC. By adjusting the black level to correspond to VRB the entire range of the ADC can be used.

If the offset of the CIS output is greater than 500mV an external reference can be applied to VIN3. The external reference can be used to adjust for large offsets only when the internal mode is configured through the serial port.

Since the offset DAC adjustment is done before the gain stage it is gain–dependent. For example: If the gain needs to be changed between lines (red to blue, etc.) the offset is calibrated before the signal passes through the PGA.

### PGA (Programmable Gain Amplifier) DAC

The gain of the input waveform is controlled by a 6-bit PGA. The PGA is used along with the offset DAC for the purpose of using the entire range of the ADC. The PGA has a linear gain from 1 to 10. Figure 10. is a plot of the transfer curve for the PGA gain.

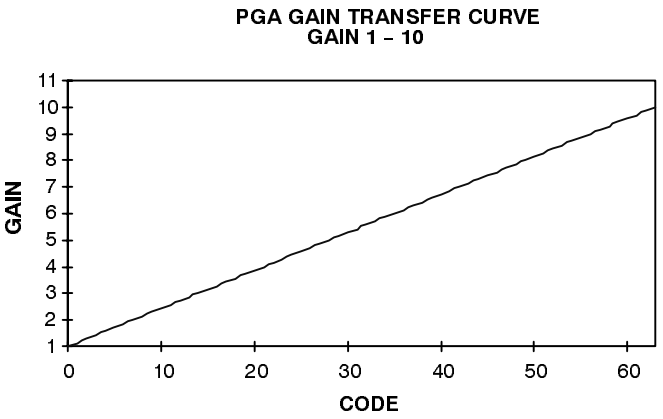



**Figure 10. Transfer Curve For The 6-Bit PGA**

After the signal is level shifted to correspond with the bottom ladder reference voltage, the system can be calibrated such that a white video pixel can represent the top ladder reference voltage to the ADC. This allows for a full scale conversion maximizing the resolution of the ADC.

### Analog to Digital Converter

The ADC is a 10-bit, 10 MSPS analog-to-digital converter for high speed and high accuracy. The ADC uses a subranging architecture to maintain low power consumption at high conversion rates. The output of the ADC is a 5-bit databus. ADCCLK samples the input on its falling edge. After the input is sampled the LSB is latched to the output drivers. On the rising edge of the ADCCLK, the MSB is latched to the output drivers. The output needs to be demultiplexed with external circuitry or a digital ASIC. There is a three clock cycle latency for the analog-to-digital converter.

The VRT and VRB reference voltages for the ADC are generated internally, unless the external $V_{RT}$ mode (D5 set to [1]) is selected. In the external $V_{RT}$ mode, the $V_{RT}$ voltage is set through the VREF+ pin. This allows the user to select the dynamic range of the ADC.

### Serial Load Control Registers

The serial load registers are controlled by a standard three wire serial interface. LD, SCLK and SDATA are the three input signals that control this process. The LD signal is set low to initiate the loading of the internal registers.

There are four internal mode registers that are accessed via a 10–bit data string. The SDATA is latched automatically after ten SCLKs have been counted. If ten clocks are not present on SCLK before the LD signal returns high, no data will be loaded into the internal registers. If more than 10 clocks are present on SCLK, the additional clocks will be ignored. The data corresponding to the first ten SCLKs will be loaded only.

The first two MSBs choose which internal register will be selected. The remaining 8 LSBs contain the data needed for programming the internal register for a particular configuration.

### Power Up State of the Internal Registers

The control register settings upon intial power up are for CIS, DC Coupled Mode (VRT is set to internal, Input DC Reference=AGND and MUX input VIN0). Gain and Offset are set to zero. The test modes are disabled in the power up state.

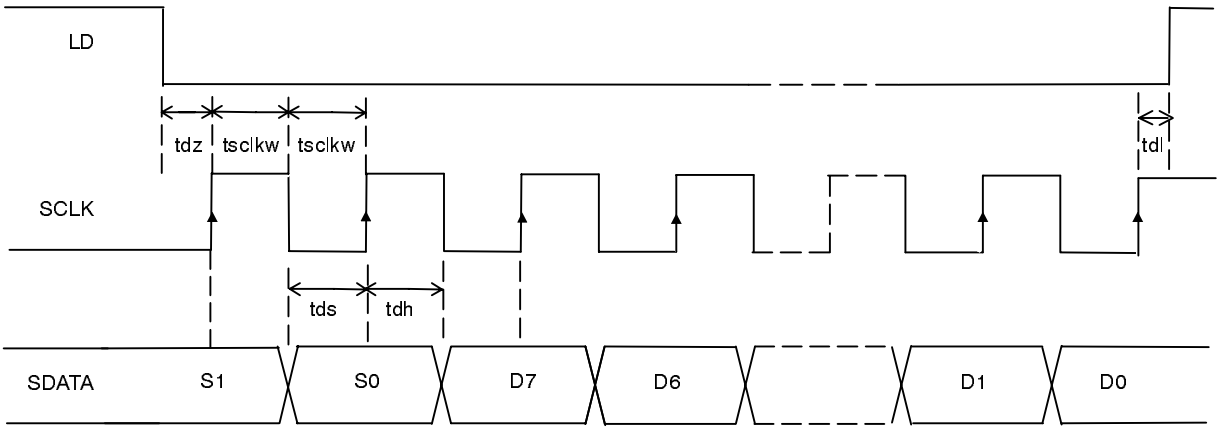



**Figure 11. Write Timing Diagram**

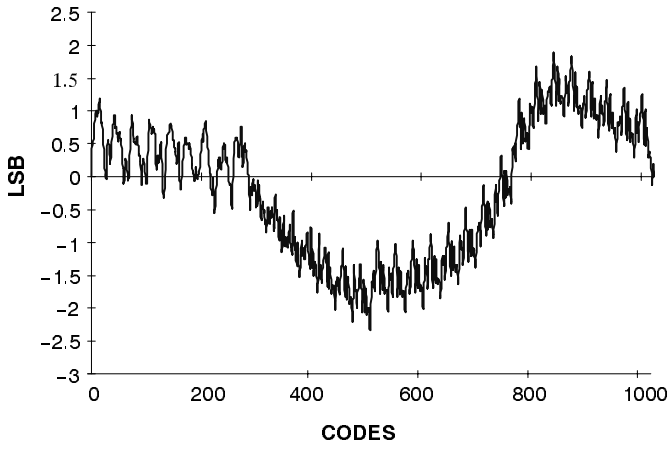
## Control Registers

| Function (Register S1/S0) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Power-up State (Note 1) |
|---|---|---|---|---|---|---|---|---|---|
| **Gain (00)** | G5 (MSB) | G4 | G3 | G2 | G1 | G0 (LSB) | X | X | 000000XX |
| **Offset (01)** | O7 (MSB) | O6 | O5 | O4 | O3 | O2 | O1 | O0 (LSB) | 01000000 |
| **Mode (10)** | X | X | $V_{RT}$ 0: INTERNAL 1: EXTERNAL | INPUT DC REFERENCE ($V_{DCREF}$) 0:INTERNAL ($V_{DCREF}$= AGND) 1: EXTERNAL ($V_{DCREF}$=$V_{DCEXT}$) | DC/AC 0: DC 1: AC | CIS/CCD 0: CIS 1: CCD | MUX SEL 0 0: VIN0 0 1: VIN1 1 0: VIN2 1 1: VIN3 | MUX SEL 0 0: VIN0 0 1: VIN1 1 0: VIN2 1 1: VIN3 | XX000000 |
| **Mode & Test (11)** | X | X | X | DIGITAL RESET 0: NO RESET 1: RESET (REGISTERS ARE RESET TO POWER-UP STATES) | TEST3 0: TEST3 DISABLED 1: OUTPUT OF BUFFER TIED TO VIN3 PIN (VIN3 PIN BECOMES AN OUTPUT) | TEST2 0: TEST2 DISABLED 1: OUTPUT OF PGA TIED TO VIN2 PIN (VIN2 PIN BECOMES AN OUTPUT) | TEST1 0: TEST1 DISABLED 1: VIN1 PIN TIED TO INPUT OF ADC (PGA OUTPUT DISCONNECTED FROM INPUT OF ADC) | X | XXX0000X |

***Note:***

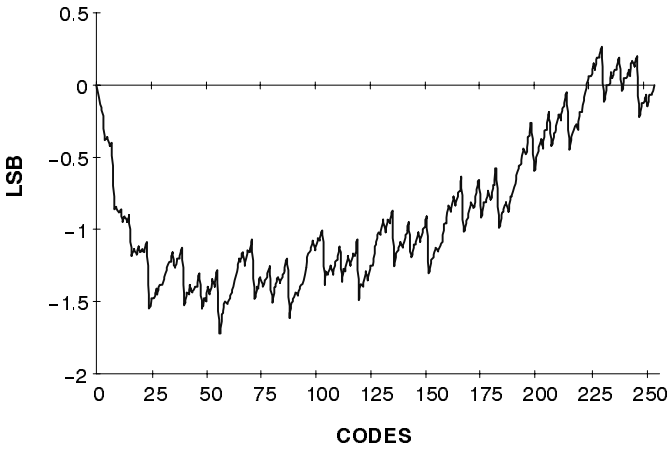
*1 These are the control register settings upon initial power-up. The previous register settings are retained following a logic power-down initiated by the PDB signal.*

XRD9829 ADC
INL



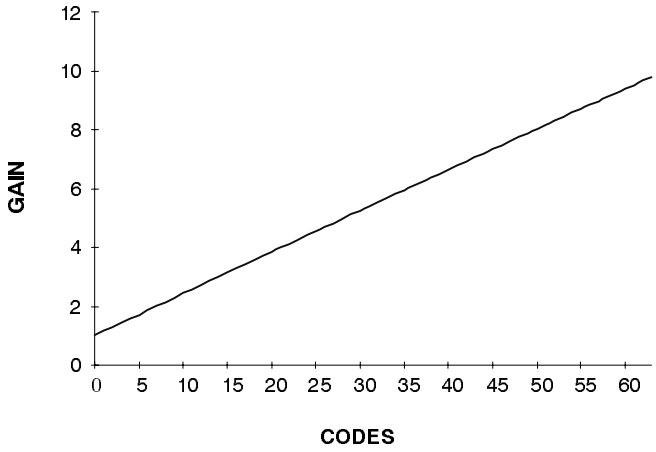

Graph 1.

XRD9829 OFFSET DAC
INL




Graph 2.

XRD9829 GAIN DAC
LINEARITY



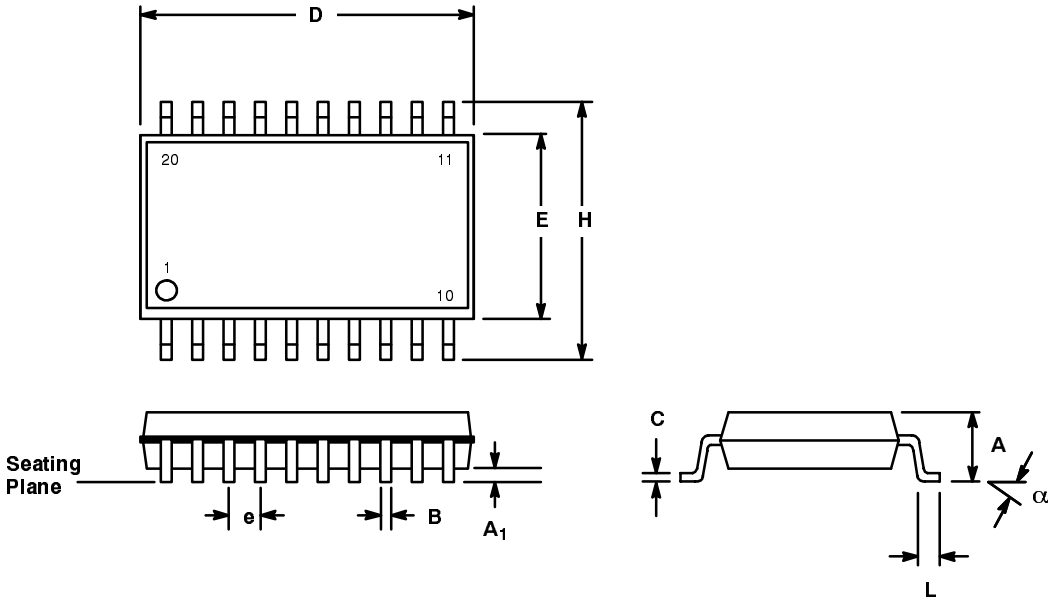

Graph 3.

XRD9829 GAIN DAC INL


Graph 4.

## 20 LEAD SMALL OUTLINE
## (300 MIL JEDEC SOIC)

*Rev. 1.00*




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| $A_1$ | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| D | 0.496 | 0.512 | 12.60 | 13.00 |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| α | 0° | 8° | 0° | 8° |

*Note: The control dimension is the millimeter column*

# Notes

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