



CYPRESS

CY24130

HOTLink II™ SMPTE Receiver Training Clock

Features

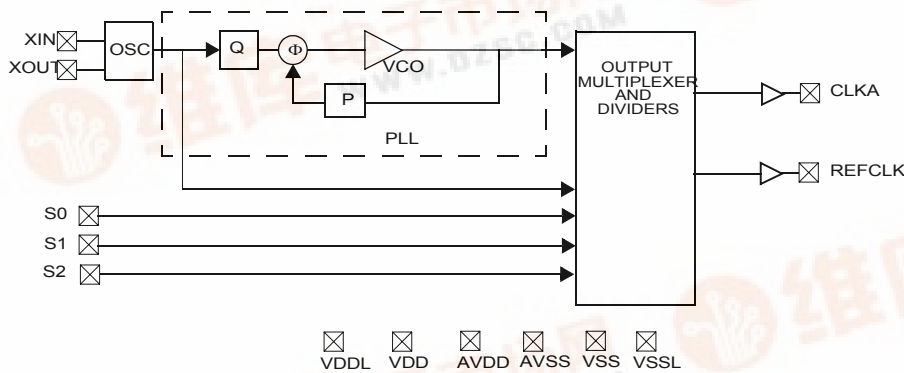
- Integrated phase-locked loop
- Low-jitter, high-accuracy outputs
- 3.3V operation

Benefits

- Internal PLL with up to 400-MHz internal operation
- Meets critical timing requirements in complex system designs
- Enables application compatibility

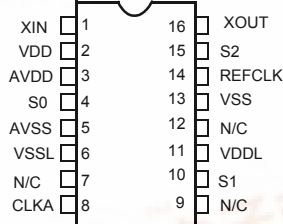
Part Number	Outputs	Input Frequency	Output Frequency Range
CY24130-1	2	27 MHz (Driven Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)
CY24130-2	2	27 MHz (Crystal Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)

Logic Block Diagram



Pin Configuration

CY24130-1, -2
16-pin TSSOP



Frequency Select Options

S2	S1	S0	CLKA	REFCLK	Units
0	0	0	27	27	MHz
0	0	1	36	27	MHz
0	1	0	54	27	MHz
0	1	1	148.50	27	MHz
1	0	0	74.25	27	MHz
1	0	1	OFF, pulled low	27	MHz
1	1	0	OFF, pulled low	27	MHz
1	1	1	OFF, pulled low	27	MHz

Pin Description

Name	Pin Number	Description
XIN	1	Reference Crystal Input.
V _{DD}	2	Voltage Supply.
AV _{DD}	3	Analog Voltage Supply.
S0	4	Frequency Select 0.
AV _{SS}	5	Analog Ground.
V _{SSL}	6	VDDL Ground.
N/C	7	No Connect.
CLKA	8	27-/36-/54-/148.50-/74.25-MHz Clock Output (frequency selectable).
N/C	9	No Connect.
S1	10	Frequency Select 1.
V _{DDL}	11	Voltage Supply.
N/C	12	No Connect.
VSS	13	Ground.
REFCLK	14	Reference Clock Output.
S2	15	Frequency Select 2.
XOUT	16	Reference Crystal Output. Leave floating for -1.

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V _{DD} , AV _{DD}	Supply Voltage	-0.5	7.0	V
V _{DDL}	I/O Supply Voltage	-	7.0	V
T _J	Junction Temperature	-	125	°C
	Digital Inputs	AV _{SS} - 0.3	AV _{DD} + 0.3	V
	Electro-Static Discharge	2	-	kV

Recommended Operating Conditions

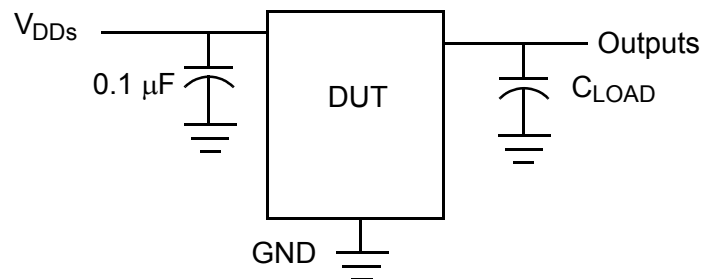
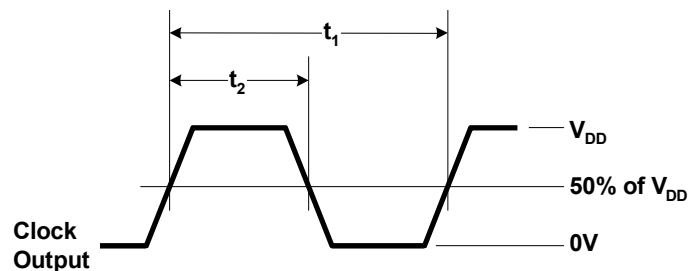
Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD} /AV _{DDL} /V _{DDL}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0	-	70	°C
C _{LOAD}	Max. Load Capacitance	-	-	15	pF
f _{REF}	Reference Frequency	-	27	-	MHz
C _{LNOM}	Nominal Parallel Crystal Load Capacitance for -2	-	18	-	pF

DC Electrical Specifications

Parameter ^[1]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24	–	mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	–	5	10	μA
I_{IL}	Input Low Current	$V_{IL} = 0V$	–	–	10	μA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	–	V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3	V
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current	–	16	–	mA
I_{VDDL}	Supply Current	V_{DDL} Current	–	14	–	mA

AC Electrical Specifications

Parameter ^[1]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> ; t_1/t_2 , 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.8	1.4	–	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.8	1.4	–	V/ns
t_9	Clock Jitter	CLKA Peak-Peak Period Jitter	–	100	–	ps
t_{10}	PLL Lock Time		–	–	3	ms

Test and Measurement Set-up

Voltage and Timing Definitions

Figure 1. Duty Cycle Definitions
Note:

1. Not 100% tested.

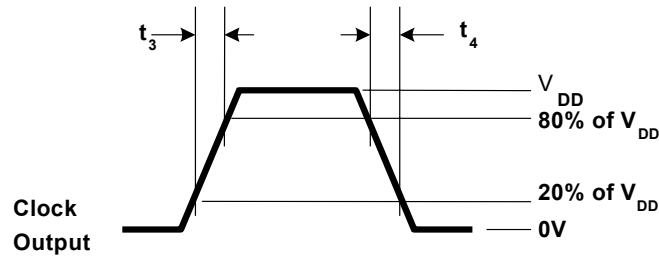


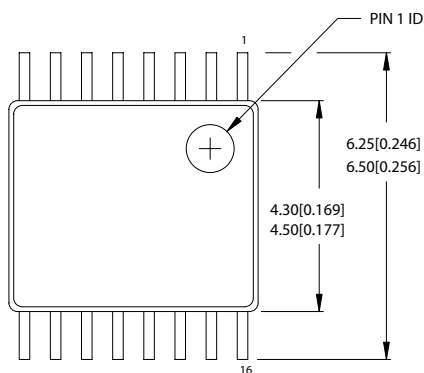
Figure 2. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
Lead-free			
CY24130ZXC-1	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-1T	16-Pin TSSOP – Tape and Reel	Commercial	3.3V
CY24130ZXC-2	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-2T	16-Pin TSSOP – Tape and Reel	Commercial	3.3V

Package Drawing and Dimensions

16-lead TSSOP 4.40 MM Body Z16.173

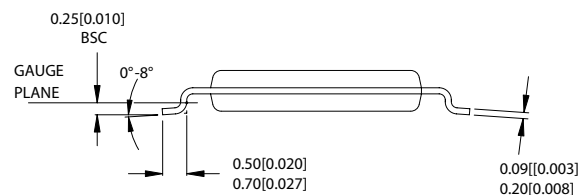
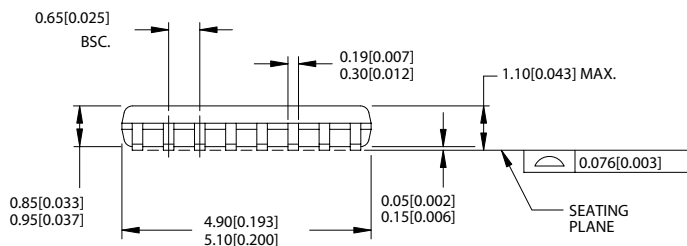


DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.



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Document History Page

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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	314514	See ECN	RGL	New Data Sheet