



CY28351

Differential Clock Buffer/Driver DDR400- and DDR333-Compliant

Features

- Supports 333-MHz and 400-MHz DDR SDRAM
- 60 – 200-MHz operating frequency
- Phase-locked loop (PLL) clock distribution for double data rate synchronous DRAM applications
- Distributes one clock input to ten differential outputs
- External feedback pin (FBIN) is used to synchronize the outputs to the clock input
- Conforms to the DDRI specification
- Spread Aware for electromagnetic interference (EMI) reduction
- 48-pin SSOP package

Description

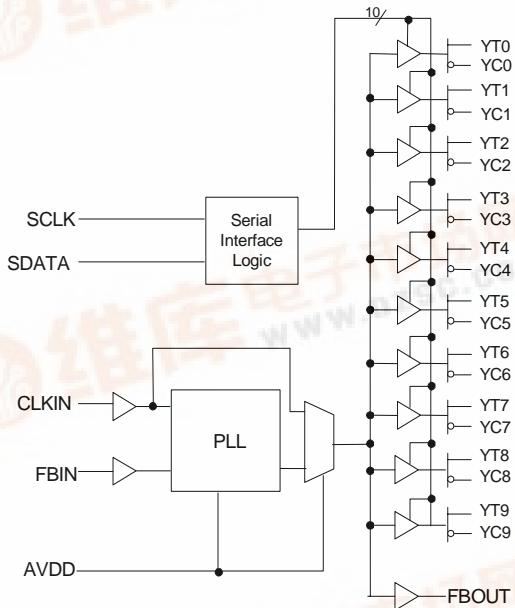
This PLL clock buffer is designed for 2.5-V_{DD} and 2.5-AV_{DD} operation and differential outputs levels.

This device is a zero delay buffer that distributes a clock input (CLKIN) to ten differential pairs of clock outputs (YT[0:9], YC[0:9]) and one feedback clock output (FBOUT). The clock outputs are individually controlled by the serial inputs SCLK and SDATA.

The two-line serial bus can set each output clock pair (YT[0:9], YC[0:9]) to the Hi-Z state. When AV_{DD} is grounded, the PLL is turned off and bypassed for the test purposes.

The PLL in this device uses the input clock (CLKIN) and the feedback clock (FBIN) to provide high-performance, low-skew, low-jitter output differential clocks.

Block Diagram



Pin Configuration

VSS	1	•	48	VSS
YC0	2		47	YC5
YT0	3		46	YT5
VDDQ	4		45	VDDQ
YT1	5		44	YT6
YC1	6		43	YC6
VSS	7		42	VSS
VSS	8		41	VSS
YC2	9		40	YC7
YT2	10		39	YT7
VDD	11		38	VDDQ
SCLK	12		37	SDATA
CLKIN	13		36	NC
NC	14		35	FBIN
VDDI	15		34	VDDQ
AVDD	16		33	FBOUT
AVSS	17		32	NC
VSS	18		31	VSS
YC3	19		30	YC8
YT3	20		29	YT8
VDDQ	21		28	VDDQ
YT4	22		27	YT9
YC4	23		26	YC9
VSS	24		25	VSS

CY28351

Pin Description^[1]

Pin Number	Pin Name	I/O	Pin Description	Electrical Characteristics
13	CLKIN	I	Clock Input.	Input
35	FBIN	I	Feedback Clock Input. Connect to FBOUT for accessing the PLL.	Input
3, 5, 10, 20, 22 46, 44, 39, 29, 27	YT(0:9)	O	Clock Outputs.	Differential Outputs
2, 6, 9, 19, 23 47, 43, 40, 30, 26	YC(0:9)	O	Clock Outputs.	
33	FBOUT	O	Feedback Clock Output. Connect to FBIN for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	Output
12	SCLK	I	Serial Clock Input. Clocks data at SDATA into the internal register.	Data Input for the two-line serial bus
37	SDATA	I/O	Serial Data Input. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.	Data Input and Output for the two-line serial bus
11	VDD		2.5V Power Supply for Logic.	2.5V Nominal
4, 21, 28, 34, 38, 45	VDDQ		2.5V Power Supply for Output Clock Buffers.	2.5V Nominal
16	AVDD		2.5V Power Supply for PLL.	2.5V Nominal
15	VDDI		2.5V Power Supply for Two-line Serial Interface.	2.5V Nominal
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	VSS		Common Ground.	0.0V Ground
17	AVSS	-	Analog Ground.	0.0V Analog Ground
14, 32, 36	NC		Not Connected.	

Zero Delay Buffer

When used as a zero delay buffer, the CY28351 will likely be in a nested clock tree application. For these applications the CY28351 offers a clock input as a PLL reference. The CY28351 then can lock onto the reference and translate with near zero delay to low skew outputs. For normal operation, the external feedback input, FBIN, is connected to the feedback output, FBOUT. By connecting the feedback output to the feedback input the propagation delay through the device is

eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When V_{DDA} is strapped LOW, the PLL is turned off and bypassed for test purposes.

Function Table

Input		Outputs			PLL
VDDA	CLKIN	YT(0:9) ^[2]	YC(0:9) ^[2]	FBOUT	
GND	L	L	H	L	BYPASSED/OFF
GND	H	H	L	H	BYPASSED/OFF
2.5V	L	L	H	L	On
2.5V	H	H	L	H	On
2.5V	< 20 MHz	Hi-Z	Hi-Z	Hi-Z	Off

Notes:

1. A bypass capacitor (0.1 μ F) should be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.
2. Each output pair can be three-stated via the two-line serial interface.

Power Management

The individual output enable/disable control of the CY28351 allows the user to implement unique power management schemes into the design. Outputs are three-stated when disabled through the two-line interface as individual bits are set LOW in Byte0 and Byte1 registers. The feedback output (FBOUT) cannot be disabled via two line serial bus. The enabling and disabling of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks.

Byte0: Output Register 1 (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	3, 2	YT0, YC0
6	1	5, 6	YT1, YC1
5	1	10, 9	YT2, YC2
4	1	20, 19	YT3, YC3
3	1	22, 23	YT4, YC4
2	1	46, 47	YT5, YC5
1	1	44, 43	YT6, YC6
0	1	39, 40	YT7, YC7

Byte1: Output Register 2 (1 = Enable, 0 = Disable)

Bit	@Pup	Pin#	Description
7	1	29, 30	YT8, YC8
6	1	27, 26	YT9, YC9
5	0	—	Reserved
4	0	—	Reserved
3	0	—	Reserved
2	0	—	Reserved
1	0	—	Reserved
0	0	—	Reserved

Byte2: Test Register 3

Bit	@Pup	Pin#	Description
7	1	—	0 = PLL leakage test, 1 = disable test
6	1	—	Reserved
5	1	—	Reserved
4	1	—	Reserved
3	1	—	Reserved
2	1	—	Reserved
1	1	—	Reserved
0	1	—	Reserved

Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:

- Command Code byte
- Byte Count byte.

Maximum Ratings^[3]

Input Voltage Relative to V_{SS} :	$V_{SS} - 0.3V$
Input Voltage Relative to V_{DDQ} or $A V_{DD}$:	$V_{DD} + 0.3V$
Storage Temperature:	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature:	$0^{\circ}C$ to $+70^{\circ}C$
Maximum Power Supply:	3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range:

$$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters $V_{DD} = V_{DDA} = V_{DDQ} = V_{DDI} = 2.5V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ ^[4]

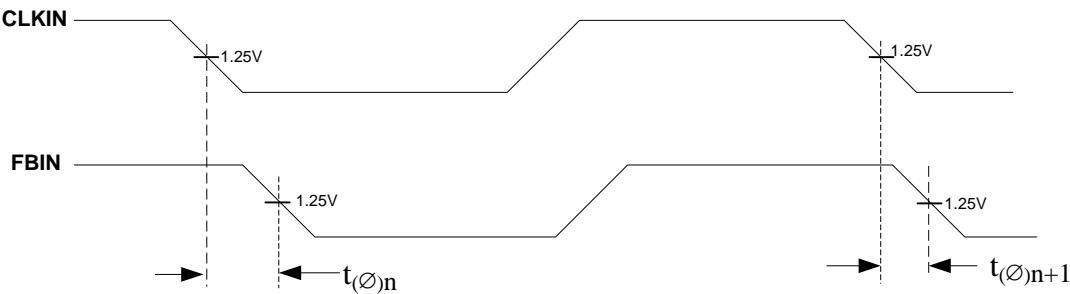
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	SDATA , SCLK			1.0	V
V_{IH}	Input High Voltage	SDATA , SCLK	2.2			V
V_{IL}	Input Voltage Low	CLKIN, FBIN			0.4	V
V_{IH}	Input Voltage High	CLKIN, FBIN	2.1			V
I_{IN}	Input Current	$V_{IN} = 0V$ or $V_{IN} = V_{DDQ}$, CLKT, FBIN	-10		10	μA
I_{OL}	Output Low Current	$V_{DDQ} = 2.375V$, $V_{OUT} = 1.2V$	26	35		mA
I_{OH}	Output High Current	$V_{DDQ} = 2.375V$, $V_{OUT} = 1V$	-18	-32		mA
V_{OL}	Output Low Voltage	$V_{DDQ} = 2.375V$, $I_{OL} = 12$ mA			0.6	V
V_{OH}	Output High Voltage	$V_{DDQ} = 2.375V$, $I_{OH} = -12$ mA	1.7			V
V_{OUT}	Output Voltage Swing ^[5]		1.1		$V_{DDQ} - 0.4$	V
V_{OC}	Output Crossing Voltage ^[6]		$(V_{DDQ}/2) - 0.2$	$V_{DDQ}/2$	$(V_{DDQ}/2) + 0.2$	V
I_{OZ}	High-Impedance Output Current	$V_O = GND$ or $V_O = V_{DDQ}$	-10		10	μA
I_{DDQ}	Dynamic Supply Current ^[7]	All V_{DDQ} and V_{DDI} , $f_O = 170$ MHz		235	300	mA
I_{DSTAT}	Static Supply Current				1	mA
I_{DD}	PLL Supply Current	V_{DDA} only		9	12	mA
C_{IN}	Input Pin Capacitance			4	6	pF

AC Parameters $V_{DD} = V_{DDQ} = 2.5V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ ^[8,9]

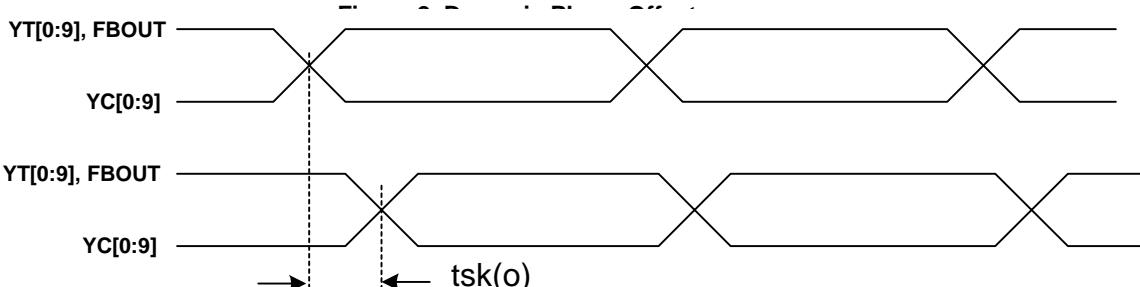
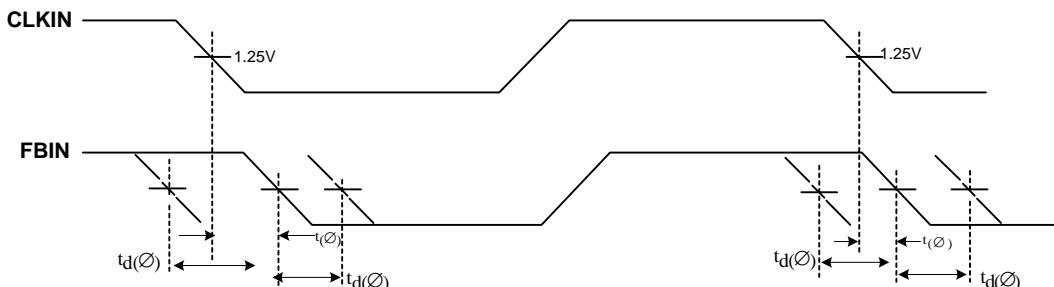
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{CLK}	Operating Clock Frequency		60		200	MHz
t_{DC}	Input Clock Duty Cycle		40		60	%
t_{LOCK}	Maximum PLL lock Time				100	μs
$t_{R/Tf}$	Output Clocks Slew Rate	20% to 80% of VOD	1		2.5	V/ns
t_{pZL}, t_{pZH}	Output Enable Time (all outputs) ^[10]			3		ns
t_{pLZ}, t_{pHZ}	Output Disable Time (all outputs) ^[10]			3		ns
t_{CCJ}	Cycle to Cycle Jitter ^[12]	$f > 66$ MHz	-100		100	ps
$t_{jit(h-per)}$	Half-period jitter ^[12]	$f > 66$ MHz	-100		100	ps
t_{PLH}	LOW-to-HIGH Propagation Delay, CLKIN to YT		1.5	3.5	6	ns
t_{PHL}	HIGH-to-LOW Propagation Delay, CLKIN to YT		1.5	3.5	6	ns
t_{SKEW}	Any Output to Any Output Skew ^[11]				100	ps
t_{PHASE}	Phase Error ^[11]		-150		150	ps
t_{PHASEJ}	Phase Error Jitter	$f > 66$ MHz	-50		50	ps

Notes:

3. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
4. unused inputs must be held HIGH or LOW to prevent them from floating.
5. For load conditions, see *Figure 7*.
6. The value of V_{OC} is expected to be $|V_{TR} + V_{CP}|/2$. In case of each clock directly terminated by a 120Ω resistor. See *Figure 7*.
7. All outputs switching loaded with 16 pF in 600 Ω environment. See *Figure 7*.
8. Parameters are guaranteed by design and characterization. Not 100% tested in production
9. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 33.3 kHz with a down spread of -0.5%.
10. Refers to transition of non-inverting output.
11. All differential input and output terminals are terminated with $120\Omega/16$ pF, as shown in *Figure 7*.
12. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.

Parameter Measurement Information


$$t_{(\emptyset)n} = \frac{\sum_{n=1}^N t_{(\emptyset)n}}{N} \quad (N \text{ is large number of samples})$$

Figure 1. Static Phase Offset

Figure 3. Output Skew

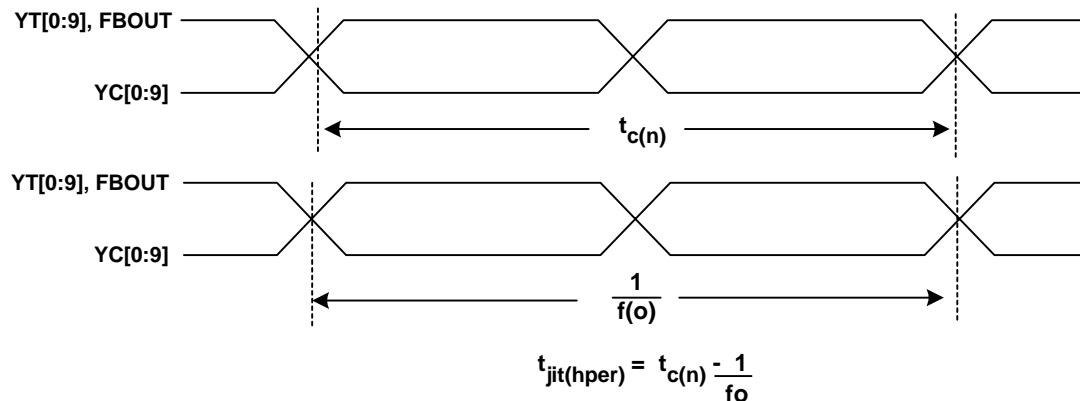


Figure 4. Period Jitter

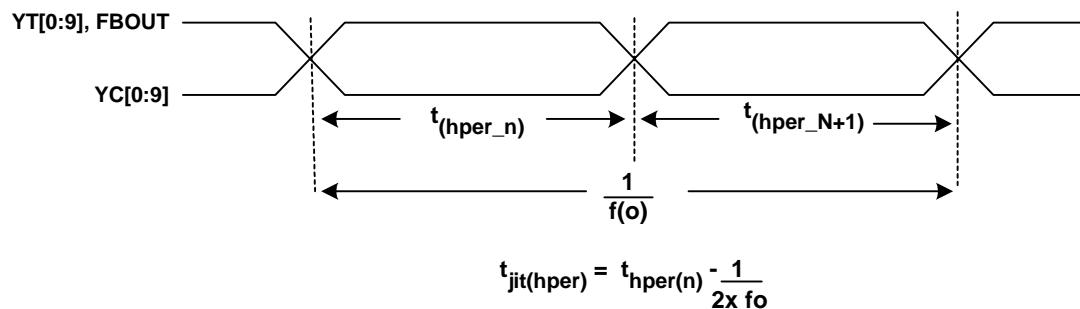


Figure 5. Half-Period Jitter

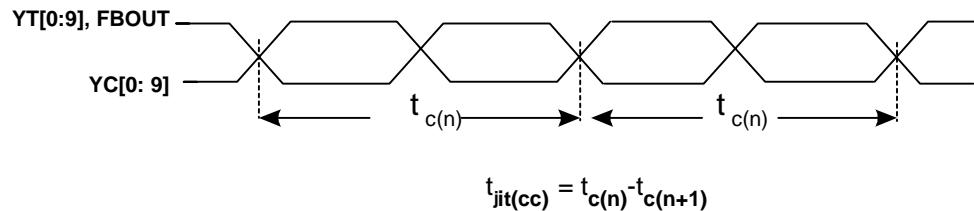


Figure 6. Cycle-to-Cycle Jitter

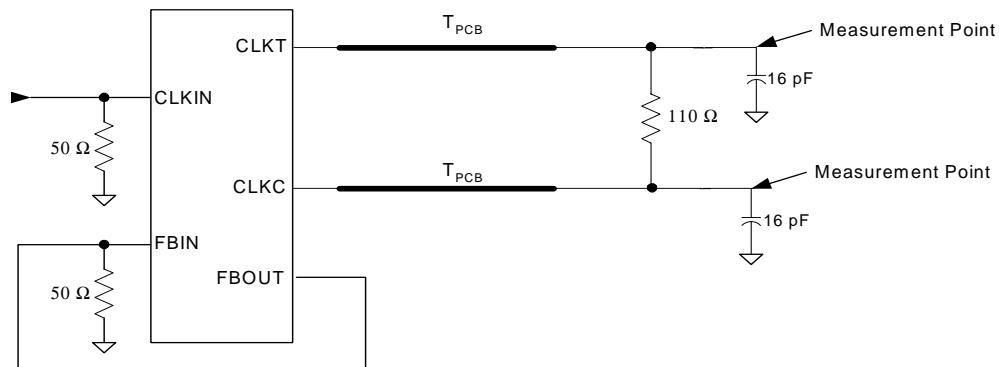
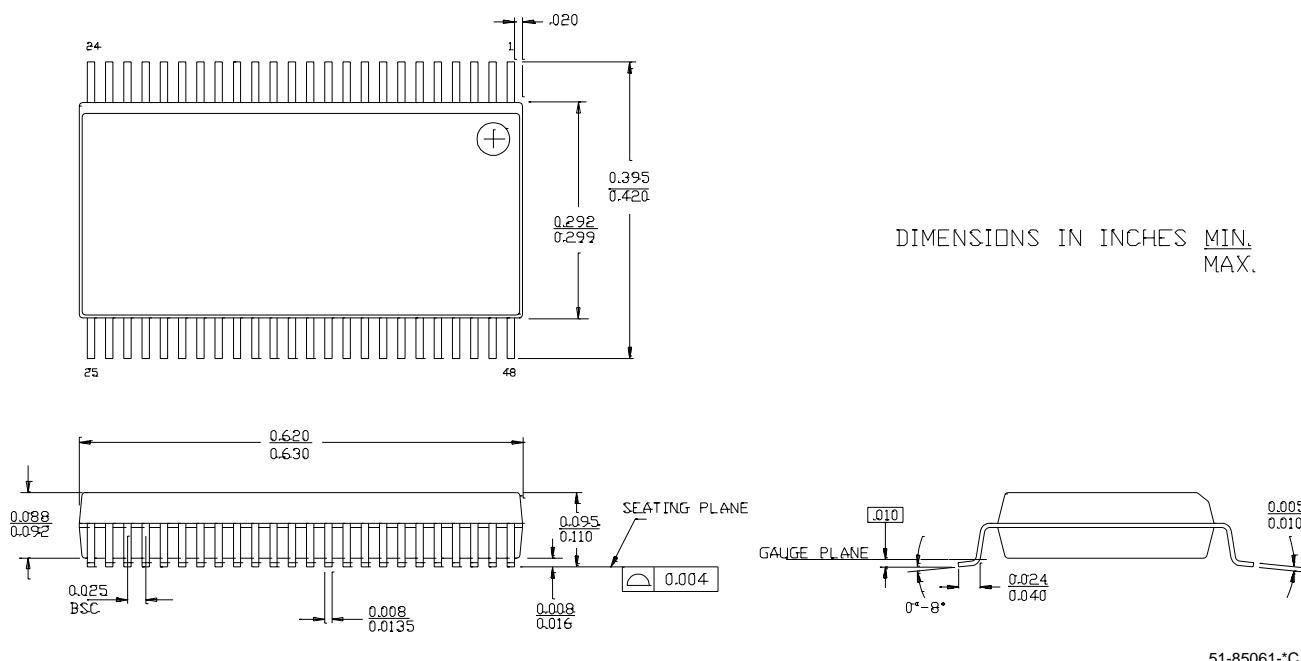


Figure 7. Differential Output Jitter Measurement Setup

Ordering Information

Part Number	Package Type	Product Flow
CY28351OC	48-pin SSOP	Commercial, 0° to 70°C
CY28351OCT	48-pin SSOP—Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions
48-lead Shrunk Small Outline Package O48


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Document History Page

Document Title: CY28351 Differential Clock Buffer/Driver, DDR400- and DDR333-Compliant
Document Number: 38-07370

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112786	05/08/02	DMG	New Data Sheet
*A	122910	12/26/02	RBI	Add power up requirements to maximum ratings information
*B	127011	05/28/03	RGL	Change the maximum operating clock frequency from 170 MHz to 200 MHz Added DDR400- and DDR333-Compliant in the title.