Integrated Circuit Systems, Inc.

ICS9342

133MHz Clock Generator and Integrated Buffer for PowerPC™

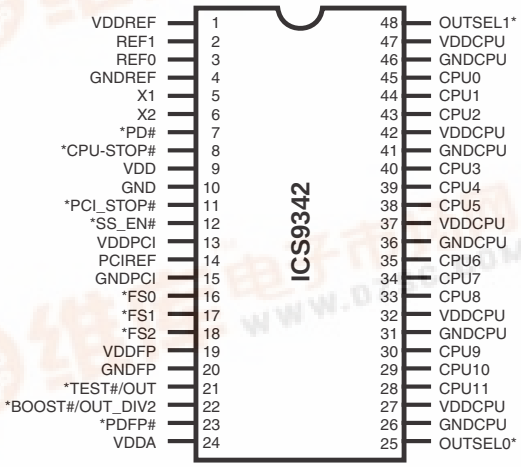
Recommended Application:
Power PC System Clock

Output Features:
- 12- CPUs @ 3.3V, up to 146MHz
- 1- PCIREF @ 3.3V, up to 73MHz
- 1 - OUT 3.3V, 64MHz
- 1 - OUT/2 3.3V, OUT/2MHz
- 2 - REF @ 3.3V, 14.318MHz

Features:
- Up to 146MHz frequency support
- Support power management: CPU, PCI stop and power down mode.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%).
- Uses external 14.318MHz crystal
- FS pins for frequency select
- Support for industrial temperature range (-40C° to 85C°)

Key Specifications:
- CPU Output Skew: <200ps
- CPU - PCI Output Skew: <500ps
- CPU Output Jitter: <150ps
- PCI Output Jitter: <500ps

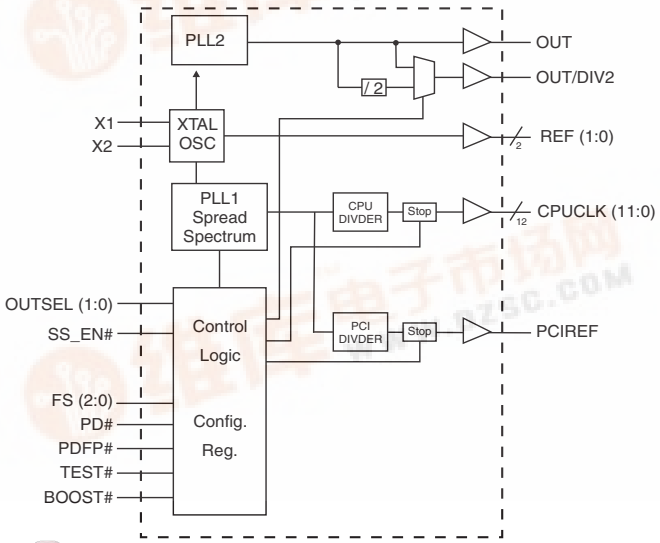
Pin Configuration



48-Pin 300mil SSOP

* Internal pull-up resistor of 120K to VDD on indicated inputs.

Block Diagram



Functionality

TEST	FS2	FS1	FS0	CPU MHz	PCI MHz	REF MHz
1	1	1	1	133.33	33.33	14.318
1	1	1	0	100.00	33.33	14.318
1	1	0	1	83.33	33.33	14.318
1	1	0	0	66.66	33.33	14.318
1	0	1	1	133.33	66.66	14.318
1	0	1	0	100.00	66.66	14.318
1	0	0	1	83.33	66.66	14.318
1	0	0	0	66.66	66.66	14.318

ICS9342

General Description

The **ICS9342** generates all clocks required for high speed PowerPC RISC microprocessor systems. With a zero delay buffer chip such as the ICS9112-17 multiple PCI clock outputs can be generated in phase with PCIREF.

Spread Spectrum may be enabled by driving the SS_EN# pin low. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9342** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref(1:0), XTAL power supply, nominal 3.3V
2,3	REF[1:0]	OUT	14.318 MHz reference clocks
4	GNDREF	PWR	Ground pin for the REF outputs
5	X1	IN	Crystal input,nominally 14.318MHz.
6	X2	OUT	Crystal output, nominally 14.318MHz.
7	PD#	IN	Powers down chip, active low.
8	CPU_STOP#	IN	Stops all CPUCLKs [11:0] at logic 0 level, when input low
9	VDD	PWR	3.3V power for the digital core.
10	GND	PWR	Ground pin for the digital core.
11	PCI_STOP#	IN	Drives PCIREF to logic 0 level, when input low
12	SS_EN#	IN	Spread spectrum is turned on by driving this input low and turned off by driving it high.
13	VDDPCI	PWR	Power supply for PCIREF, nominal 3.3V.
14	PCIREF	OUT	Reference clock for PCI Zero Delay Buffer.
15	GNDPCI	PWR	Ground pin for PCIREF.
18, 17, 16	FS (2:0)	IN	Frequency select pins.
19	VDDFP	PWR	3.3V power for the Fixed PLL core.
20	GNDFP	PER	Ground pin for the Fixed PLL core.
21	OUT	OUT	3.3V OUT reference clock.
	TEST#	IN	Logic input to select over clocking or under clocking frequencies. (latched input)
22	OUT_DIV2	OUT	3.3V 1/2 frequency OUT reference clock.
	BOOST#	IN	Logic input to select normal or test mode frequencies. (latched input)
23	PDFP#	IN	Powers down Fixed PLL. When driven to low, OUT and OUT_DIV2 clocks will be stopped
24	VDDA	PWR	3.3V power for the PLL core
48, 25	OUTSEL(1:0)	IN	Frequency select pins for OUT and OUT_DIV2 clocks.
26, 31, 36, 41, 46	GNDCPU	PWR	Ground pin for CPU clocks.
27, 32, 37, 42, 47	VDDCPU	PWR	3.3V power supply for CPU clocks.

Frequency Selection

BOOST#	TEST#	FS2	FS1	FS0	CPU MHz	PCI MHz	REF MHz	SS TYPE/VALUE If SS enabled
X	1	1	1	1	133.33	33.33	14.318	0 to -0.5% Down Spread
X	1	1	1	0	100.00	33.33	14.318	0 to -0.5% Down Spread
X	1	1	0	1	83.33	33.33	14.318	0 to -0.5% Down Spread
X	1	1	0	0	66.66	33.33	14.318	0 to -0.5% Down Spread
X	1	0	1	1	133.33	66.66	14.318	0 to -0.5% Down Spread
X	1	0	1	0	100.00	66.66	14.318	0 to -0.5% Down Spread
X	1	0	0	1	83.33	66.66	14.318	0 to -.5% Down Spread
X	1	0	0	0	66.66	66.66	14.318	0 to -0.5% Down Spread
1	0	1	1	1	146.62	36.6	14.318	+ 0.25% Center Spread
1	0	1	1	0	109.99	36.6	14.318	+ 0.25% Center Spread
1	0	1	0	1	91.58	36.6	14.318	+ 0.25% Center Spread
1	0	1	0	0	73.31	36.6	14.318	+ 0.25% Center Spread
1	0	0	1	1	146.62	73.3	14.318	+ 0.25% Center Spread
1	0	0	1	0	109.99	73.3	14.318	+ 0.25% Center Spread
1	0	0	0	1	91.58	73.3	14.318	+ 0.25% Center Spread
1	0	0	0	0	73.31	73.3	14.318	+ 0.25% Center Spread
0	0	1	1	1	119.98	30.00	14.318	+ 0.25% Center Spread
0	0	1	1	0	90.00	30.00	14.318	+ 0.25% Center Spread
0	0	1	0	1	74.93	30.00	14.318	+ 0.25% Center Spread
0	0	1	0	0	Test Mode, CPU=Ref/4, PCI=Ref/8			
0	0	0	1	1	119.98	60.00	14.318	+ 0.25% Center Spread
0	0	0	1	0	90.00	60.00	14.318	+ 0.25% Center Spread
0	0	0	0	1	74.93	60.00	14.318	+ 0.25% Center Spread
0	0	0	0	0	Tristate, all outputs			

OUT_SEL1	OUT_SEL0	OUT (MHz)	OUT_DIV2 (MHz)	REF (MHz)
1	1	48	24	14.318
1	0	40	20	14.318
0	1	64	32	14.318
0	0	48	48#	14.318

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... -40°C to +85°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	Select @ 66MHz; Max discrete cap loads		134	175	mA
	$I_{DD3.3OP83}$	Select @ 83MHz; Max discrete cap loads		165	200	
	$I_{DD3.3OP100}$	Select @ 100MHz; Max discrete cap loads		198	225	
	$I_{DD3.3OP133}$	Select @ 133MHz; Max discrete cap loads		254	300	
Power Down Supply Current	$I_{DD3.3PD}$	PD# = 0		313	400	µA
Input frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	13.5	18	22.5	pF
Transition Time[1]	T_{Trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_S	From 1st crossing to 1% target Freq.		1		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$t_{CPU-PCI}$	V_T = 1.5 V		190	500	ps

Electrical Characteristics - CPU

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	20	45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	29	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -8.0 mA	2	2.4		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.32	0.4	V
Output High Current	I_{OH2B}	V_{OH} =1.7 V		-37	-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.13	2	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.27	2	ns
Duty Cycle	d_{t2B}[1]	VT = 1.5 V; Cpu@ 66M, 83M, 100M	45	52	56	%
		VT = 1.5 V; Cpu@133M & 146.6M	51	56	60	
Skew	t_{sk2B}[1]	VT = 1.5 V		187	200	ps
Jitter, Cycle-to-cycle	$tj_{cyc-cyc2B}$[1]	VT = 1.5 V; Normal		95	150	ps
		VT = 1.5 V; Spread, CPU = 91.58MHz		143	200	
		VT = 1.5 V; Spread, CPU remaining freq.		143	175	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%; C_L =30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	21	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	21.2	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4			
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-60	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	47		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.9	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		170	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, OUT, OUT/2

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance		R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20	34	60	Ω
		R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20	31	60	Ω
Output High Voltage		V_{OH5}	I_{OH} = -12 mA	2.4	2.9		V
Output Low Voltage		V_{OL5}	I_{OL} = 10 mA		0.33	0.4	V
Output High Current		I_{OH5}	V_{OH} = 2.0 V		-30	-20	mA
Output Low Current		I_{OL5}	V_{OL} = 0.8 V	16	23		mA
REF	Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; OUT	1.5	1.8	4	ns
	Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; OUT	1.5	2	4	ns
	Duty Cycle[1]	d_{t5}	V_T = 1.5 V; OUT	45	52	55	%
OUT	Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; OUT/2	1.5	2.2	4	ns
	Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; OUT/2	1.5	2.1	4	ns
	Duty Cycle[1]	d_{t5}	V_T = 1.5 V; OUT/2	45	50	55	%
OUT/2	Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; REF	1.5	2.7	4	ns
	Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; REF	1.5	2.8	4	ns
	Duty Cycle[1]	d_{t5}	V_T = 1.5 V; REF	45	50	55	%
Jitter, Cycle-to-cycle1		$t_{jcyc-cyc5}$	V_T = 1.5 V; OUT, OUT/2		280	500	ps
Jitter, Cycle-to-cycle[1]		$t_{jcyc-cyc5}$	V_T = 1.5 V; REF		450	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9342 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

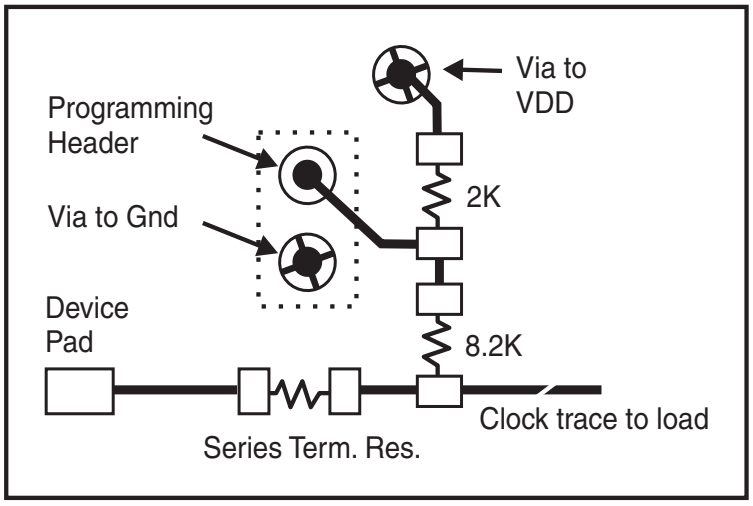


Fig. 1

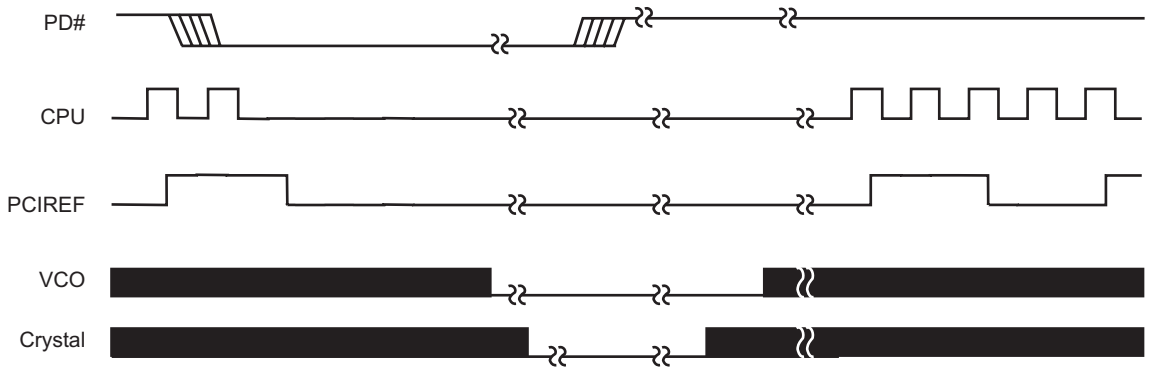
Power Management

PD#	PDFP#	OUT1, OUT_DIV2	CPU, PCI, REF
1	1	RUNNING	RUNNING
1	0	STOPPED	RUNNING
0	1	STOPPED	STOPPED
0	0	STOPPED	STOPPED

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

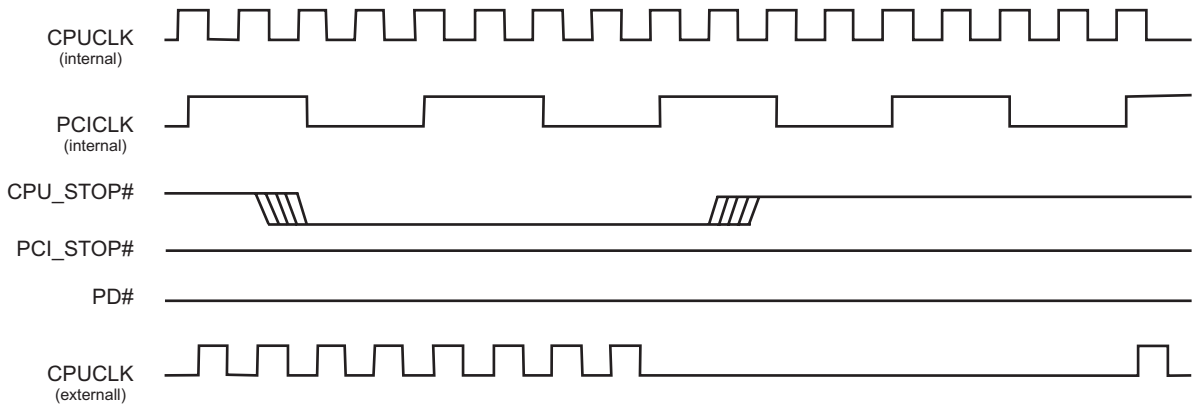
Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. The REF and OUT clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPU (defined as inside the ICS9342 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

CPU_STOP# Timing Diagram

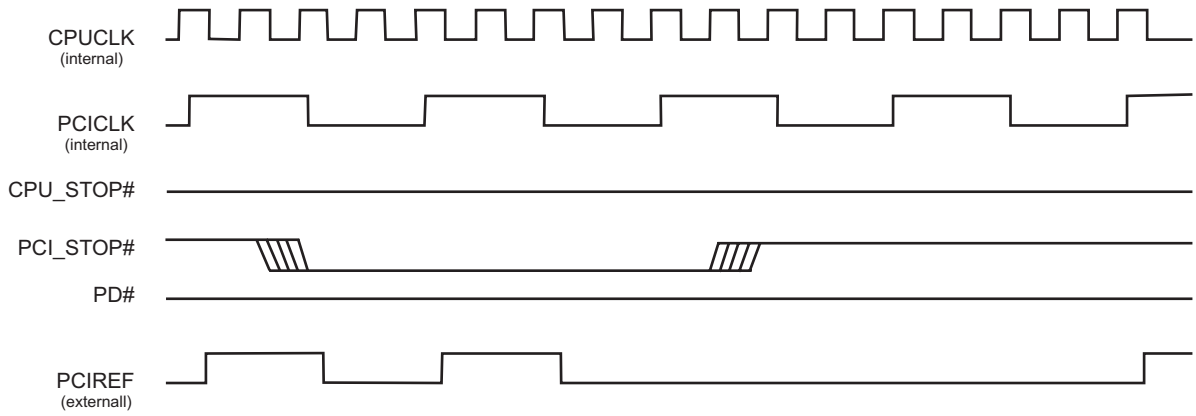
CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock (and hence CPU clock) and must be internally synchronized to the external output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse.



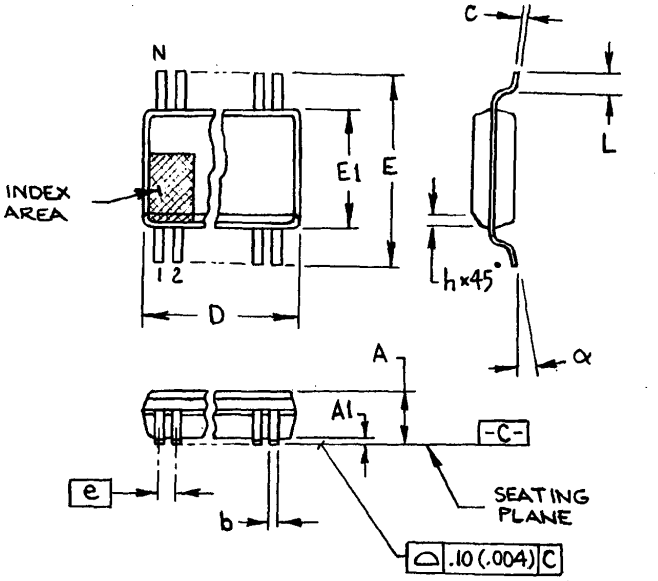
Notes:
1. All timing is referenced to the internal CPUCLK.
2. The internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. PD# and PCI_STOP# are shown in a high state.

PCI_STOP# Timing Diagram

PCI_STOP# is an input to the clock synthesizer. It is used to turn off the PCIREF clock for low power operation. PCIREF clock is required to be stopped in a low state and started such that a full high pulse width is guaranteed.



Notes:
1. All timing is referenced to CPUCLK.
2. Internal means inside the chip.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high state.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

Ordering Information

ICS9342yF-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device