YM3436D

DIR2

Digital audio Interface Receiver

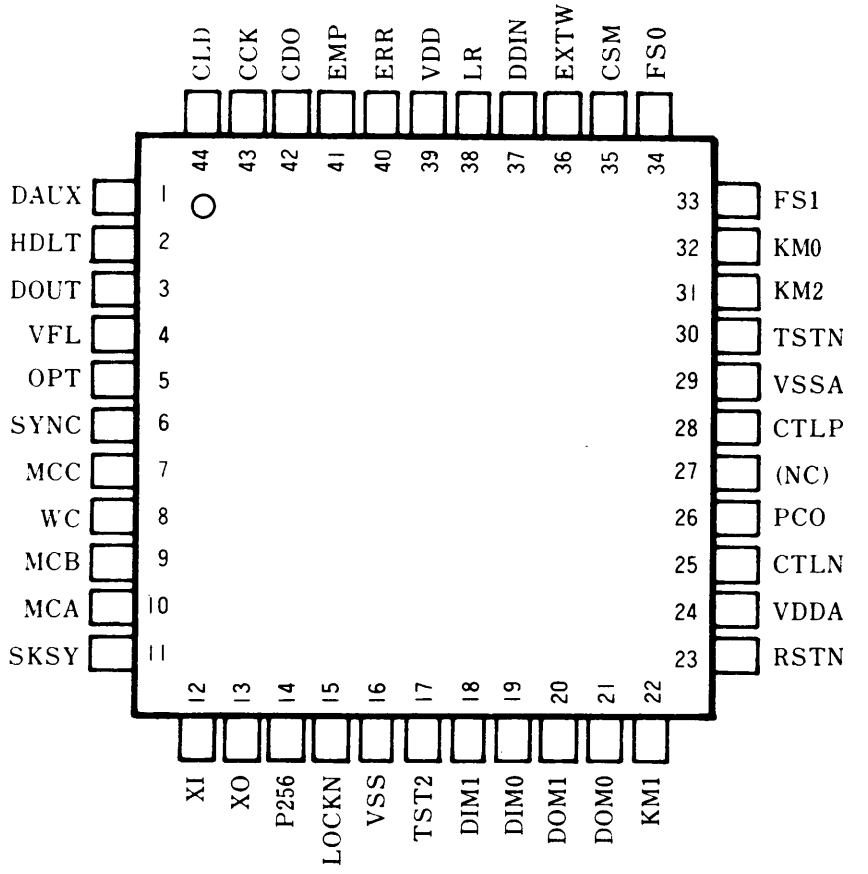
■ OUTLINE

The YM3436D(DIR2) receives and demodulates the digital audio interface format signals, conforming with the EIAJ CP-340 or AES/EBU. Comparing to the YM3623B(DIR), external synchronization and error processing functions are further improved and it is made applicable more widely by using the channel status and user data outputs.

■ FEATURES

- Capable to accept the A/D input and asynchronous input as well as the digital audio interface signal input.
- As a phase comparator and VCO are built in, a PLL circuit synchronized with the external input can be formed easily (fs=32kHz～48kHz)
- Capable to demodulate the digital audio interface signal and output 24-bit 2-channel audio data and control data.
- As a clock master, it supplies various kinds of clock signals to the other LSIs.
- The built-in asynchronous buffer enables the output phase to be retained even on clock switching. Also capable of easy interface between the equipments where full synchronization is impossible such as when several digital audio interface signals are received simultaneously.
- Detects transmission errors and reception errors and executes error processing of data hold and muting.
- Executes decoding and output of the validity flag, channel status, user data as control data. Especially, the channel status conforms with both Consumer use and Professional use formats. Also, information can be read out microprocessor interface.
- 5V power supply, Si-gate CMOS, 44-pin QFP.

■ PIN CONFIGURATION

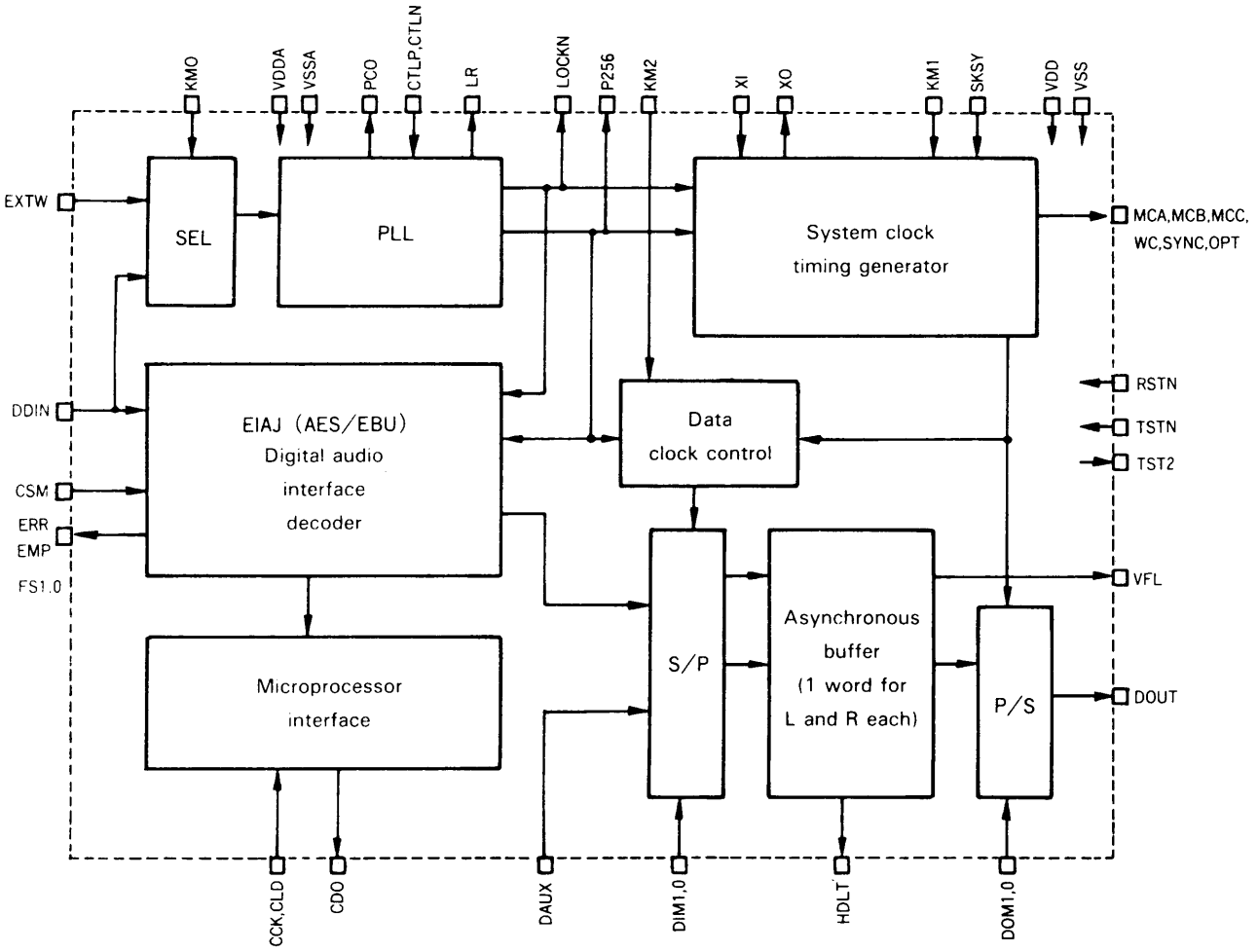


<44QFP TOP VIEW>

■ PIN DESCRIPTIONS

No.	Name	I/O	Description
1	DAUX	I	Audio data auxiliary input
2	HDLT	O	Asynchronous buffer operation flag output
3	DOUT	O	Audio data output
4	VFL	O	Validity flag output
5	OPT	O	Synchronous signal output (fs) for DAC
6	SYNC	O	Synchronous signal output (fs) for DSP
7	MCC	O	Bit clock output (64fs)
8	WC	O	Word clock output (fs)
9	MCB	O	Bit clock output (128fs)
10	MCA	O	Bit clock output (256fs)
11	SKSY	I	Clock synchronous control input
12	XI	I	Crystal oscillator connection, or external clock input (256fs)
13	XO	O	Crystal oscillator connection
14	P256	O	VCO clock output (256fs when locked)
15	LOCKN	O	PLL lock flag output ('L'; when locked, 'H'; when unlocked)
16	VSS	—	Ground (for logic block)
17	TST2	O	LSI test terminal (usually disconnected)
18	DIM1	I	Data input mode select 1
19	DIM0	I	Data input mode select 0
20	DOM1	I	Data output mode select 1
21	DOM0	I	Data output mode select 0
22	KM1	I	Clock mode select 1 ('H'; PLL auto switching, 'L'; XI fixed)
23	RSTN	I	System reset input ('L' active)
24	VDDA	—	+5V power supply (for VCO block connected with VDD externally)
25	CTLN	I	VCO control input
26	PCO	O	PLL phase comparator output
27	(NC)		(Disconnected externally)
28	CTLP	I	VCO adjustment input (usually connected with VSSA)
29	VSSA	—	Ground (for VCO block, connected with VSS externally)
30	TSTN	I	LSI test terminal (usually disconnected)
31	KM2	I	Clock mode select 2 ('H'; PLL synchronized, 'L'; XI synchronized)
32	KM0	I	Clock mode select 0 ('H'; EXTW input, 'L'; DDIN input)
33	FS1	O	Sampling frequency code output 1/channel status output
34	FS0	O	Sampling frequency code output 0/user data output
35	CSM	I	Channel status, user data output select
36	EXTW	I	Audio data auxiliary input word clock
37	DDIN	I	EIAJ(AES/EBU) digital audio interface signal input
38	LR	O	PLL word clock output (fs when locked)
39	VDD	—	+5V power supply (for logic block)
40	ERR	O	Data error flag output
41	EMP	O	Emphasis control code output/block start synchronous signal output
42	CDO	O	Microprocessor interface data output
43	CCK	I	Microprocessor interface clock input
44	CLD	I	Microprocessor interface load input

■ BLOCK DIAGRAM



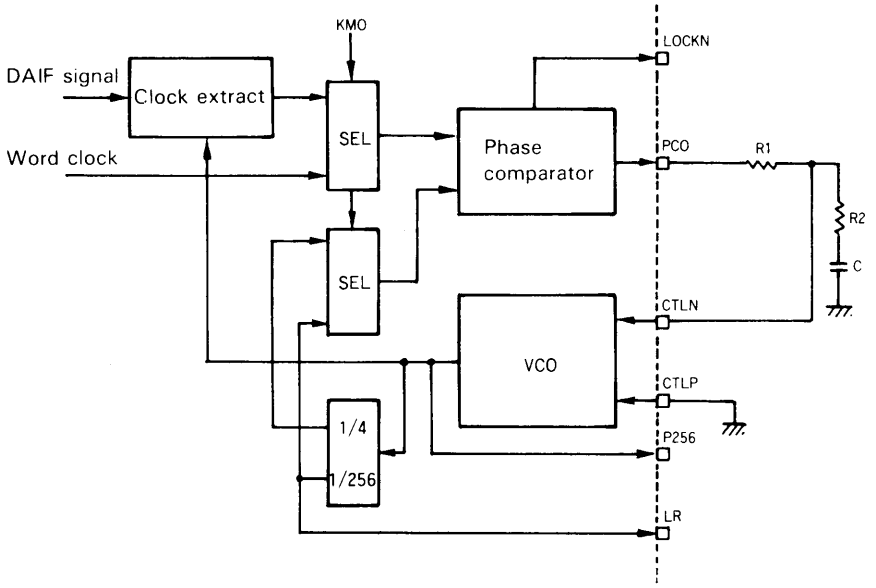
■ FUNCTION DESCRIPTION

1. Data input DDIN, DAUX, DIM1, DIM0

The digital audio interface signal (hereinafter referred to as "DAIF signal") of EIAJ(AES/EBU) format is inputted into the DDIN terminal. In addition to that, this LSI has an auxiliary input terminal DAUX for the audio data to which signals from the A/D converter and DSP can be inputted. The input format for the DAUX is selected by DIM0 and DIM1 terminals.

2. PLL block PCO, CTLN, CTLP, P256, LR, LOCKN, KM0, KM2, EXTW

DIR2 has a phase comparator and VCO to regenerate the clock signals synchronized with the input rate. The output of the phase comparator is output from the PCO terminal. With an appropriate time constant attached externally, and by applying input to the CTLN terminal, the PLL clock regeneration circuit is formed. The CTLP terminal is for VCO adjustment. Usually it should be grounded. The VCO oscillation frequency is 256fs and output from the P256 terminal. The clock signal obtained by dividing the VCO clock by 256 is output from the LR terminal. Whether the PLL is locked or not is checked inside and the LOCKN terminal becomes 'L' when it is locked.



Normally, the PLL circuit synchronizes with the DAIF signal which is inputted to the DDIN terminal but it can also synchronize with the duty 50% word clock(fs) which is inputted to the EXTW terminal. Which signal to be synchronized with is selected by the KM0 terminal.

However, when accepting the data from the LSI which operates according to the clock singnals of DIR2, such as A/D converter, interfacing without using the PLL circuit can be also selected by the KM2 terminal.

KM0; Synchronized signal select 'L'=DDIN input 'H'=EXTW input

KM2; DAUX synchronization select 'L'=XI clock synchronization 'H'=PLL clock synchronization (invalid at DIM1, 0='H', 'H')

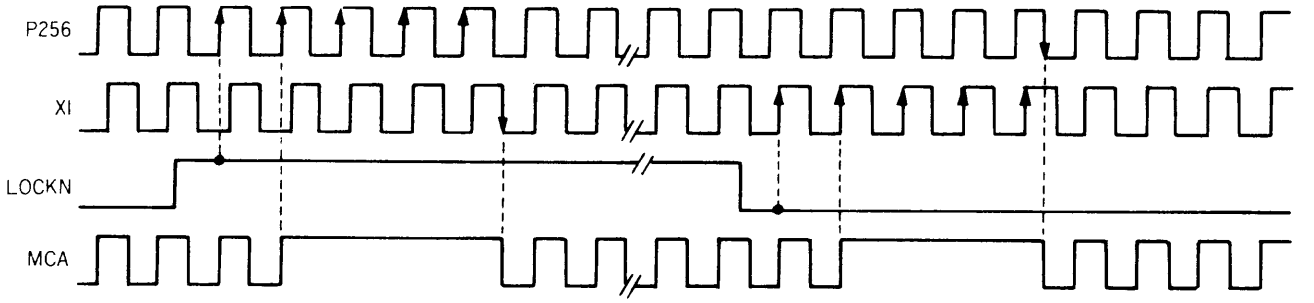
3. System clocks output XI, XO, MCA, MCB, MCC, WC, SYNC, OPT, KM1, SKSY

A 256fs crystal oscillation circuit is formed at XI and XO terminals to generate the XI clock. This is used as the system clock for defaulting when the internal reset cycle or signal to be synchronized with are not inputted. The XI clock signal should be supplied constantly. As a clock master, this LSI outputs various system clock signals to the other LSIs. The clock source of the system clock is selected by the KM1 terminal.

KM1; Clock source select
'L'=XI clock fixed
'H'=VCO clock automatic switching
(automatically switched to the XI clock when the PLL is not locked)

The MCA outputs 256fs clock and then MCB, MCC, WC, SYNC and OPT are outut by dividing the MCA.

When in the VCO clock automatic switching mode, continuity of the system clock is maintained except only 3-cycle stop of the MCA clock when the VI and VCO clock are switched.



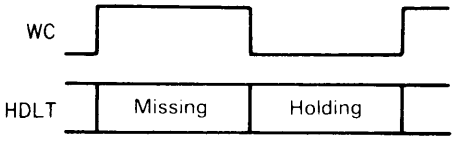
In this case, however, the phase relation between the word clock which was synchronized newly and the former word clock becomes undefined. For this reason, the data reception block and the data output block are connected by asynchronous buffer of L and R one word each. Thus even when there is a phase difference between the input and output, if their sampling frequencies are the same, data can be output continuously without missing any data. Also, the system clock divider can be reset by the SKSY terminal setting, if necessary.

SKSY; System clock reset control select
When KM1='L'; The system clock divider is reset at the fall timing of the SKSY.
(When the data must be output according to the system timing)
When KM1='H'; When the SKSY is set to 'L', the system clock divider is reset by the word clock signal which is synchronized with the PLL.
(When SKSY is 'H', the continuity of the system clock is maintained.)

4. Data output DOUT, DOM0, DOM1, VFL, HDLT

After undergoing buffering at the asynchronous buffer, the audio data is output from the DOUT terminal. The data format is selected by DOM0 and DOM1 terminals. The output timing is synchronized with the MCB. When the DAIF signal is received, the validity flag is output from the VFL terminal for each sub-frame, otherwise, the VFL is 'L'.

When the sampling frequency differs between the PLL and the system, holding or missing of the data occurs and such asynchronous buffer condition is output from the HDLT terminal.



With HDLT='H',
when WC='L': Data is held.
when WC='H': Missing of data occurs.

5. Error processing ERR

Any error that has occurred in the transmission circuit and reception stage is detected by the lock condition of the PLL and pality check. When an error has occurred, the audio data is held for L and R respectively up to 1 sample. If it is more than that, L and R are muted simultaneously. Muting is not cancelled till 4096 samples are processed without any error for both L and R channels. The ERR terminal output becomes 'H' when the PLL is unlocked and a parily error has occurred. It is possible to monitor the DAIF signal state even when an auxiliary input of the A/D or such is selected.

6. Channel status and user data output CSM, EMP, FS0, FS1

The channel status and user data included in the DAIF signal are decoded and output from each of the EMP, FS0 and FS1 terminals. It is also readable through the microprocessor interface. There are two output forms and their selection is done by the CSM terminal.

- CSM='L'; Latch mode

  The emphasis control code and sampling frequency code are latched and output for each block.

  EMP; Emphasis control code output

  FS0, FS1; Sampling frequency code output

FS1	FS0	Sampling frequency	
		For Consumer use	For Professional use
L	L	44.1KHz	—
L	H	48 KHz	48 KHz
H	L	—	44.1KHz
H	H	32 KHz	32 KHz

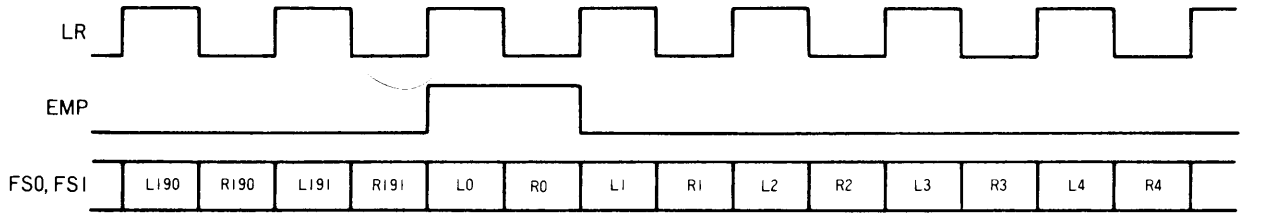
- CSM='H'; Synchronous output mode

  All bits of the channel status and user data are output continuously for each sub-frame.

  EMP; Block start synchronous signal

  FS1 ; Channel status continuous output

  FS0 ; User data continuous output

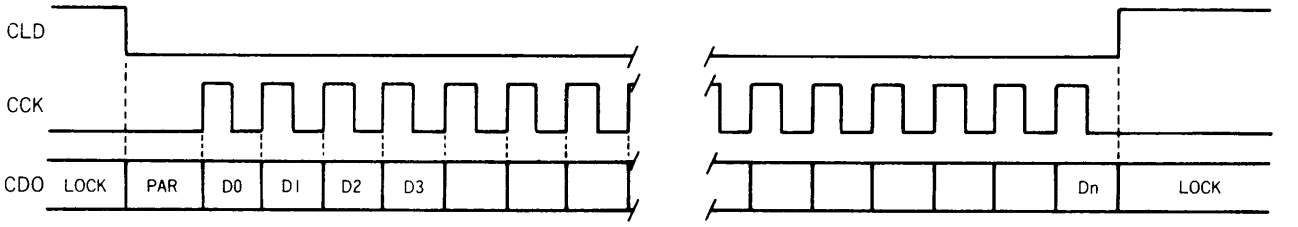


7. Microprocessor interface CLD, CCK, CDO

Following information items are output from the microprocessor interface.

- Lock condition of PLL
- Parity check condition
- Head end 32 bits of channel status
- 32 bits local sample address of channel status (for professional use format only)
- Head end 32 bits of user data

(There is no specification to delimit the user data in the same way as the channel status data, the DIR2 delimits the user bits in blocks just as for the channel status bits and the first 32 bits of the user bits are output. This is not a general format; however, this is very useful when used with YM3437(DIT2), forming is done that way and the head end 32 bits are output.)



LOCK: PLL lock condition ('0'=Locked, '1'=Unlocked)
PAR : Parity error condition ('0'=No error, '1'=Parity error occurred)

D0 ~ Dn: Channel status and user data information

<Data Assignment>

	D0	D1 ~ D31	D32 ~ D63	D64 ~ D67	D68	D69 ~ D100
For Consumer use	0	Channel status bits 1 to 31	User data bits 0 to 31			
For Professional use	1	Channel status bits 1 to 31	Local sample address code	Reliability flag lower 4 bits	CRC bit	User data bits 0 to 31

Note) The CRC bit becomes '1' only when the CRC check esulted in an error.

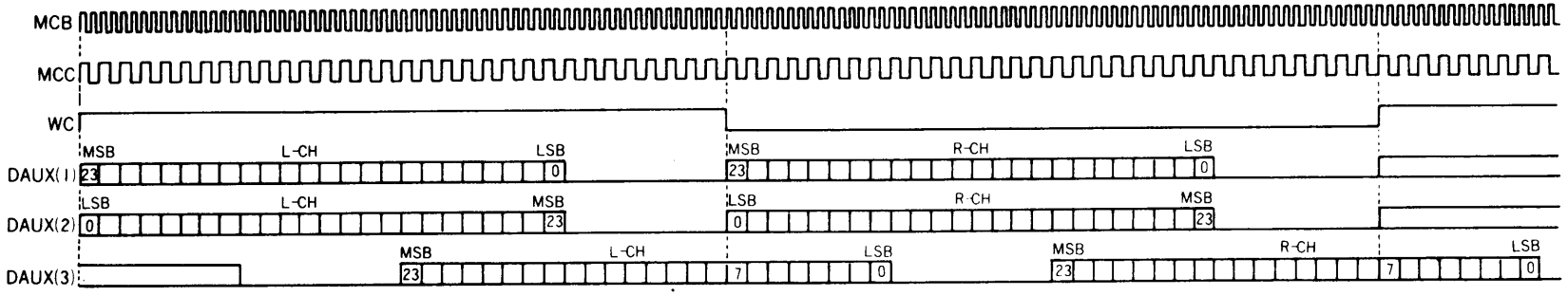
8. Initial clear/test RSTN, TSTN, TST2

For the power on resetting, it is necessary that the RSTN terminal be 'L' for the XI 256 clock cycles. TSTN and TST2 terminals are for the LSI test and usually should be discornected.

(1) Auxiliary input format

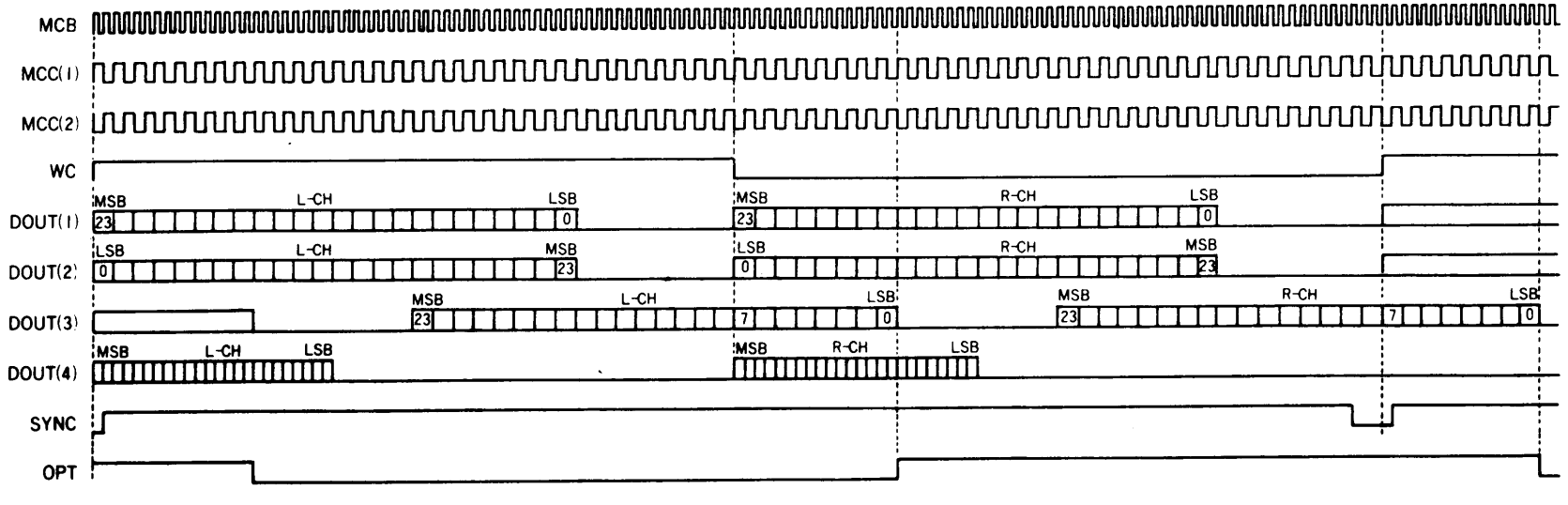
DIM 1	DIM 0	Format
L	L	DAUX(1)
L	H	DAUX(2)
H	L	DAUX(3)
H	H	DDIN input

(The polarity of MCC depends on the output format.)



(2) Data output format

DOM 1	DOM 0	Format
L	L	MCC(1), DOUT(1)
L	H	MCC(1), DOUT(2)
H	L	MCC(2), DOUT(3)
H	H	MCC(1), DOUT(4)



■ ELECTRICAL CHARACTERISTICS

• ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	V_{SS} − 0.3 ~ V_{DD} + 0.5	V
Operation temperature	Top	0 ~ +70	°C
Storage temperature	Tstg	−50 ~ +125	°C

• RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operation temperature	Top	0	25	70	°C

• DC CHARACTERISTICS (Conditions; Ta=0 ~ 70°C, V_{DD}=5.0 ± 0.25V)

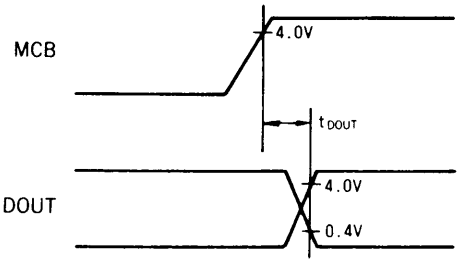
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{DD}	V_{DD}=5.0V		22	30	mA
Input voltage H level(1)	V_{IH1}	(Note 1)	2.0			V
Input voltage L level(1)	V_{IL1}	(Note 1)			0.8	V
Input voltage H level(2)	V_{IH2}	(Note 2)	3.6			V
Input voltage L level(2)	V_{IL2}	(Note 2)			1.0	V
Input leakage current	I_{LK}		−10		10	μA
Output voltage H level	V_{OH}	I_{OH} = −50μA	4.0			V
Output voltage L level	V_{OL}	I_{OL}=2.0mA			0.4	V
Input capacitance	C_I				10	pF
Output capacitance	C_O				10	pF

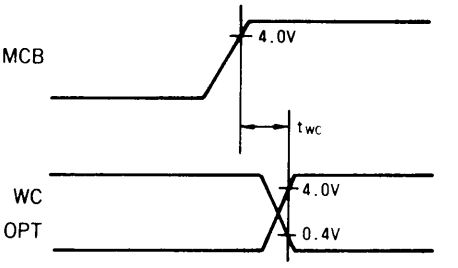
Note 1; Applicable to input terminals except XI

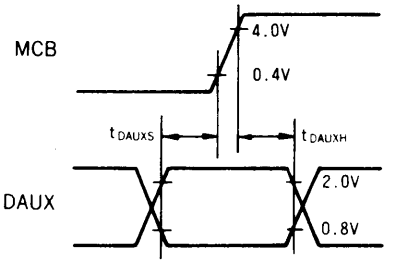
Note 2; Applicable to XI terminal

• AC CHARACTERISTICS (Conditions; Ta=0 ~ 70°C, V_{DD}=5.0 ± 0.25V)

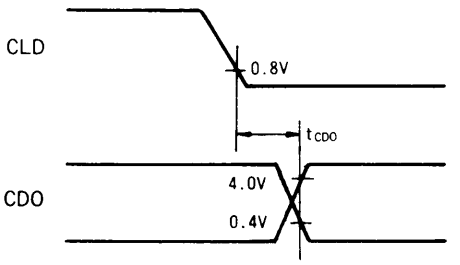
Parameter	Symbol	Min.	Typ.	Max.	Unit
XI frequency	f_{XI}	7.37		13.5	MHz
Duty		40	50	60	%
XI Rise time				50	ns
Fall time				50	ns
DOUT output delay	t_{DOUT}			40	ns
WC, OPT output delay	t_{WC}			35	ns
DAUX setup time	t_{AUXS}	70			ns
DAUX hold time	t_{AUXH}			70	ns
CDO delay	t_{CDO}			130	ns
RSTN pulse width		256/f_{XI}			
CCK pulse width		16/f_{XI}			

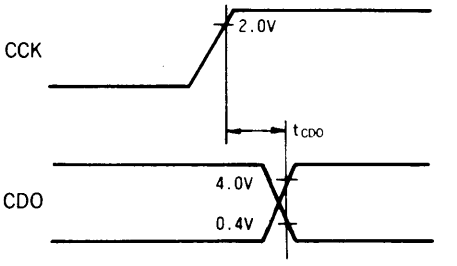

MCB
4.0V
t_{DOUT}
DOUT
4.0V
0.4V


MCB
4.0V
t_{WC}
WC
OPT
4.0V
0.4V

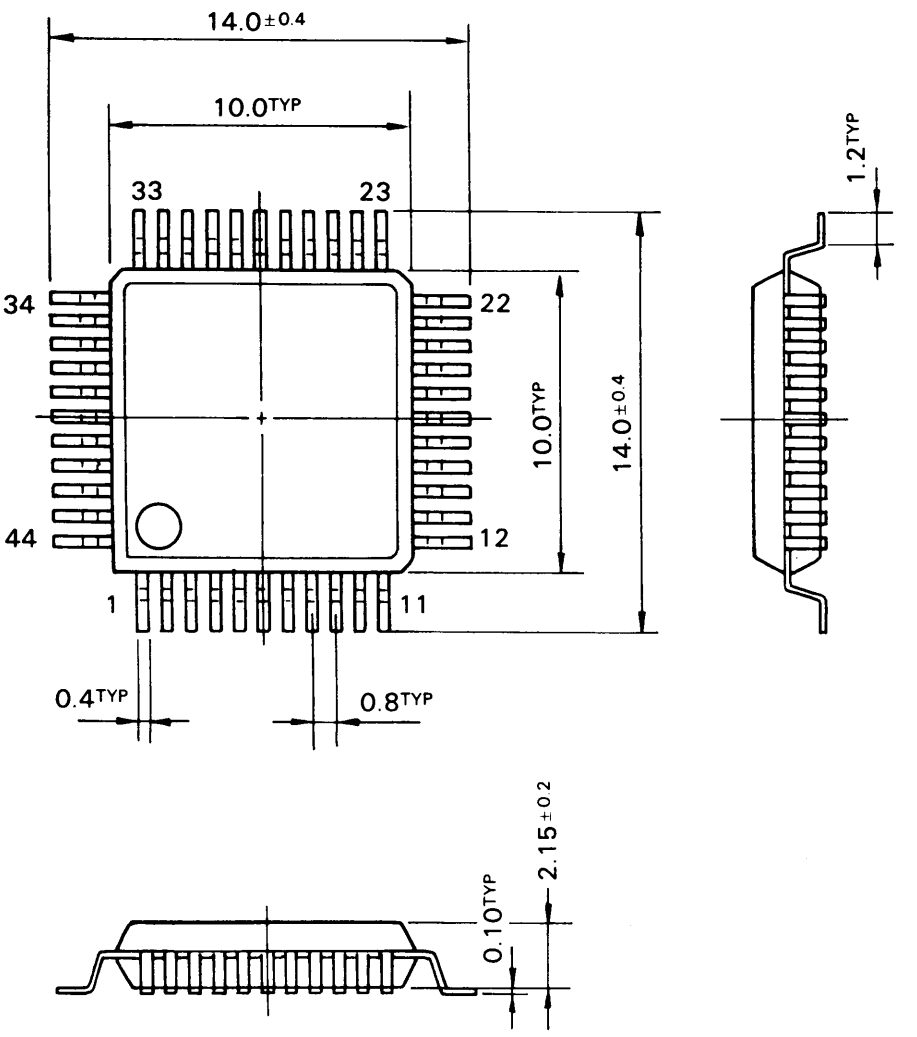

MCB
4.0V
0.4V
t_{DAUXS}
t_{DAUXH}
DAUX
2.0V
0.8V

(when KM2 is 'L')


CLD
0.8V
t_{CDO}
CDO
4.0V
0.4V


CCK
2.0V
t_{CDO}
CDO
4.0V
0.4V

■ EXTERNAL DIMENSIONS



DIMENSION IN mm

Note : The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

Note) Specifications of this product are subject to change for improvement without prior notice.

MEMO

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