YSS248

AC3PL

Dolby AC-3 & Pro Logic decoder

■ OUTLINE

YSS248(AC3PL) has two kinds of decoding functions: The first is Dolby AC-3 5.1 channel full decoding which decodes the signal that has been coded as prescribed in IEC958 and the second is Dolby Pro Logic decoding. This device has built-in memory for center and surround channels signal delay, no external memory is required. A one-chip solution achieves simple design with low cost for your application.

■ FEATURES

- AC-3 5.1 channel full decode.
- 24 bit DSP. (Group-A AC-3 decoder)
- Possible to decode multi-language encoded data.
  (possible to decode based on data-stream-number)
- AC-3 karaoke mode.
- Original compression mode as well as four compression modes recommended by Dolby.
- AC-3 decoding latency is fixed to two audio blocks (512 samples).
- Included de-emphasis filter.
- Pro Logic decoding for AC-3 2 channels decoded signal as well as ordinary PCM.
- Reads AC-3 bitstream information through the microprocessor interface.
- Provides total sixteen I/O ports.
- Possible to connect almost all SPDIF receivers, A/D and D/A converters, by setting I/O data interface format.
- No external memory is required (center and surround channels signal delay memory are included).
- Has a built-in PLL oscillation circuit to generate its own operating clock.
- Internal operating clock is 20 MHz.
- 5v single power supply, Si-gate CMOS process.
- 100QFP

Note)
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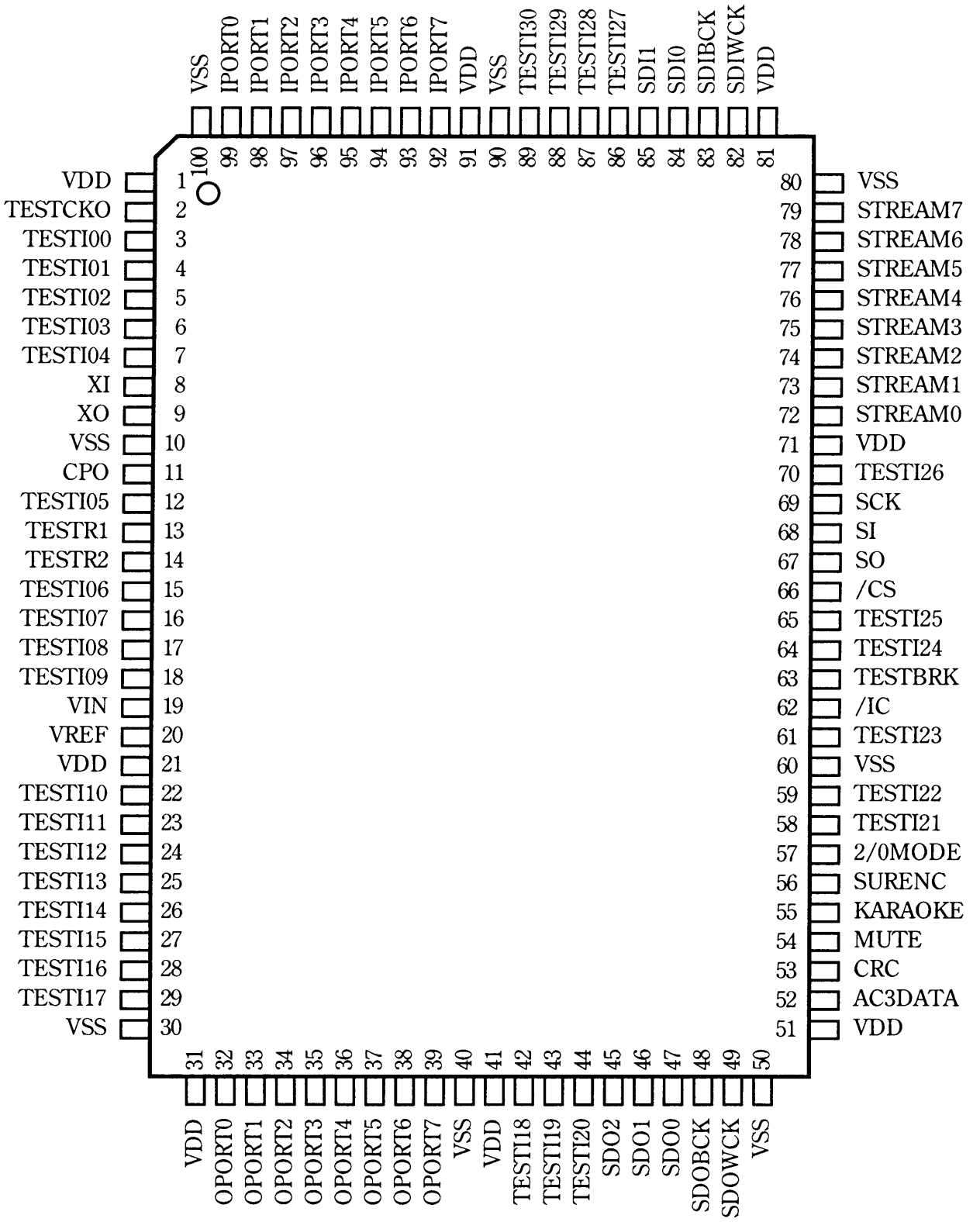
Use of this LSI must be licensed by Dolby Laboratories Licensing Corporation.

■ PIN CONFIGURATION



< 100pin QFP top view >

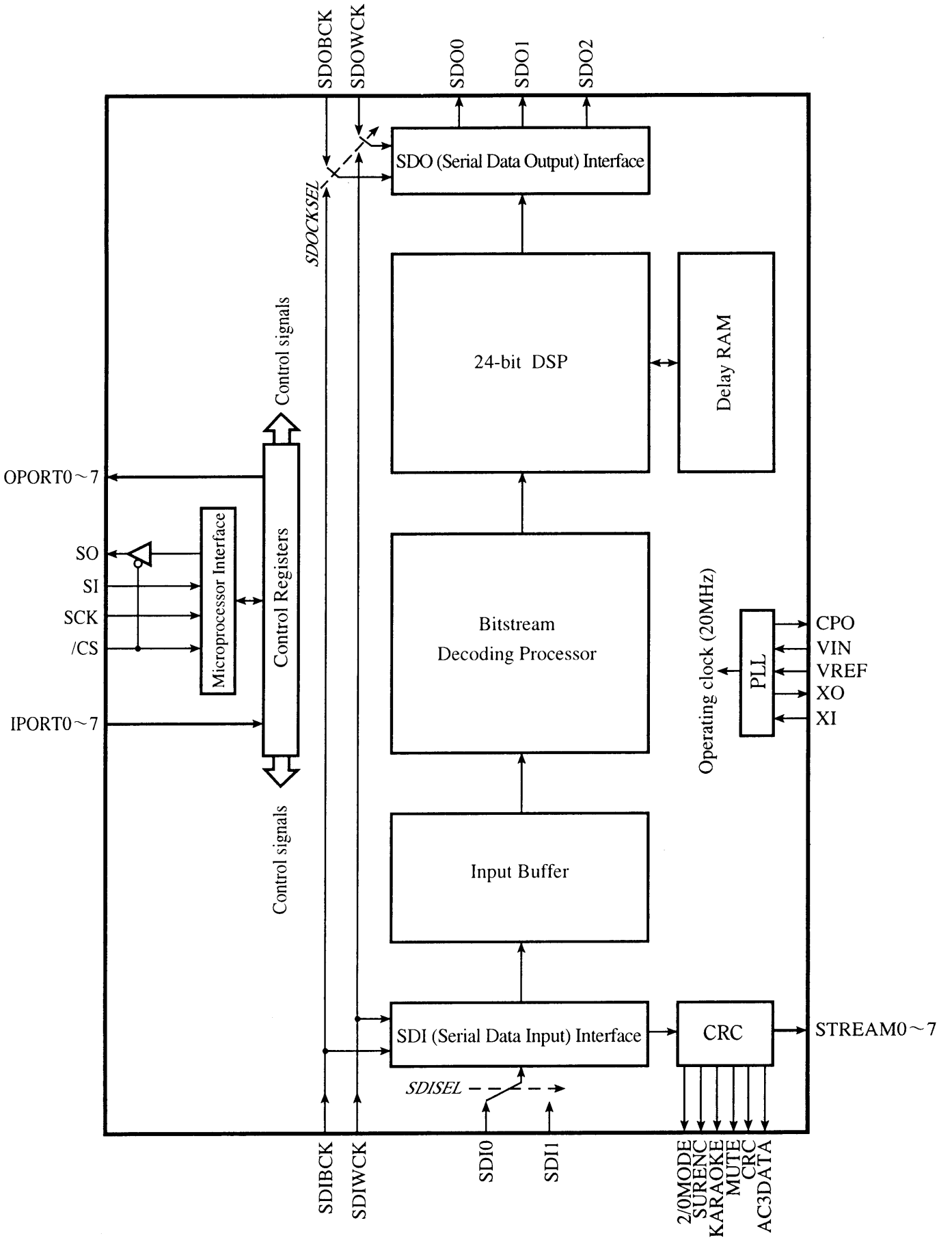
■ PIN FUNCTION

No.	NAME	I/O	FUNCTION
1	VDD	-	+5V power supply
2	TESTCKO	O	Test terminal (to be open in normal use)
3	TESTI00	I+	Test terminal (to be open in normal use)
4	TESTI01	I+	Test terminal (to be open in normal use)
5	TESTI02	I+	Test terminal (to be open in normal use)
6	TESTI03	I+	Test terminal (to be open in normal use)
7	TESTI04	I+	Test terminal (to be open in normal use)
8	XI	I	Crystal oscillator connection or input external clock (5.0MHz~40.0MHz)
9	XO	O	Crystal oscillator connection
10	VSS	-	Ground
11	CPO	AO	Output terminal for PLL, to be connected to VIN terminal through the external analog filter circuit
12	TESTI05	I+	Test terminal (to be open in normal use)
13	TESTR1	I+	Test terminal (to be open in normal use)
14	TESTR2	I+	Test terminal (to be open in normal use)
15	TESTI06	I+	Test terminal (to be open in normal use)
16	TESTI07	I+	Test terminal (to be open in normal use)
17	TESTI08	I+	Test terminal (to be open in normal use)
18	TESTI09	I+	Test terminal (to be open in normal use)
19	VIN	AI	Input terminal for PLL, to be connected to CPO terminal through the external analog filter circuit
20	VREF	AI	Input terminal for PLL, to be connected to VDD terminal through the external analog filter circuit
21	VDD	-	+5V power supply
22	TESTI10	I+	Test terminal (to be open in normal use)
23	TESTI11	I+	Test terminal (to be open in normal use)
24	TESTI12	I+	Test terminal (to be open in normal use)
25	TESTI13	I+	Test terminal (to be open in normal use)
26	TESTI14	I+	Test terminal (to be open in normal use)
27	TESTI15	I+	Test terminal (to be open in normal use)
28	TESTI16	I+	Test terminal (to be open in normal use)
29	TESTI17	I+	Test terminal (to be open in normal use)
30	VSS	-	Ground
31	VDD	-	+5V power supply
32	OPORT0	O	Output port for general purpose
33	OPORT1	O	Output port for general purpose
34	OPORT2	O	Output port for general purpose
35	OPORT3	O	Output port for general purpose
36	OPORT4	O	Output port for general purpose
37	OPORT5	O	Output port for general purpose
38	OPORT6	O	Output port for general purpose
39	OPORT7	O	Output port for general purpose
40	VSS	-	Ground
41	VDD	-	+5V power supply
42	TESTI18	I+	Test terminal (to be open in normal use)
43	TESTI19	I+	Test terminal (to be open in normal use)
44	TESTI20	I+	Test terminal (to be open in normal use)
45	SDO2	O	PCM output terminal (C, LFE)
46	SDO1	O	PCM output terminal (LS, RS)
47	SDO0	O	PCM output terminal (L, R)
48	SDOBCK	I+	Bit clock input terminal for SDO output signal
49	SDOWCK	I+	Word clock input terminal for SDO output signal
50	VSS	-	Ground
51	VDD	-	+5V power supply
52	AC3DATA	O	Detection of non-PCM data
53	CRC	O	Detection of CRC error

No.	NAME	I/O	FUNCTION
54	MUTE	O	Detection of auto mute
55	KARAOKE	O	Detection of AC-3 karaoke data
56	SURENC	O	Detection of AC-3 2/0 mode and Dolby surround encoded input
57	2/0MODE	O	Detection of AC-3 2/0 mode input
58	TESTI21	I+	Test terminal (to be open in normal use)
59	TESTI22	I+	Test terminal (to be open in normal use)
60	VSS	-	Ground
61	TESTI23	I+	Test terminal (to be open in normal use)
62	/IC	Is	Initial clear
63	TESTBRK	I+	Test terminal (to be open in normal use)
64	TESTI24	I+	Test terminal (to be open in normal use)
65	TESTI25	I+	Test terminal (to be open in normal use)
66	/CS	Is	Microprocessor interface Chip select
67	SO	Ot	Microprocessor interface Serial data output
68	SI	Is	Microprocessor interface Serial data input
69	SCK	Is	Microprocessor interface Clock input
70	TESTI26	I+	Test terminal (to be open in normal use)
71	VDD	-	+5V power supply
72	STREAM0	O	Detection of Stream 0
73	STREAM1	O	Detection of Stream 1
74	STREAM2	O	Detection of Stream 2
75	STREAM3	O	Detection of Stream 3
76	STREAM4	O	Detection of Stream 4
77	STREAM5	O	Detection of Stream 5
78	STREAM6	O	Detection of Stream 6
79	STREAM7	O	Detection of Stream 7
80	VSS	-	Ground
81	VDD	-	+5V power supply
82	SDIWCK	I	Word clock input terminal for SDI input signal
83	SDIBCK	I	Bit clock input terminal for SDI input signal
84	SDI0	I	AC-3 bitstream (or PCM) data input terminal
85	SDI1	I	AC-3 bitstream (or PCM) data input terminal
86	TESTI27	I+	Test terminal (to be open in normal use)
87	TESTI28	I+	Test terminal (to be open in normal use)
88	TESTI29	I+	Test terminal (to be open in normal use)
89	TESTI30	I+	Test terminal (to be open in normal use)
90	VSS	-	Ground
91	VDD	-	+5V power supply
92	IPORT7	I+	Input port for general purpose
93	IPORT6	I+	Input port for general purpose
94	IPORT5	I+	Input port for general purpose
95	IPORT4	I+	Input port for general purpose
96	IPORT3	I+	Input port for general purpose
97	IPORT2	I+	Input port for general purpose
98	IPORT1	I+	Input port for general purpose
99	IPORT0	I+	Input port for general purpose
100	VSS	-	Ground

注) Is : Schmidt trigger input terminal
I+ : Input terminal with a pull-up resistor
O : Digital output terminal (For V_{OH} and V_{OL}, refer to the Electrical Characteristics table.)
Ot : Tri-state digital output terminal (For V_{OH} and V_{OL}, refer to the Electrical Characteristics table.)
AI : Analog input terminal
AO : Analog output terminal

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

1. Clocks XI, XO, VIN, VREF, CPO

XI and XO terminals are used to form a crystal oscillation circuit. The oscillation frequency is 40 MHz that is divided by 2 internally to provide the operating clock of 20 MHz. To make clock signal, use XI and XO terminals to perform self oscillation or feed an external clock signal to the XI terminal.

This LSI operates in a PLL oscillation mode as well. When selecting the PLL oscillation mode, connect an external analog filter between VIN, VREF, and CPO terminals feed an external clock signal whose frequency is lower than 20 MHz to the XI terminal, and utilize multiplier.

2. Data Interface SDIBCK, SDIWCK, SDI0, SDI1, SDOBCK, SDOWCK, SDO0~2

AC-3 bitstream data or PCM data should be fed from SDI0 or SDI1 terminal. This signal needs to be synchronized with SDIBCK(bit clock) and SDIWCK(work clock) signals.

PCM data are outputted from the terminals SDO0 ~ SDO2.

Synchronization of PCM output data with SDIBCK/SDIWCK, or SDOBCK/SDOWCK can be selected according to the setting of the control register.

One of the following parameters can be selected according to the setting of the control registers:

SDI0 or SDI1 port selection, phase of bit and word clocks, input and output data formats, numbers of data bits.

Please refer to "INPUT/OUTPUT DATA FORMAT".

3. Input Data Status AC3DATA, MUTE, CRC, KARAOKE, SURENC, 2/0 MODE

Status of SDI input signal can be known by monitoring signals outputted from the AC3DATA, MUTE, CRC, KARAOKE, SURENC and 2/0 MODE terminals. The status of these terminals can be also known by reading the register (address 0x2F).

Conditions that make the output terminal level "H" are as follows.

AC3DATA	When the SDI input signal is non-PCM encoded Audio data based on the IEC958 interface format data.
CRC	When there is a CRC error in the AC-3 bitstream data.
MUTE	When the output data of SDO0 ~ SDO2 are auto-muted by finding some data error.
KARAOKE	When the SDI input data is AC-3 karaoke data.
SURENC	When the AC-3 bitstream data is in the 2/0 mode and encoded by Dolby surround.
2/0MODE	When the AC-3 bitstream data is in the 2/0 mode.

4. Stream Data STREAM0~7

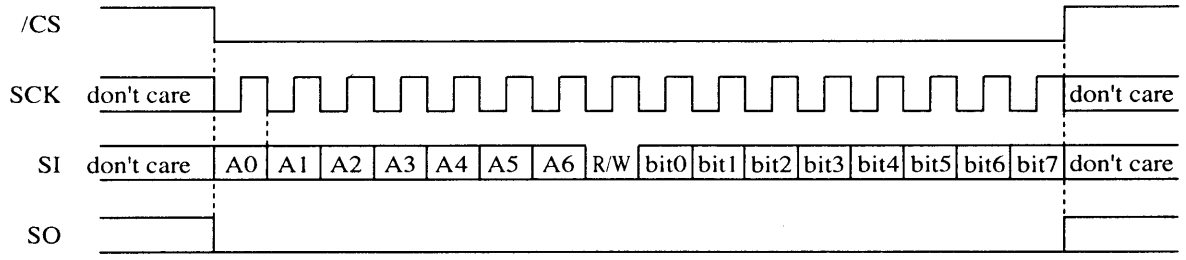
The data-stream-number (ID) whose information is included in the AC-3 bitstream data is output at STREAM 0~7 terminals. Also, the status of these terminals can be checked by reading the register (address 0x2E).

5. Microprocessor Interface /CS, SCK, SI, SO

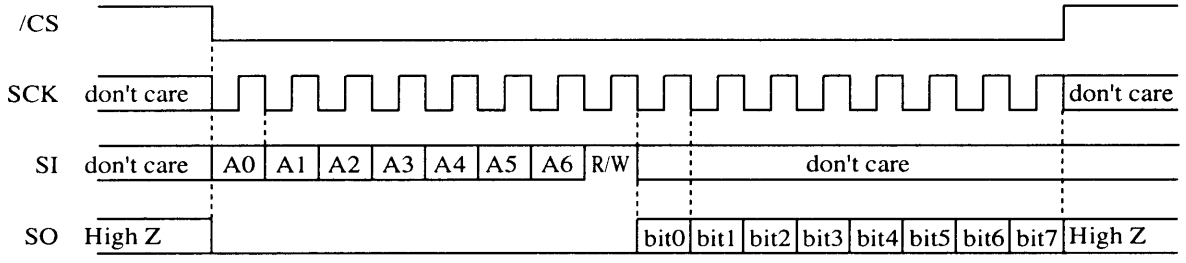
The control registers can be read/written via the microprocessor interface.

Please refer to the following format chart for the details of read/write timing.

○Register Write Timing



○Register Read Timing



Data read/write method

When writing data:

Enter the address bits (A0 ~ A6) of the register to be written from the SI terminal (the first 7 bits synchronized with SCK) and set the R/W bit to "0". Then enter the data (bits 0~7) from the SI terminal following the R/W bit.

When reading data:

Enter the address bits (A0 ~ A6) of the register to be read from the SI terminal (the first 7 bits synchronized with SCK) and set the R/W bit to "1". The register data will be outputted from the SO terminal. (9 ~ 16 bits synchronized with SCK)

Note: Both address bits (A0~6) and data bits (bit 0~7) should be inputted with LSB first.

6. General Purpose I/O Ports OPORT7~0, IPORT7~0

OPORT7 ~ 0 terminals are data output ports for general purpose. Data written on the control register (address 0x04) is outputted from these terminals.

IPORT7 ~ 0 terminals are data input ports for general purpose. Data inputted to these terminals can be read from the control register (address 0x05).

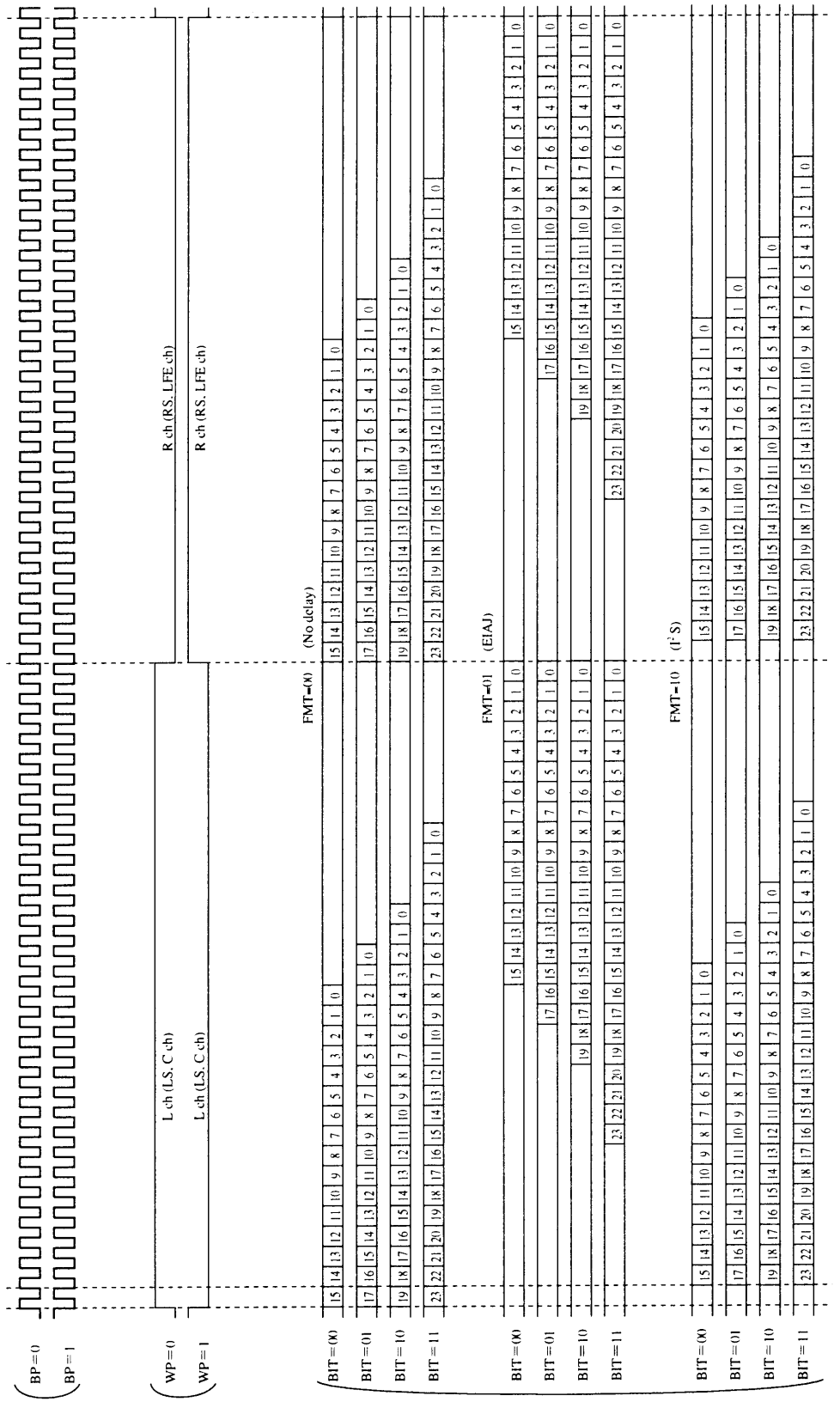
7. Initial Clear /IC

This LSI requires initial clear when turning on the power.

8. LSI Test Terminals TESTI0~30, TESTR1,2, TESTBRK, TESTCKO

TESTI0~30, TESTR1,2, TESTBRK and TESTCKO are LSI test terminals. Leave them open in normal use.

■ INPUT/OUTPUT DATA FORMAT



■ CONTROL REGISTER

The AC-3 decoding system is controlled by reading and writing the control registers through microprocessor interface (/CS, SCK, SI, SO).

* All bits are set to "0" by initial clear (/IC=0) except for PLL0 (bit 4) of PLL/DSN register (0x00).

Address	NAME	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00	PLL/DSN Register	PLLUSE	PLL2~0			DSNIGN	DSN2~0		
0x01	Mute Register	LMUTEN	CMUTEN	RMUTEN	RSMUTEN	LSMUTEN	LFEMUTEN	(not used)	AMOFF
0x02	SDI Register	SDISEL	(not used)	SDIFMT1~0		SDIBIT1~0		SDIWP	SDIBP
0x03	SDO Register	SDOCKSEL	(not used)	SDOFMT1~0		SDOBIT1~0		SDOWP	SDOBP
0x04	OPORT Register	OPORT7~0							
0x05	IPORT Register	IPORT7~0 (write disable)							
0x06	Test Register 0	(write inhibited)							
0x07	Test Register 1	(write inhibited)							
0x08	(not used)	(not used)							
0x09	Noise Level Register	NOISELEV7~0							
0x0A	Center Delay Register	(not used)					CDELAY2~0		
0x0B	Surround Delay Register	(not used)				SRDELAY3~0			
0x0C	Noise Register	NOISE	PN/WN	(not used)					
0x0D	FS Register	(not used)						FS1~0	
0x0E	L Volume Register	LVOL7~0							
0x0F	C Volume Register	CVOL7~0							
0x10	R Volume Register	RVOL7~0							
0x11	LS Volume Register	LSVOL7~0							
0x12	RS Volume Register	RSVOL7~0							
0x13	LFE Volume Register	LFEVOL7~0							
0x14	Compression Register	EMPON	AIBON	VOLON	DITHOFF	P11OFF	DIALOFF	COMPMOD1~0	
0x15	HDYNRNG Register	HDYNRNG7~0							
0x16	LDYNRNG Register	LDYNRNG7~0							
0x17	Mode Register	AC3/PCM	PLDECON	PLSRMOD	DUALMOD1~0		OUTMOD2~0		

Addresses below (0x18~0x2F) are read only (write disable) registers.

Address	NAME	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x18	Bitstream Register 0	fscod		frmsizecod					
0x19	Bitstream Register 1	bsid					bsmod		
0x1A	Bitstream Register 2	acmod			cmixlev		surmixlev		lfeon
0x1B	Bitstream Register 3	dsurmod		copyrightb	origbs	0	0	0	0
0x1C	Bitstream Register 4	0	0	0	dialnorm				
0x1D	Bitstream Register 5	0	0	0	dialnorm2				
0x1E	Bitstream Register 6	audprodie	mixlevel					roomtyp	
0x1F	Bitstream Register 7	audprodi2e	mixlevel2					roomtyp2	
0x20	Bitstream Register 8	timecod1e	0	timecod1					
0x21	Bitstream Register 9	timecod1							
0x22	Bitstream Register 10	timecod2e	0	timecod2					
0x23	Bitstream Register 11	timecod2							
0x24	Bitstream Register 12	langcode	langcod2e	compre	compr2e	0	0	0	0
0x25	Bitstream Register 13	langcod							
0x26	Bitstream Register 14	langcod2							
0x27	Bitstream Register 15	compr							
0x28	Bitstream Register 16	compr2							
0x29	Bitstream Register 17	dynrng							
0x2A	Bitstream Register 18	dynrng2							
0x2B	(not used)	(write disable, all "0" out when read)							
0x2C									
0x2D									
0x2E	Data Stream Register	STREAM7	STREAM6	STREAM5	STREAM4	STREAM3	STREAM2	STREAM1	STREAM0
0x2F	Status Register	0	0	2/0MODE	SURENC	KARAOKE	MUTE	CRC	AC3DATA

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	VDD	Vss-0.5	Vss+7.0	V
Input Voltage	VI	Vss-0.5	VDD+0.5	V
Storage Temperature	Tstg	-50	+125	℃

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD	4.75	5.0	5.25	V
Operating Temperature	Top	0	25	70	℃

3. DC Characteristics (Condition :VDD=5.0±0.25V, Ta=0~70℃)

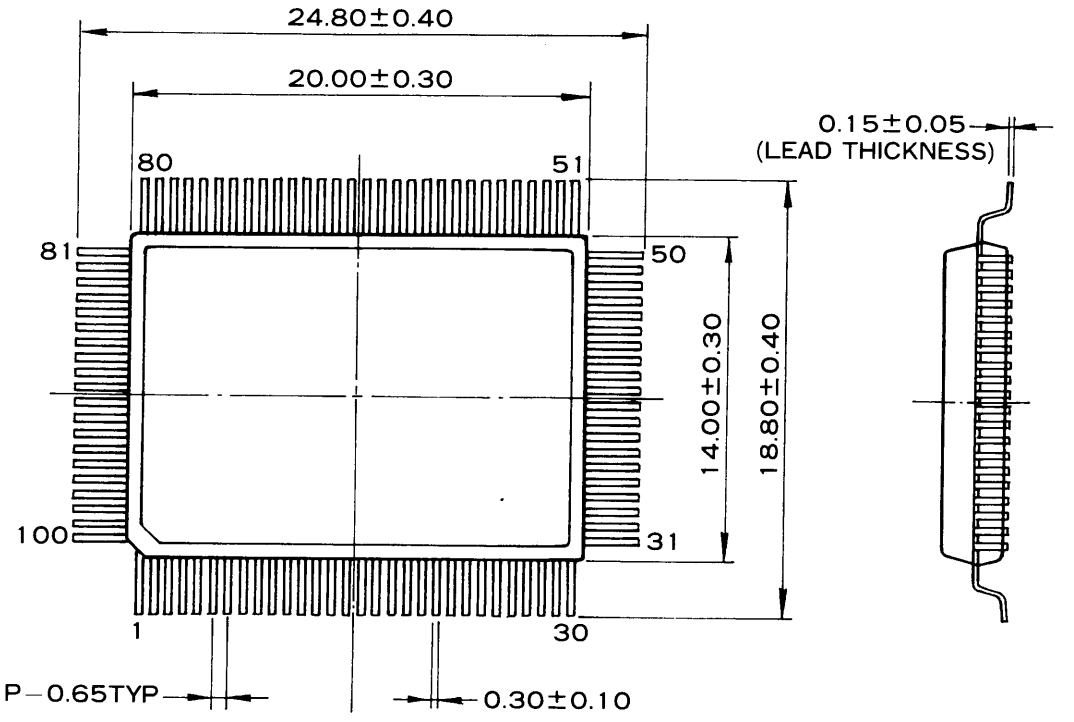
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Consumption	PD	XI=40MHz, PLL not used		500		mW
Input Voltage H Level	VIH	*1)	0.7VDD			V
		*2)	2.2			V
Input Voltage L Level	VIL	*1)			0.2VDD	V
		*2)			0.8	V
Output Voltage H Level	VOH	IOH=-80 μA	VDD-1.0			V
Output Voltage L Level	VOL	IOL=1.6mA			0.4	V
Input Leakage Current	ILI	Terminal without a pull-up resistor	-10		10	μA
Pull-up Resistor	RU		25		100	kΩ

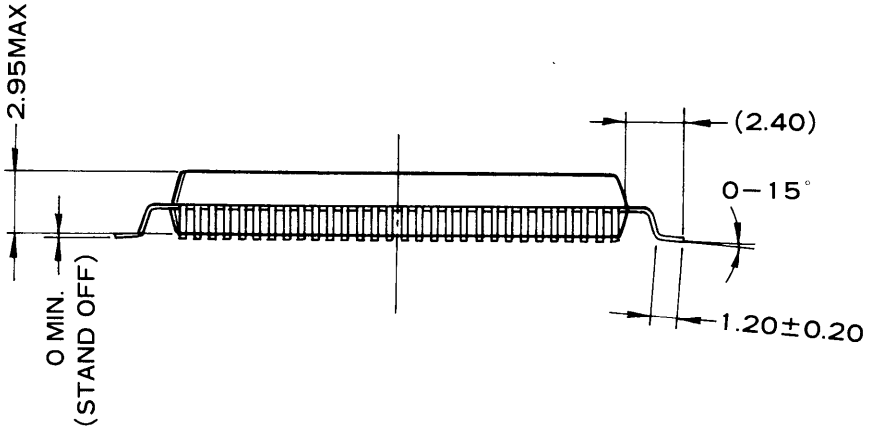
*1) Applicable to XI and /IC input terminals.

*2) Applicable to input terminals except XI and /IC terminals.

■ EXTERNAL DIMENSIONS

C-PK100FP-1





カッコ内の寸法値は参考値とする
モールド外形寸法はバリを含まない
単位(UNIT):mm

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

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