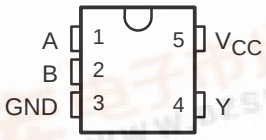
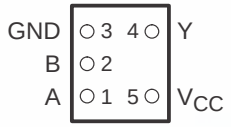
- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 4 ns at 3.3 V
- Low Power Consumption, 10-μA Max $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**DBV OR DCK PACKAGE**
**(TOP VIEW)**




**YEA, YEP, YZA, OR YZP PACKAGE**
**(BOTTOM VIEW)**




## description/ordering information

This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1G86 performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING‡ |
|---|---|---|---|---|
| –40°C to 85°C | NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA | Reel of 3000 | SN74LVC1G86YEAR | _ _ _CH_ |
| | NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free) | | SN74LVC1G86YZAR | |
| | NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP | | SN74LVC1G86YEPR | |
| | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | | SN74LVC1G86YZPR | |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74LVC1G86DBVR | C86_ |
| | | Reel of 250 | SN74LVC1G86DBVT | |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74LVC1G86DCKR | CH_ |
| | | Reel of 250 | SN74LVC1G86DCKT | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site. YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

## description/ordering information (continued)

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

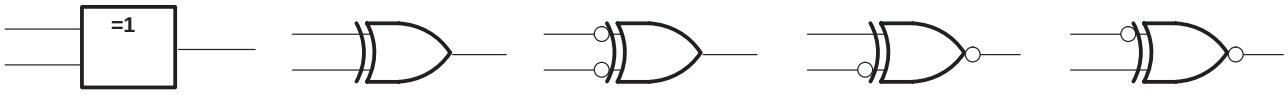
**FUNCTION TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

## exclusive-OR logic

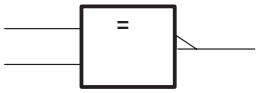
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

**EXCLUSIVE OR**




These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**

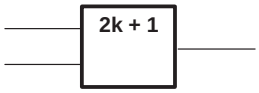



The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

**EVEN-PARITY ELEMENT**


The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**




The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | –0.5 V to 6.5 V |
| Input voltage range, $V_I$ (see Note 1) | –0.5 V to 6.5 V |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | –0.5 V to 6.5 V |
| Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) | –0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0) | –50 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0) | –50 mA |
| Continuous output current, $I_O$ | ±50 mA |
| Continuous current through $V_{CC}$ or GND | ±100 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package | 206°C/W |
| DCK package | 252°C/W |
| YEA/YZA package | 154°C/W |
| YEP/YZP package | 132°C/W |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $0.7 \times V_{CC}$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $0.3 \times V_{CC}$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 10 | |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 5 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 1.65 V to 5.5 V | $V_{CC}$–0.1 | | | V |
| | | $I_{OH}$ = –4 mA | | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = –8 mA | | 2.3 V | 1.9 | | | |
| | | $I_{OH}$ = –16 mA | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | | 2.3 | | | |
| | | $I_{OH}$ = –32 mA | | 4.5 V | 3.8 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 1.65 V to 5.5 V | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.3 | |
| | | $I_{OL}$ = 16 mA | | 3 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | | | | 0.55 | |
| | | $I_{OL}$ = 32 mA | | 4.5 V | | | 0.55 | |
| $I_I$ | A or B input | $V_I$ = 5.5 V or GND | | 0 to 5.5 V | | | ±5 | μA |
| $I_{off}$ | | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 1.65 V to 5.5 V | | | 10 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V | | | 500 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 6 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## switching characteristics over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 2.1 | 9.1 | 1 | 4.5 | 0.6 | 4 | 0.8 | 3.3 | ns |

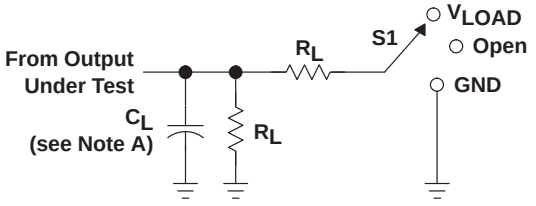
## switching characteristics over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 3.5 | 9.9 | 1.8 | 5.5 | 1.3 | 5 | 1 | 4 | ns |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 22 | 22 | 22 | 24 | pF |

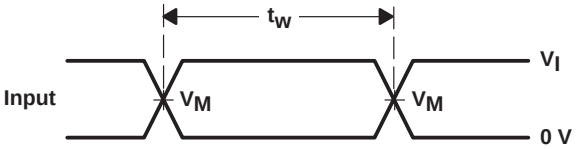
## PARAMETER MEASUREMENT INFORMATION



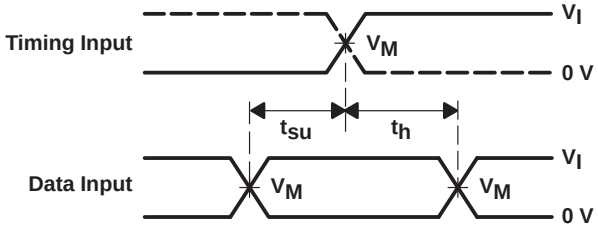

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

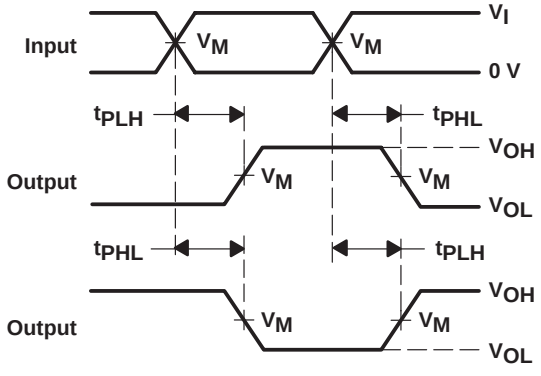
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 15 pF | 1 MΩ | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 MΩ | 0.3 V |



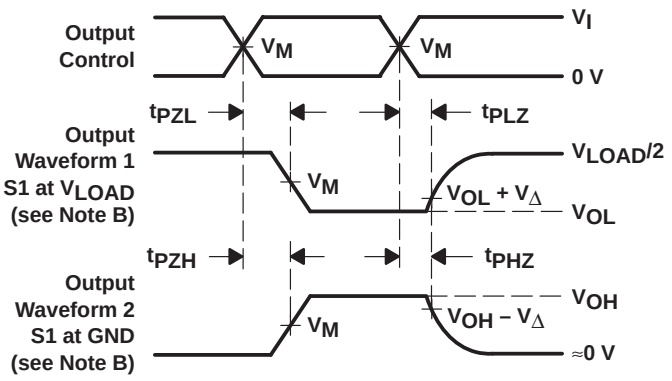

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

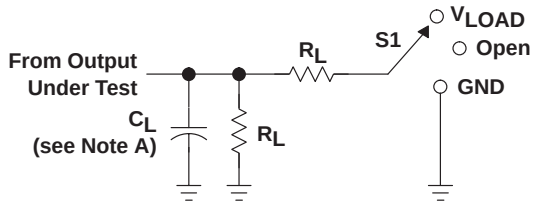



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

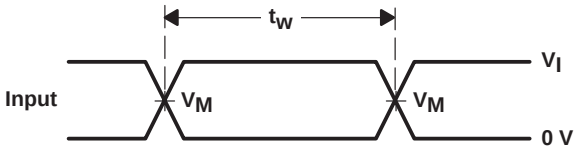
## PARAMETER MEASUREMENT INFORMATION



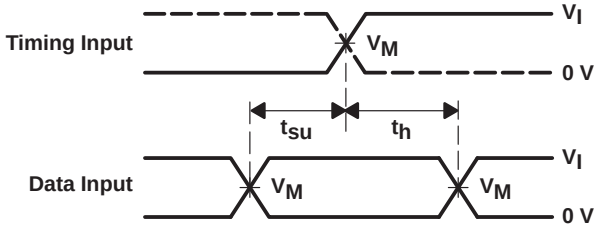

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

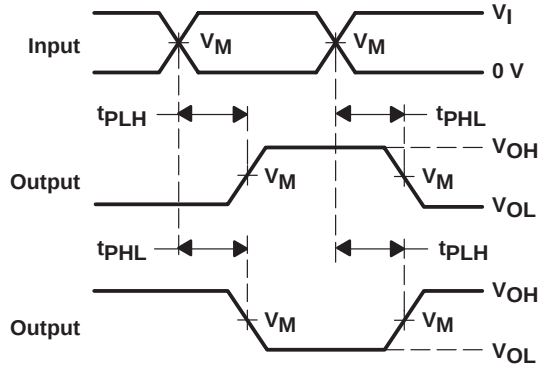
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



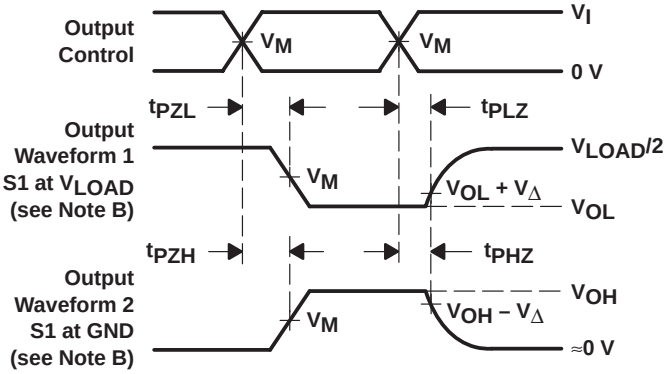

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

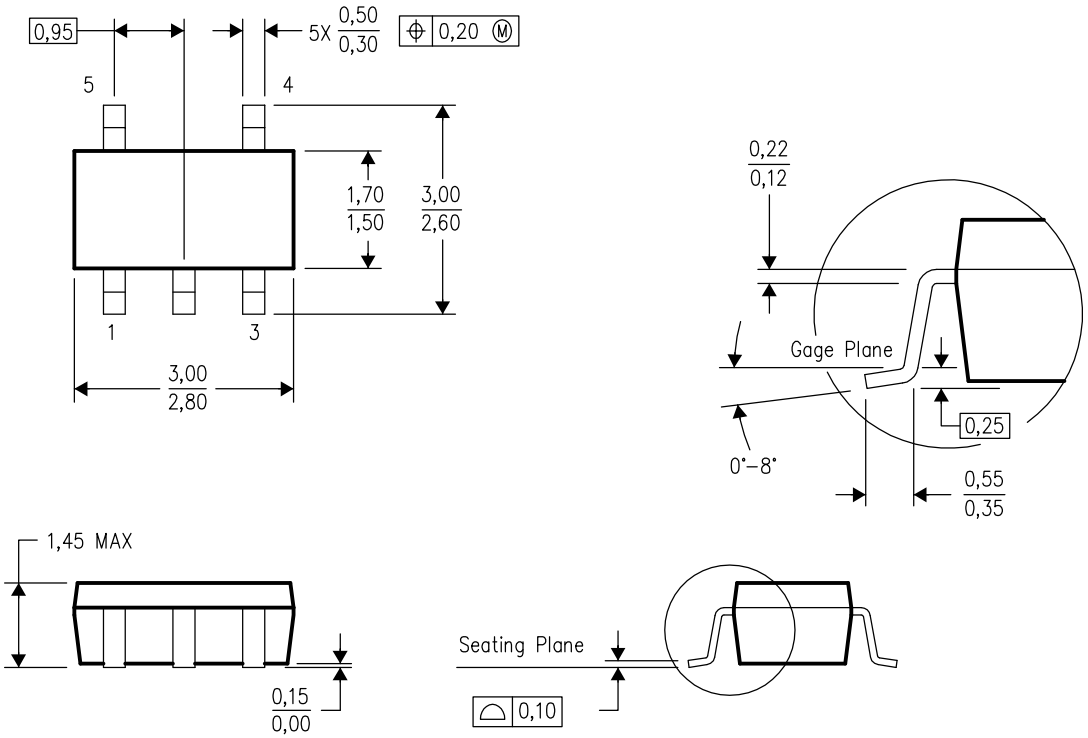
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74LVC1G86DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G86DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G86DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G86DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC1G86YEAR | ACTIVE | WCSP | YEA | 5 | 3000 | None | SNPB | Level-1-260C-UNLIM |
| SN74LVC1G86YEPR | ACTIVE | WCSP | YEP | 5 | 3000 | None | SNPB | Level-1-260C-UNLIM |
| SN74LVC1G86YZAR | ACTIVE | WCSP | YZA | 5 | 3000 | None | Call TI | Call TI |
| SN74LVC1G86YZPR | ACTIVE | WCSP | YZP | 5 | 3000 | Pb-Free (RoHS) | SNAGCU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

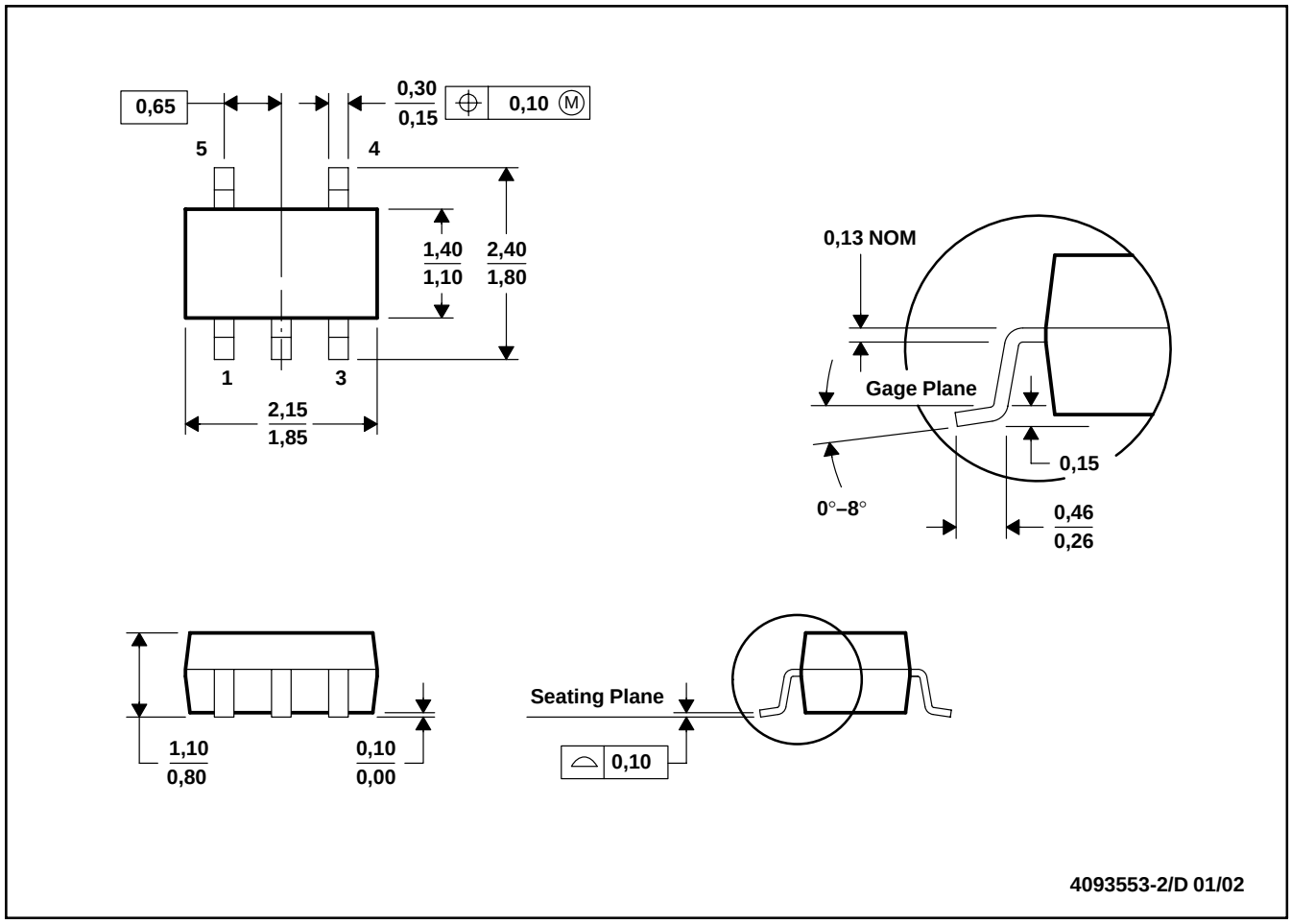
## DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/H 10/2003

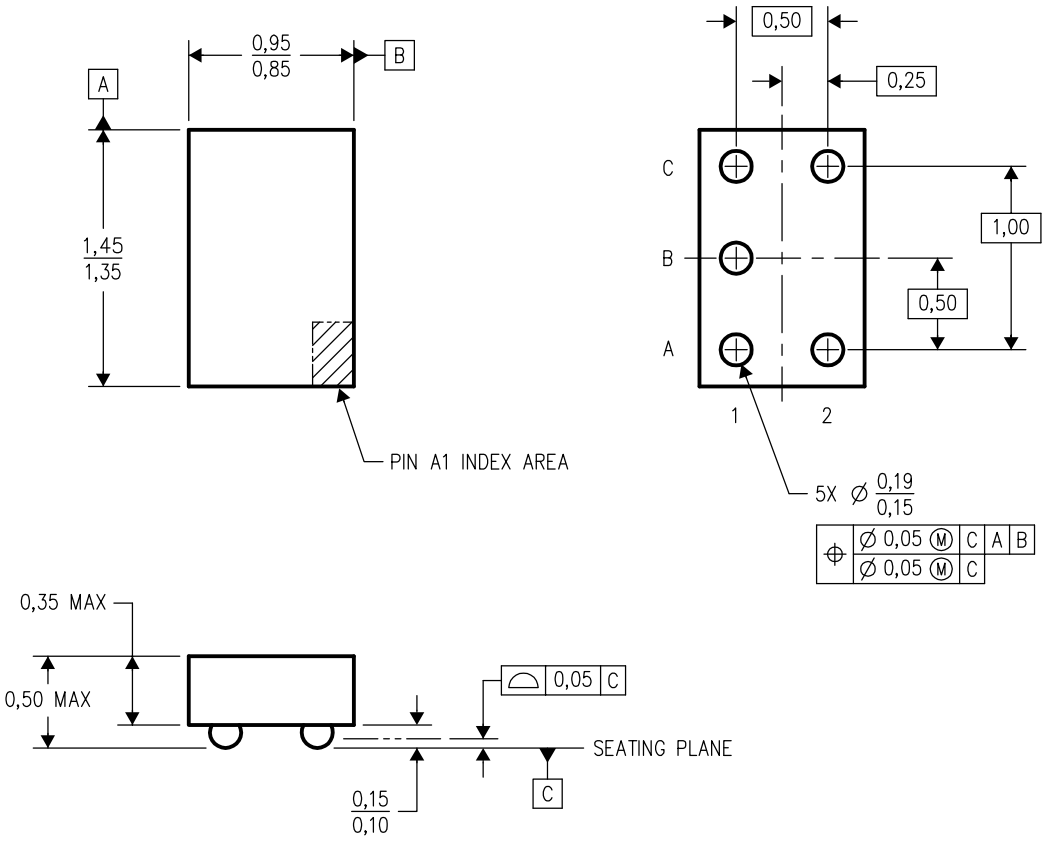
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

**DCK (R-PDSO-G5)** **PLASTIC SMALL-OUTLINE PACKAGE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

## YEA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is tin–lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead–free.

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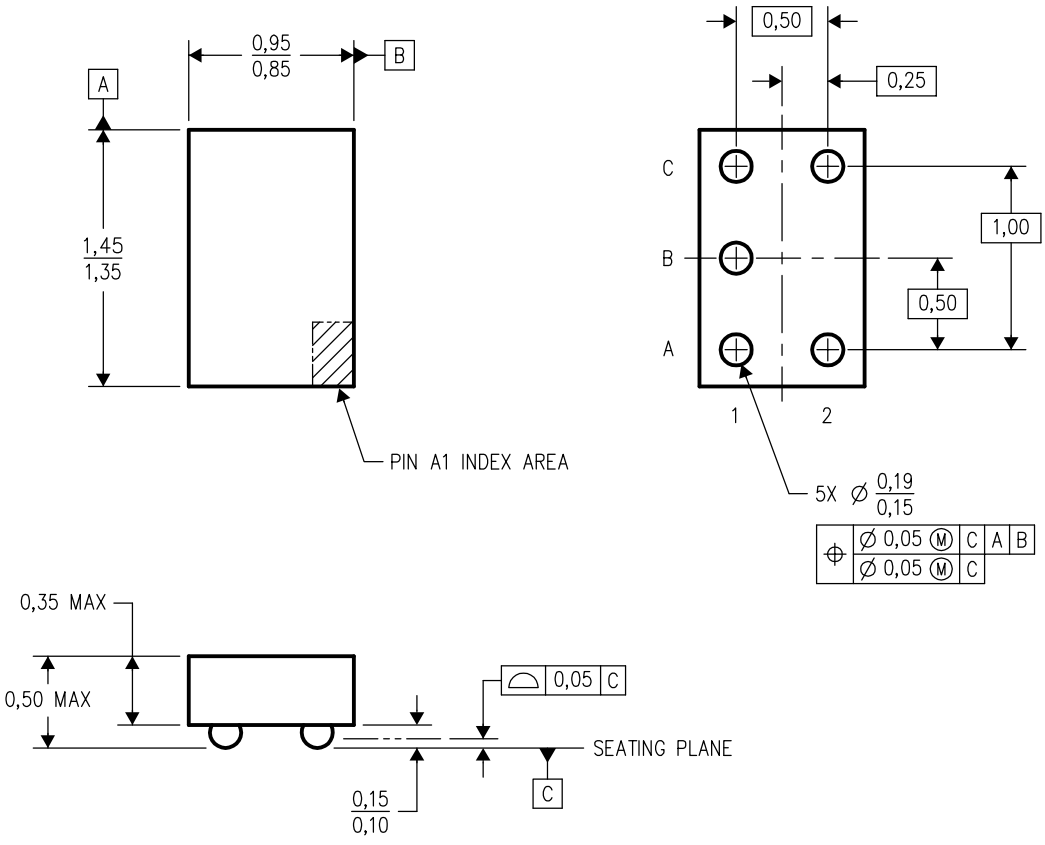
## YZA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is lead–free. Refer to the 5 YEA package (drawing 4203167) for tin–lead (SnPb).

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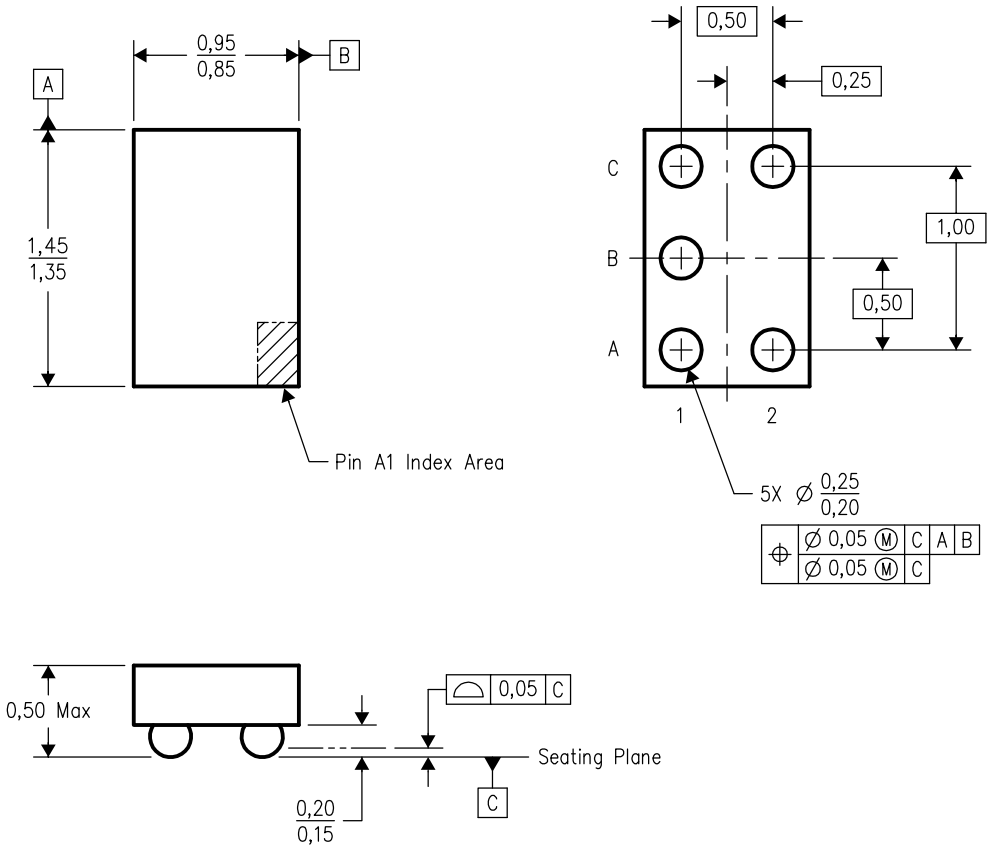
YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 5 YEP package (drawing 4204725) for tin–lead (SnPb).

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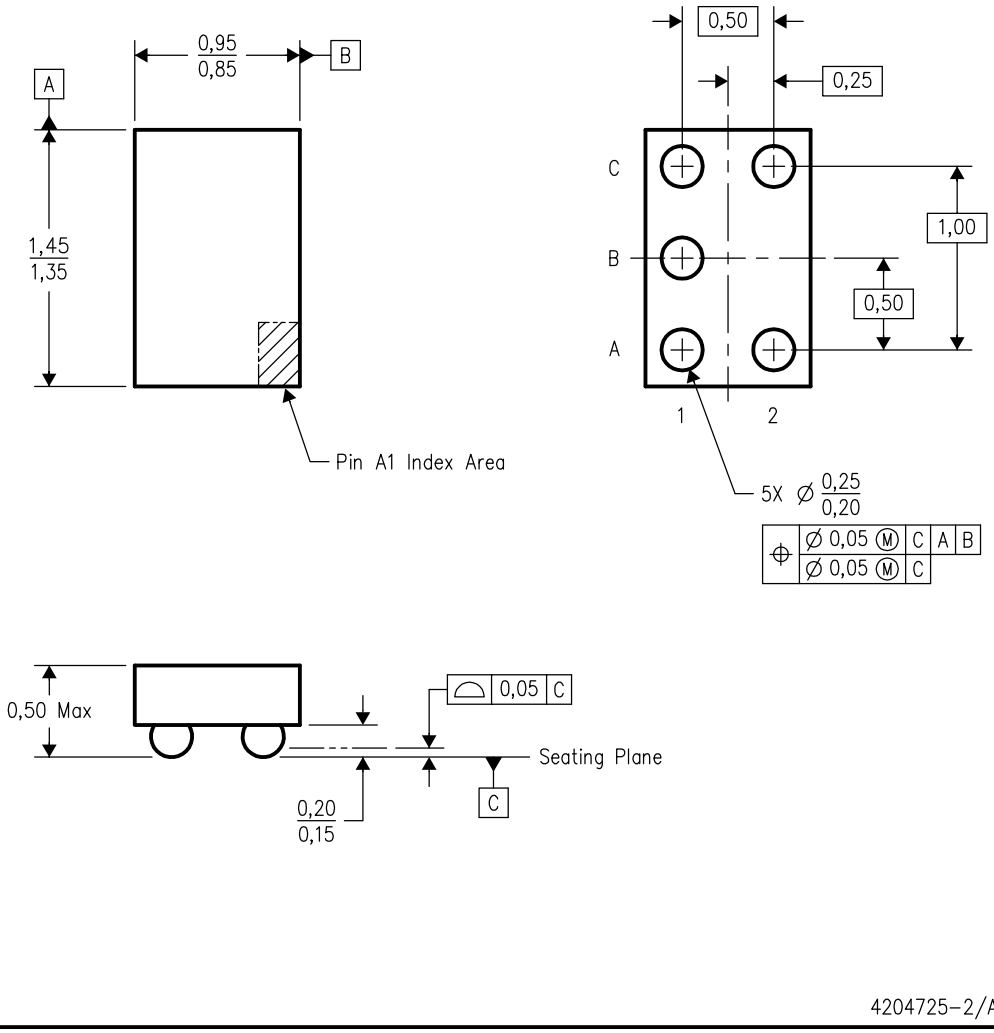
YEP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




4204725–2/A 10/2002

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead–free.

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