PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86116

CMOS Z8® PN MODULATOR WIRELESS CONTROLLER

FEATURES

Part	ROM (Kbytes)	RAM* (Kbytes)	SPEED (MHz)
Z86116	1	124	12

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0- to 5.5-Volt Operating Range
- Low-Power Consumption
- 0° to +70°C Temperature Range
- Expanded Register File (ERF)
- On-Chip PN Modulator for Spread Spectrum Communications
- 12 Input/Output Lines (One with Comparator Input)
- Vectored, Prioritized Interrupts With Programmable Polarity
- Analog Comparator
- Two Programmable 8-Bit Counter/Timers Each with Two 6-Bit Programmable Prescalers
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a RC, or External Clock Drive
- Low-Voltage Protection / Low-EMI Option

GENERAL DESCRIPTION

The Z86116 Wireless Controller is a member of the Z8® single-chip microcontroller family based on Zilog's 8-bit microcontroller core. The Z86116 is designed with specific features for wireless spread spectrum applications using direct sequence pseudo-noise (PN) modulation.

Three address spaces, the Program Memory, Register File, and Expanded Register File (ERF), support a wide range of memory configurations. Through the ERF, the designer has access to three additional control registers that provide extra peripheral devices, I/O ports, and register addresses.

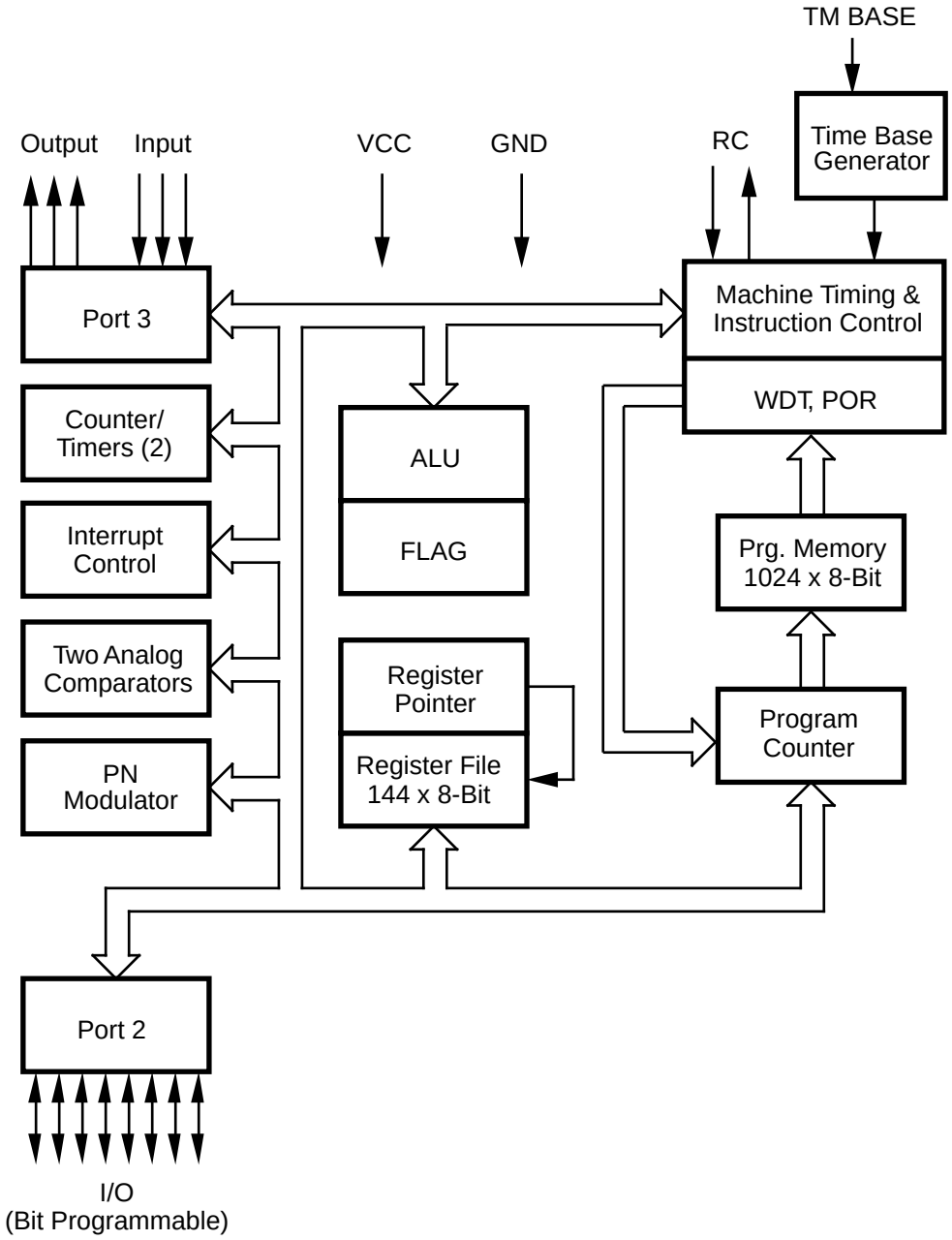
For applications demanding powerful I/O capabilities, the Z86116's dedicated input and output lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

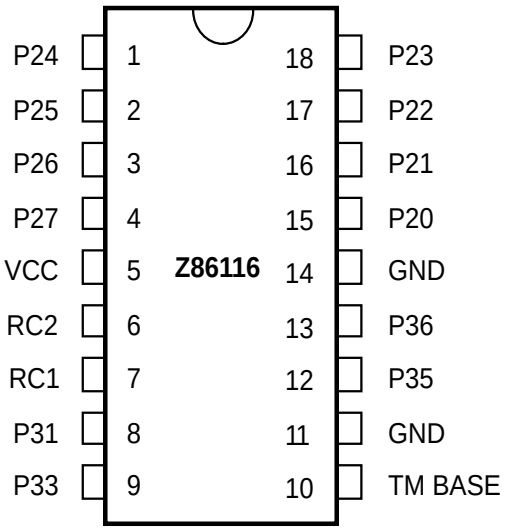
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

FUNCTIONAL DESCRIPTION



Functional Block Diagram

FUNCTIONAL DESCRIPTION (Continued)



18-Pin DIP/SOIC Pin Configuration

18-Pin DIP/SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	Input
6	RC2	RC Oscillator Clock	Output
7	RC1	RC Oscillator Clock	Input
8-9	P31, P33	Port 3, Pins 1, 3	Fixed Input
10	TM BASE	Time Base Clock	Input
11	GND	Ground	
12-13	P35-36	Port 3, Pins 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-23	Port 2, Pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

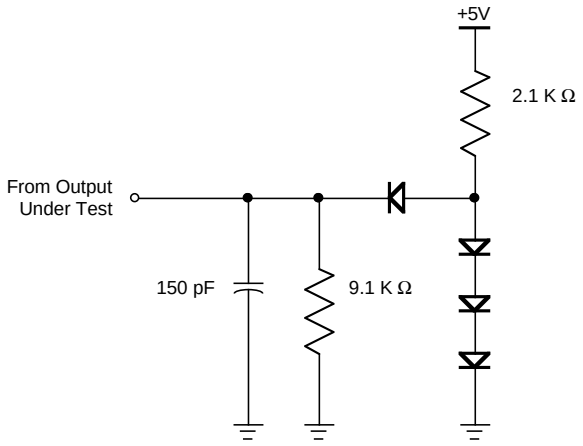
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†		C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Test Load Configuration).



Test Load Configuration

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	3.0V		12		V	$I_{IN} \leq 250\ \mu A$	
		5.5V		12		V	$I_{IN} \leq 250\ \mu A$	
V_{CH}	Clock Input High Voltage	3.0V	0.9 V_{CC}	V_{CC} +0.3	2.4	V	Driven by External Clock Generator	
		5.5V	0.9 V_{CC}	V_{CC} +0.3	3.9	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS} –0.3	0.2 V_{CC}	1.6	V	Driven by External Clock Generator	
		5.5V	V_{SS} –0.3	0.2 V_{CC}	2.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.8	V		
V_{IL}	Input Low Voltage	3.0V	V_{SS} –0.3	0.2 V_{CC}	1.0	V		
		5.5V	V_{SS} –0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC} –0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC} –0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.8	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.0	0.4	V	I_{OL} = 6 mA, 3 Pin Max	
		5.5V		1.0	0.5	V	I_{OL} = +12 mA, 3 Pin Max	
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		
		5.5V		25	10	mV		
I_{IL}	Input Leakage (Input bias current of comparator)	3.0V	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	
I_{CC}	Supply Current	3.0V		8.0	4.5	mA	@ 12 MHz	[2,3]
		5.5V		15	9.0	mA	@ 12 MHz	[2,3]
		4.5V		15	10	µA	10 kHz; External RC	[2,5]

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5	2.0	mA	HALT mode V_{IN} = OV, V_{CC} @ 12 MHz	[2,3]
		5.5V		7.0	4.0	mA	HALT mode V_{IN} = OV, V_{CC} @ 12 MHz	[2,3]
		3.0V		2.0	1.0	mA	Clock Divide-by-16 @ 12 MHz	[2 3]
		5.5V		4.5	2.5	mA	Clock Divide-by-16 @ 12 MHz	[2,3]
I_{CC2}	Standby Current (STOP Mode)	3.0V		10	1.0	µA	STOP mode V_{IN} = OV, V_{CC} WDT is not Running	[4]
		5.5V		10	3.0	µA	STOP mode V_{IN} = OV, V_{CC} WDT is not Running	[4]
		3.0V		TBD		µA	STOP mode V_{IN} = OV, V_{CC} WDT is Running	[4]
		5.5V		TBD	200	µA	STOP mode V_{IN} = OV, V_{CC} WDT is Running	[4]
		5.5V		12	5	µA	STOP Mode; TM BASE = 32.768 KHz; WDT is not Running	[6]
T_{POR}	Power-On Reset	3.0V	7	24	13	ms		
		5.5V	3	13	7	ms		
V_{BO}	V_{CC} Low Voltage Protection Voltage		1.50	2.65	2.1	V	2 MHz max Ext. CLK Freq.	[1]

Notes

[1] V_{LV} increases as the temperature decreases.

[2] All outputs unloaded, I/O pins floating, inputs at either rail, TM BASE clock input grounded.

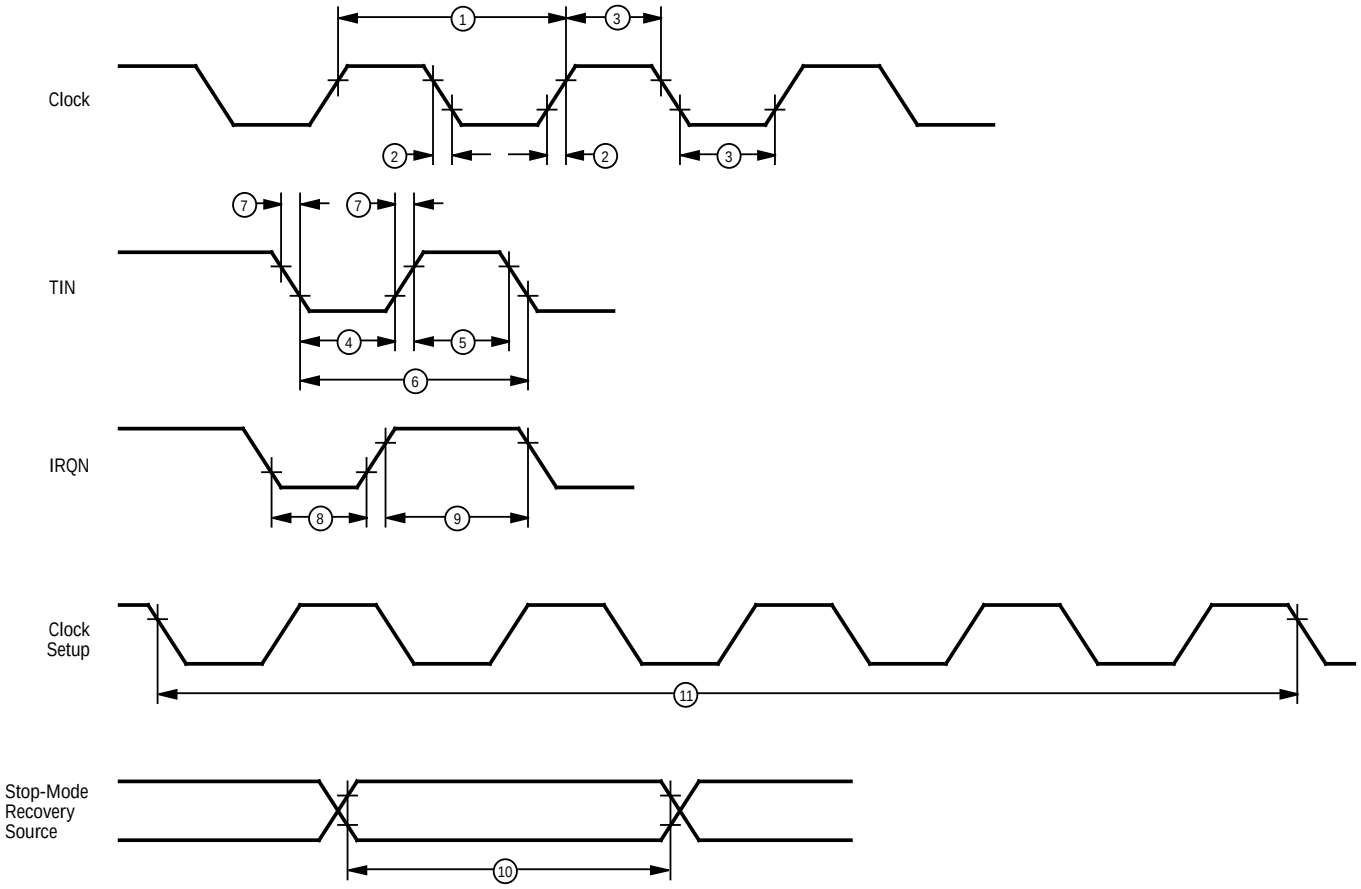
[3] $C_{L1} = C_{L2}$ = 100 pF.

[4] Same as note [2] except inputs at V_{CC}.

[5] Low EMI oscillator selected;
SCLK = RC/2
RC selected for WDT;
10 kHz RC Oscillator
(corresponding to R ≈ 1.2 MΩ, C ≈ 68 pF).

[6] Z8 in STOP mode;
WDT off;
TM BASE selected as Z8 system clock source
Time base counter enabled;
V_{CC} = 5.5V.

AC ELECTRICAL CHARACTERISTICS



AC ELECTRICAL CHARACTERISTICS (Continued)

No	Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 12 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.3V	83	100,000	ns	[1]
			5.0V	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.3V		15	ns	[1]
			5.0V		15	ns	[1]
3	TwC	Input Clock Width	3.3V	26		ns	[1]
			5.0V	26		ns	[1]
4	TwTinL	Timer Input Low Width	3.3V	100		ns	[1]
			5.0V	70		ns	[1]
5	TwTinH	Timer Input High Width	3.3V	3TpC			[1]
			5.0V	3TpC			[1]
6	TpTin	Timer Input Period	3.3V	8TpC			[1]
			5.0V	8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.3V		100	ns	[1]
			5.0V		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.3V	100		ns	[1,2]
			5.0V	70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.3V	3TpC			[1,2]
			5.0V	3TpC			[1,2]
10	Twsm	Stop-Mode Recovery Width Spec	3.3V	12		ns	
			5.0V	12		ns	
11	Tost	Oscillator Startup Time	3.3V		5TpC		Reg.[4]
			5.0V		5TpC	ns	
	Twdt	Watch-Dog Timer Refresh Time	3.3V	15			[5]
			5.0V	5		ms	D0 = 0 [6, D1 = 0 [6]
			3.3V	30		ms	D0 = 1 [6]
			5.0V	16		ms	D1 = 0 [6]
			3.3V	60		ms	D0 = 0 [6]
			5.0V	25		ms	D1 = 1 [6]
			3.3V	250		ms	D0 = 1 [6]
			5.0V	120		ms	D1 = 1 [6]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] 5.0V ±0.5V, 3.3V ±0.3V.
[4] SMR-D5 = 0.
[5] Reg. WDTMR.
[6] WDT Oscillator only.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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