PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86247
40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER (4LDTC)

GENERAL DESCRIPTION

The Z86247 40-pin Low-Cost Digital Television Controller (4LDTC) introduces a new level of sophistication to single-chip architecture. The Z86247 is a member of the Z8® single-chip microcontroller family with 8 Kbytes of ROM and 236 bytes of RAM. The device is offered in a 40-pin package and is CMOS compatible. The 4LDTC offers mask programmed ROM which enables the Z8 microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program) and combines together with the Z86C27 (DTC) and Z86127 (LDTC) to provide support for high end, mid range and low end TV applications.

Zilog's 4LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86247 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller and On Screen Display (OSD) logic circuits and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and Port 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support 8 rows by 20 columns of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying high resolution (11x15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Three 8-bit PWM ports used to vary picture levels.

The 4LDTC applications demand powerful I/O capabilities. The Z86247 fulfills this with 24 pins dedicated to input or output. These lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

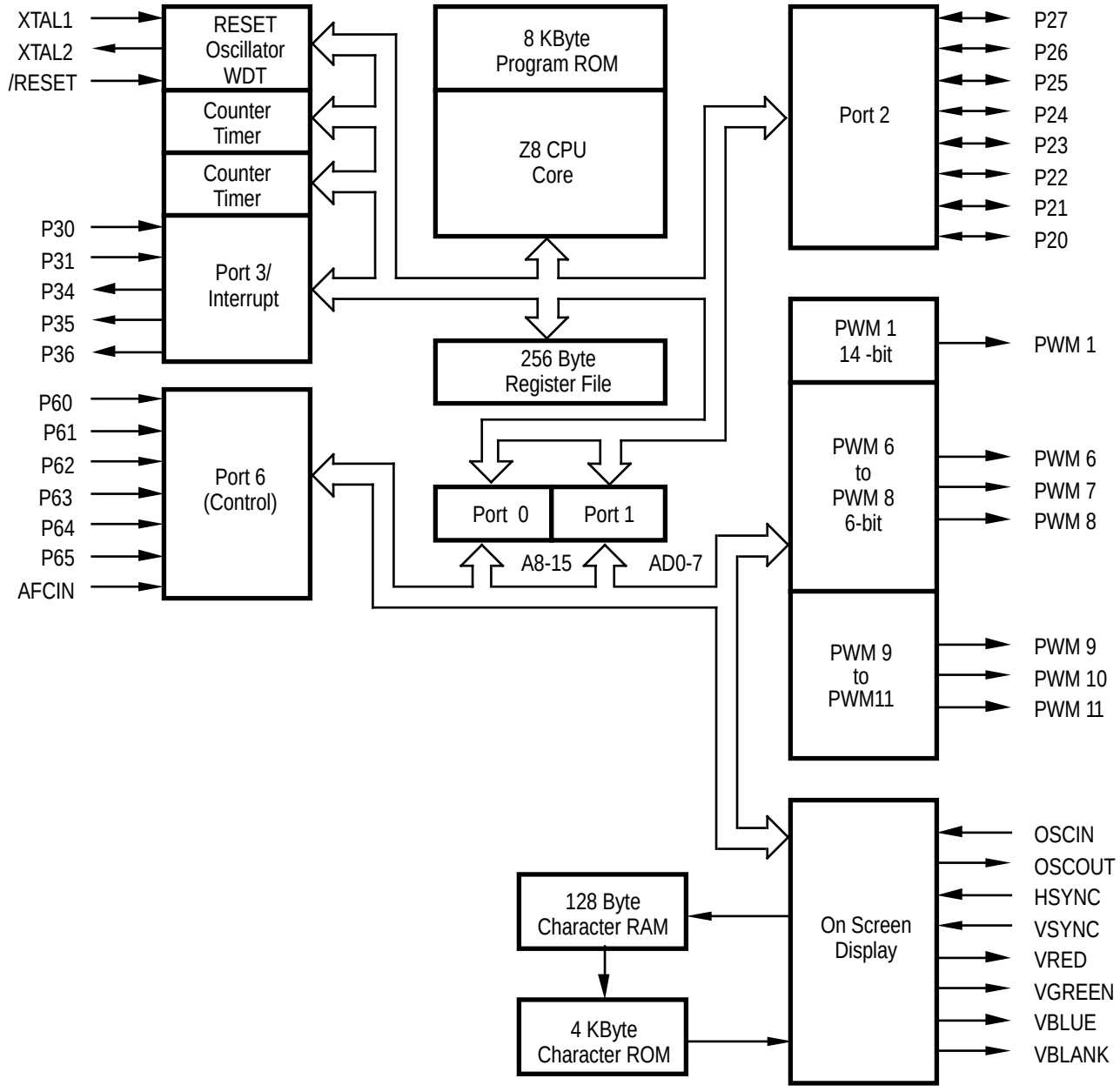
To unburden the program from coping with the real-time problems such as counting/timing and data communication, the 4LDTC offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

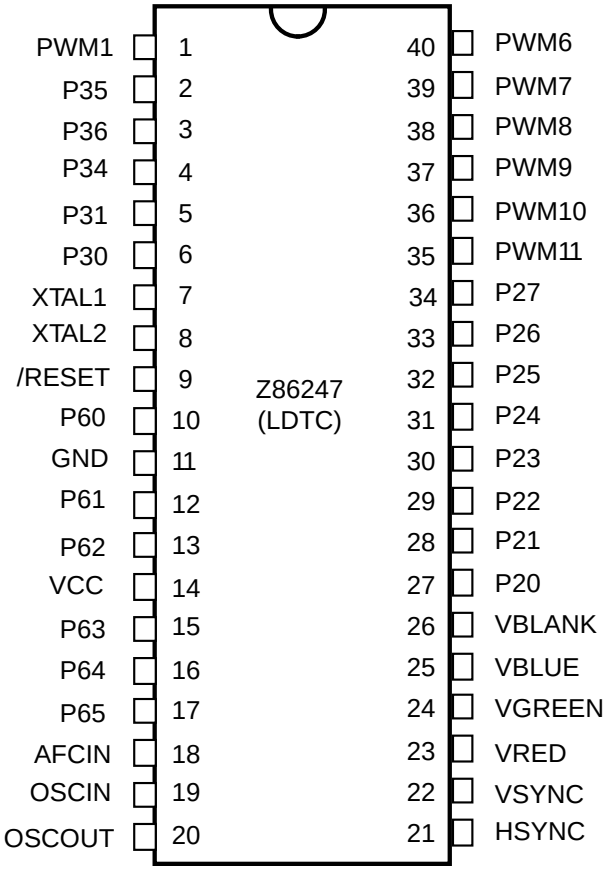
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

PIN CONFIGURATION



40-Pin Mask-ROM Plastic DIP

ABSOLUTE MAXIMUM RATINGS

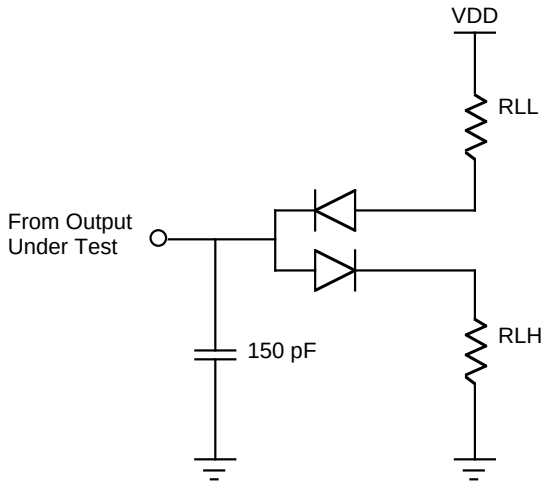
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Units	Notes
V_{CC}	Power Supply Voltage*	–0.3	+7	V	
V_I	Input Voltage	–0.3	V_{CC}+0.3	V	
V_I	Input Voltage	–0.3	V_{CC}+0.3	V	[1]
V_O	Output Voltage	–0.3	V_{CC}+8.0	V	[2,3]
I_{OH}	Output Current High		–10	mA	1 pin
I_{OH}	Output Current High		–100	mA	All total
I_{OL}	Output Current Low		20	mA	1 pin
I_{OL}	Output Current Low		200	mA	All total
T_A	Operating Temperature	†			
T_{STG}	Storage Temperature	–65	+150	C	

Notes:
[1] Port 2 open-drain
[2] PWM open-drain outputs
[3] PWM breakdown is 13.2V (normal operation). Will withstand 16V max. (non-momentary operating).
* Voltage on all pins with respect to GND.
† See Ordering Information

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

CAPACITANCE

T_A=25°C; V_{CC}=GND=0V; Freq=1.0 MHz; unmeasured pins to GND.

Parameter	Max	Units
Input capacitance	10	pF
Output capacitance	20	pF
I/O capacitance	25	pF
AFC_{IN} input capacitance	10	pF

DC CHARACTERISTICS

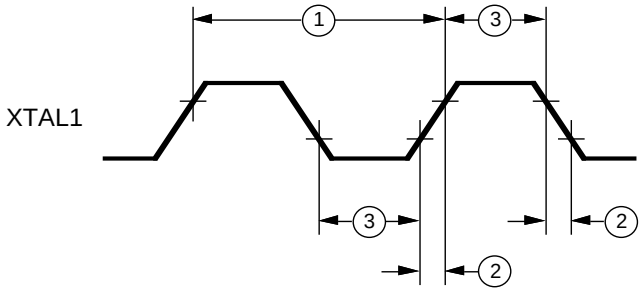
T_A=0°C to +70°C; V_{CC}=+4.5V to +5.5V; F_{OSC}=4 MHz

Sym	Parameter	T_A=0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	1.48	V	
V_{ILC}	Input XTAL/Osc In Low		0.07 V_{CC}	0.98	V	External Clock Generator Driven
V_{IH}	Input Voltage XTAL/Osc In High	0.7 V_{CC}	V_{CC}	3.2	V	External Clock Generator Driven
V_{IHC}	Input XTAL/Osc In High	0.8 V_{CC}	V_{CC}	3.0	V	External Clock Generator Driven
V_{HY}	Schmitt Hysteresis	0.1 V_{CC}		0.8	V	
V_{PU}	Maximum Pull-Up Voltage		12		V	[1]
V_{OL}	Output Voltage Low		0.4	0.16	V	I_{OL}=1.00 mA
			0.4	0.19	V	I_{OL}=0.75 mA [1]
V_{00-01}	AFC Level 01 In		0.45 V_{CC}	1.9	V	
V_{01-11}	AFC Level 11 In	0.5 V_{CC}	0.75 V_{CC}	3.12	V	
V_{OH}	Output Voltage High	V_{CC}–0.4		4.75	V	I_{OH}=–0.75 mA
I_{IR}	Reset Input Current		–80	–46	µA	V_{RL}=0V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	0V,V_{CC}
I_{OL}	Tri-State Leakage	–3.0	3.0	0.02	µA	0V,V_{CC}
I_{CC}	Supply Current		20	13.2	mA	All inputs at rail
I_{CC1}			6	3.2	mA	All inputs at rail
I_{CC2}			10	2.0	µA	All inputs at rail

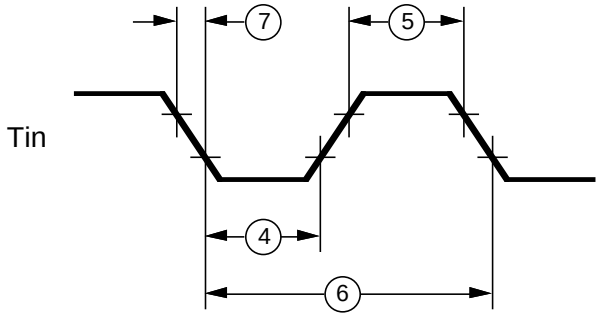
Note:
[1] PWM open-drain

AC CHARACTERISTICS

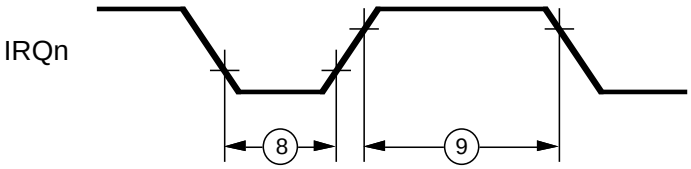
Timing Diagrams



External Clock



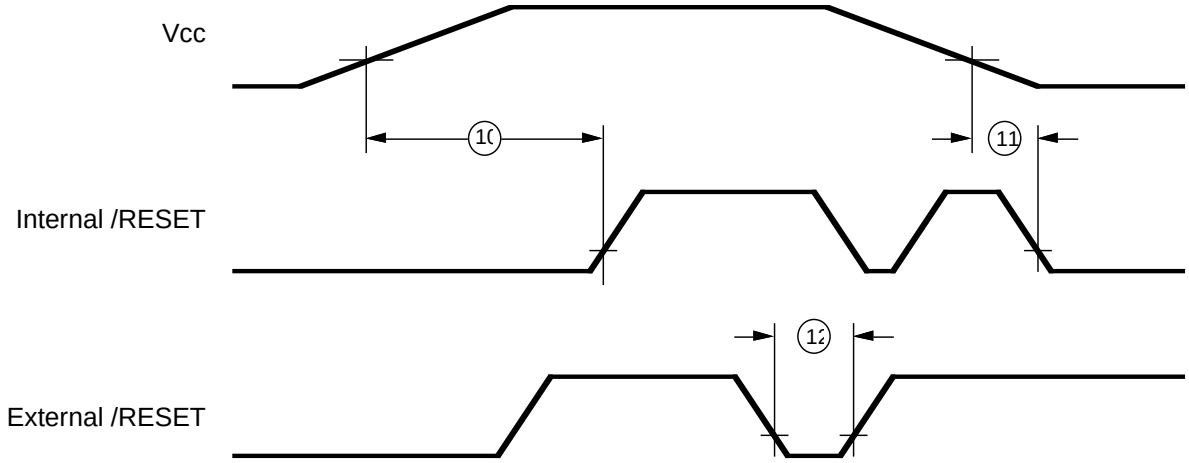
Counter Timer



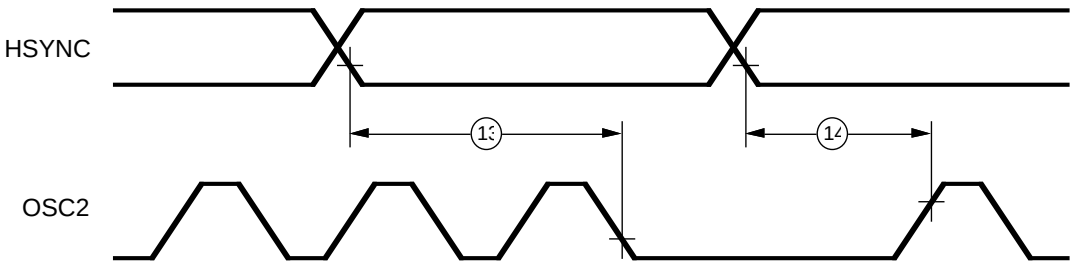
Interrupt Request

AC CHARACTERISTICS

Timing Diagrams (Continued)



Power-On Reset



On-Screen Display

AC CHARACTERISTICS

T_A=0° C to +70° C; V_{CC}=+4.5V to +5.5V; F_{OSC}=4 MHz

No	Symbol	Parameter	Min	Max	Unit
1	TpC	Input Clock Period	250	1000	ns
2	TrC,TfC	Clock Input Rise and Fall		15	ns
3	TwC	Input Clock Width	70		ns
4	TwTinL	Timer Input Low Width	70		ns
5	TwTinH	Timer Input High Width	3TpC		
6	TpTin	Timer Input Period	8TpC		
7	TrTin,TfTin	Timer Input Rise and Fall		100	ns
8a	TwIL	Int Req Input Low	70		ns
8b	TwIL		3TpC		
9	TwIH	Int Request Input High	3TpC		
10	TdPOR	Power On Reset Delay	25	100	ms
11	TdLVIRES	Low Voltage Detect to Internal RESET Condition	200		ns
12	TwRES	Reset Minimum Width	5TpC		
13	TdHsOI	H_{sync} Start to V_{osc} Stop	2TpV	3TpV	
14	TdHsOh	H_{sync} End to V_{osc} Start		1TpV	
15	TdWDT	WDT Refresh Time		12	ms

Note:
Refer to DC Characteristics for details on switching levels.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin:

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the

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