



PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86L33/L43

CMOS Z8®

CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86L33	4	237	8
Z86L43	4	236	8

* General-Purpose

- 40-Pin DIP, 44-Pin PLCC and QFP Packages (L43)
28-Pin DIP, 28-Pin SOIC (L33)
- 2.0- to 3.9-Volt Operating Range
- Low-Power Consumption
- 0°C to +70°C Operating Range
- Expanded Register File (ERF)

- 32 Input/Output Lines (L43)
24 Input/Output Lines (L33)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86L33/L43 Consumer Controller Processor (CCP™) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. This low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86L33/L43 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, External Data Memory (L43), and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers (Banks 0, D, and F)

under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86L33/L43 offers two on-chip counter/timers with a large number of user-selectable modes.

With ROM/ROMless selectivity, the Z86L43 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: /B/W (WORD is active Low); /B/W (BYTE is active Low, only).

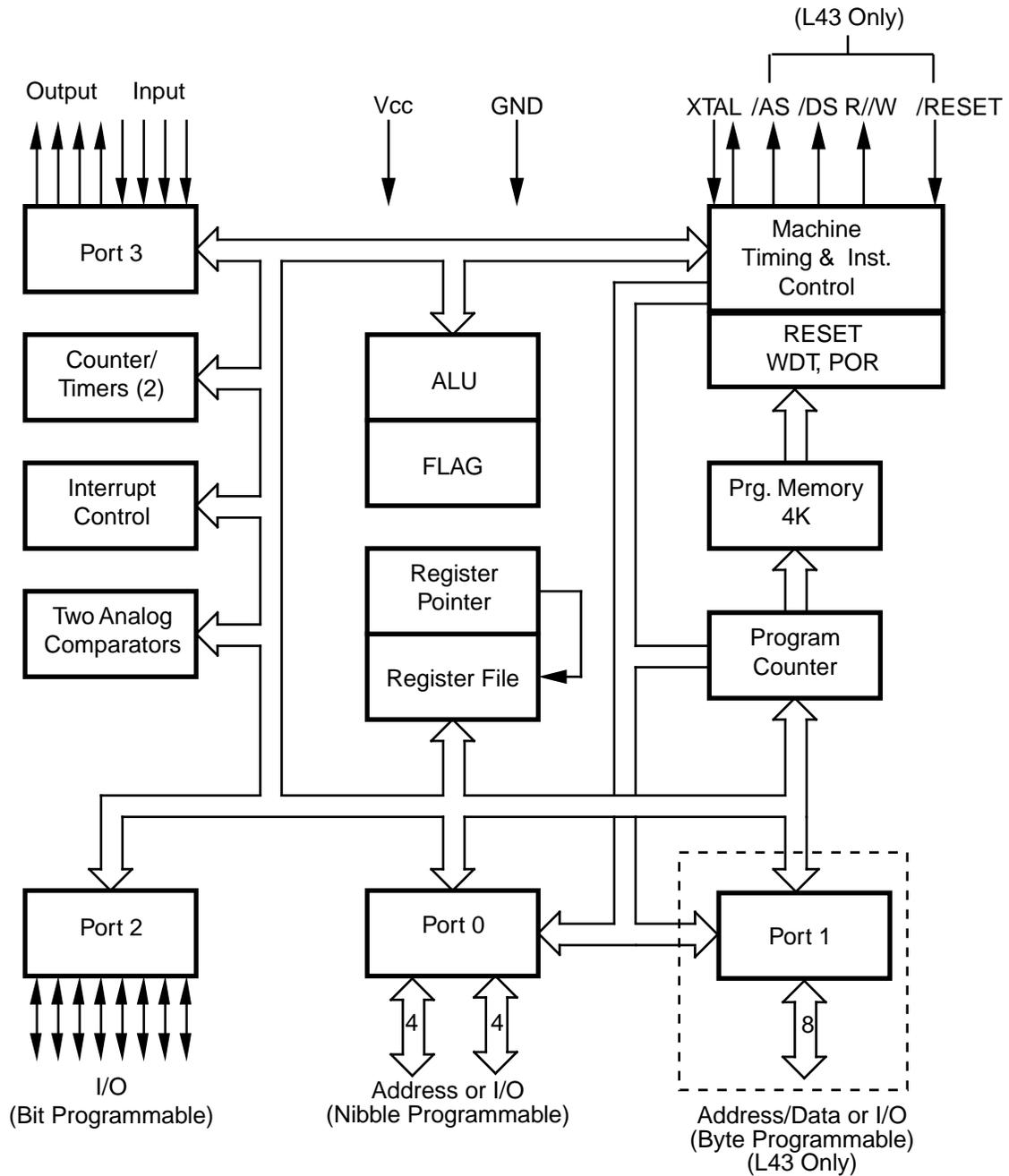
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V _{CC} GND	V _{DD} V _{SS}

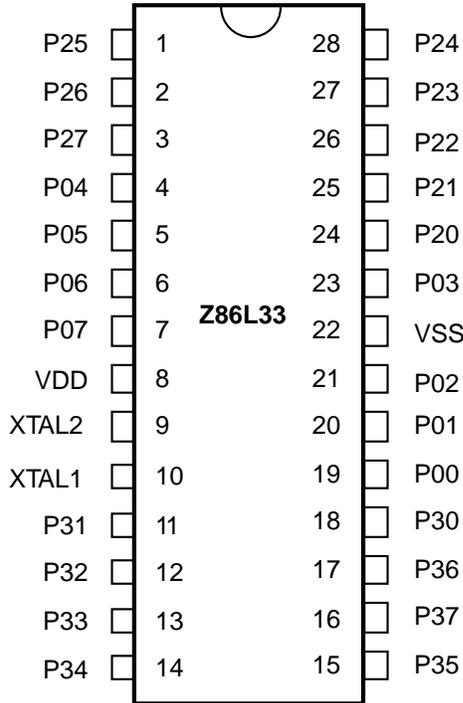
For applications demanding powerful I/O capabilities, the Z86L33 provides 24 pins, and the Z86L43 provides 32 pins dedicated to input and output. These lines are configurable



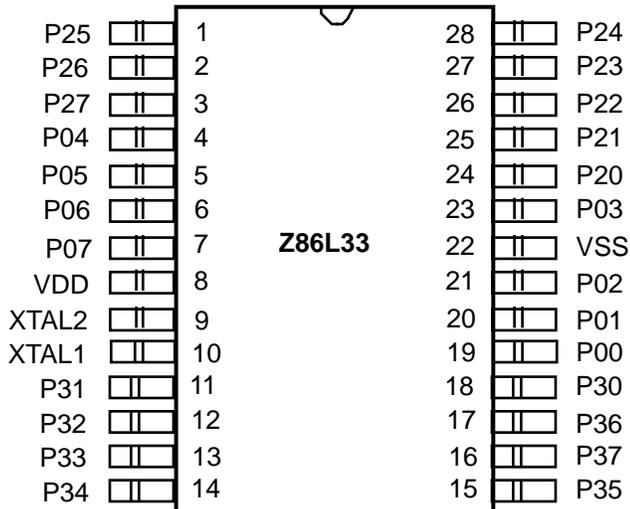
GENERAL DESCRIPTION (Continued)

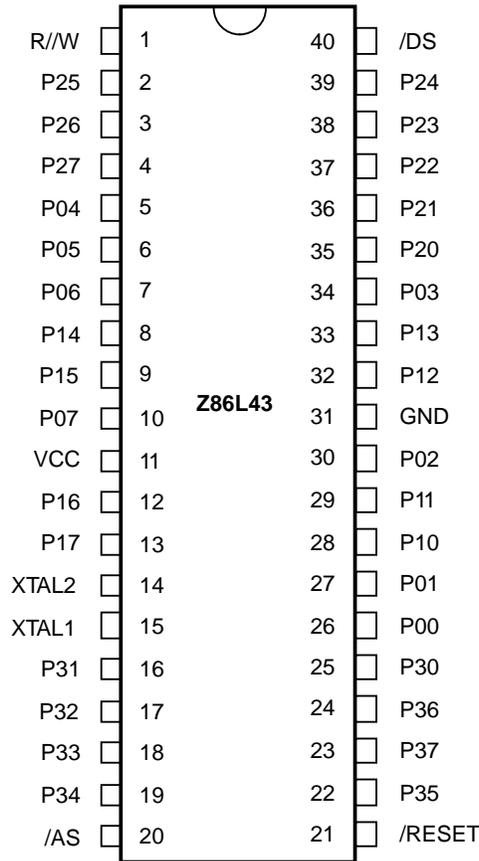


Functional Block Diagram

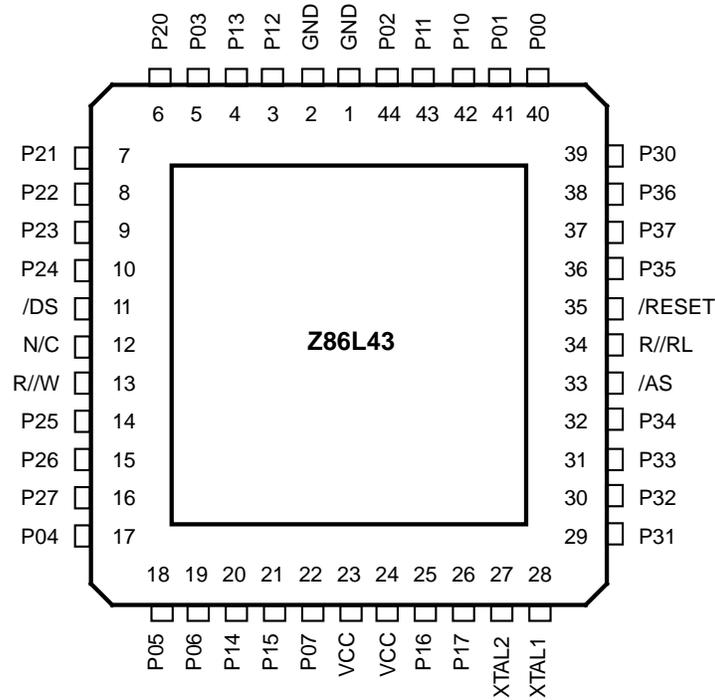
PIN DESCRIPTION

28-Pin DIP Pin Configuration
28-Pin DIP/SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-3	P27-25	Port 2, Pins 5,6,7	In/Output
4-7	P07-04	Port 0, Pins 4,5,6,7	In/Output
8	V _{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P33-31	Port 3, Pins 1,2,3	Fixed Input
14-15	P35-4	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P02-00	Port 0, Pins 0,1,2	In/Output
22	V _{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P24-20	Port 2, Pins 0,1,2,3,4	In/Output

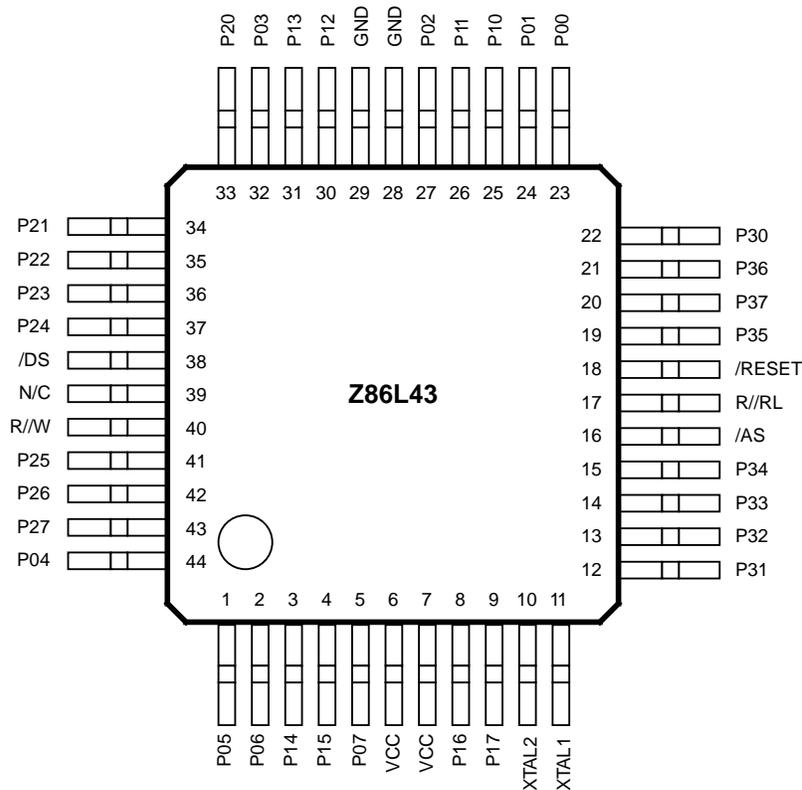

28-Pin SOIC Pin Configuration

PIN DESCRIPTION (Continued)

40-Pin DIP Assignments
40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output	22	P35	Port 3, Pin 5	Output
2-4	P25-27	Port 2, Pins 5,6,7	In/Output	23	P37	Port 3, Pin 7	Output
5-7	P04-06	Port 0, Pins 4,5,6	In/Output	24	P36	Port 3, Pin 6	Output
8-9	P14-15	Port 1, Pins 4,5	In/Output	25	P30	Port 3, Pin 0	Input
10	P07	Port 0, Pin 7	In/Output	26-27	P00-01	Port 0, Pin 0,1	In/Output
11	V _{CC}	Power Supply		28-29	P10-11	Port 1, Pin 0,1	In/Output
12-13	P16-17	Port 1, Pins 6,7	In/Output	30	P02	Port 0, Pin 2	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output	31	GND	Ground	
15	XTAL1	Crystal, Oscillator Clock	Input	32-33	P12-13	Port 1, Pin 2,3	In/Output
16-18	P31-33	Port 3, Pins 1,2,3	Input	34	P03	Port 0, Pin 3	In/Output
19	P34	Port 3, Pin 4	Output	35-39	P20-24	Port 2, Pin 0,1,2,3,4	In/Output
20	/AS	Address Strobe	Output	40	/DS	Data Strobe	Output
21	/RESET	Reset	Input				

PIN DESCRIPTION (Continued)

44-Pin PLCC Pin Assignments
44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	GND	Ground		28	XTAL1	Crystal, Oscillator Clock	Input
3-4	P12-13	Port 1, Pins 2,3	In/Output	29-31	P31-33	Port 3, Pins 1,2,3	Input
5	P03	Port 0, Pin 3	In/Output	32	P34	Port 3, Pin 4	Output
6-10	P20-24	Port 2, Pins 0,1,2,3,4	In/Output	33	/AS	Address Strobe	Output
11	/DS	Data Strobe	Output	34	R//RL	ROM/ROMless Control	Input
12	N/C	Not Connected		35	/RESET	Reset	Input
13	R/W	Read/Write	Output	36	P35	Port 3, Pin 5	Output
14-16	P25-27	Port 2, Pins 5,6,7	In/Output	37	P37	Port 3, Pin 7	Output
17-19	P04-06	Port 0, Pins 4,5,6	In/Output	38	P36	Port 3, Pin 6	Output
20-21	P14-15	Port 1, Pins 4,5	In/Output	39	P30	Port 3, Pin 0	Input
22	P07	Port 0, Pin 7	In/Output	40-41	P00-01	Port 0, Pins 0,1	In/Output
23,24	V _{CC}	Power Supply		42-43	P10-11	Port 1, Pins 0,1	In/Output
25-26	P16-17	Port 1, Pins 6,7	In/Output	44	P02	Port 0, Pin 2	In/Output
27	XTAL2	Crystal, Oscillator Clock	Output				

PIN DESCRIPTION (Continued)

44-Pin QFP Pin Assignments
44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output	21	P36	Port 3, Pin 6	Output
3-4	P14-15	Port 1, Pins 4,5	In/Output	22	P30	Port 3, Pin 0	Input
5	P07	Port 0, Pin 7	In/Output	23-24	P00-01	Port 0, Pins 0,1	In/Output
6-7	V _{CC}	Power Supply		25-26	P10-11	Port 1, Pins 0,1	In/Output
8-9	P16-17	Port 1 Pins 6,7	In/Output	27	P02	Port 0, Pin 2	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output	28-29	GND	Ground	
11	XTAL1	Crystal, Oscillator Clock	Input	30-31	P12-13	Port 1, Pins 2,3	In/Output
12-14	P31-33	Port 3, Pins 1,2,3	Input	32	P03	Port 0, Pin 3	In/Output
15	P34	Port 3, Pin 4	Output	33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
16	/AS	Address Strobe	Output	38	/DS	Data Strobe	Output
17	R//RL	ROM/ROMless Control	Input	39	N/C	Not Connected	
18	/RESET	Reset	Input	40	R/W	Read/Write	Output
19	P35	Port 3, Pin 5	Output	41-43	P25-27	Port 2, Pins 5,6,7	In/Output
20	P37	Port 3, Pin 7	Output	44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp			C
	Power Dissipation		2.2	W

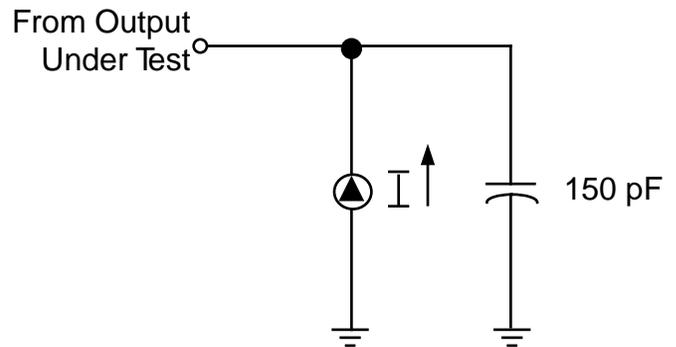
Notes:

* Voltage on all pins with respect to GND.
 See Ordering Information.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Test Load Diagram).



Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0 \text{ MHz}$, Unmeasured pins to GND

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V _{CC} Note [3]	T _A = 0° C to +70° C		Typical [13] @ 25° C	Units	Conditions	Notes
			Min	Max				
	Max Input Voltage	2.0V		7		V	I _{IN} < 250 μA	
		3.9V		7		V	I _{IN} < 250 μA	
V _{CH}	Clock Input High Voltage	2.0V	0.7 V _{CC}	V _{CC} +0.3		V	Driven by External Clock Generator	
		3.9V	0.7 V _{CC}	V _{CC} +0.3		V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0V	GND-0.3	0.2 V _{CC}		V	Driven by External Clock Generator	
		3.9V	GND-0.3	0.2 V _{CC}		V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0V	0.7 V _{CC}	V _{CC} +0.3		V		
		3.9V	0.7 V _{CC}	V _{CC} +0.3		V		
V _{IL}	Input Low Voltage	2.0V	GND-0.3	0.2 V _{CC}		V		
		3.9V	GND-0.3	0.2 V _{CC}		V		
V _{OH1}	Output High Voltage	2.0V	V _{CC} -0.4			V	I _{OH} = -2.0 mA	[8]
		3.9V	V _{CC} -0.4			V	I _{OH} = -2.0 mA	[8]
V _{OL1}	Output Low Voltage	2.0V		0.6		V	I _{OL} = +4.0 mA	[8]
		3.9V		0.4		V	I _{OL} = +4.0 mA	[8]
V _{OL2}	Output Low Voltage	2.0V		1.2		V	I _{OL} = +6 mA	[8]
		3.9V		1.2		V	I _{OL} = +12 mA	[8]
V _{RH}	Reset Input High Voltage	2.0V	.8 V _{CC}	V _{CC}		V		
		3.9V	.8 V _{CC}	V _{CC}		V		
V _{RI}	Reset Input Low Voltage	2.0V	GND-0.3	0.2 V _{CC}		V		
		3.9V	GND-0.3	0.2 V _{CC}		V		
V _{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		[10]
		3.9V		25	10	mV		[10]
I _{IL}	Input Leakage	2.0V	-1	2	<1	μA	V _{IN} = 0V, V _{CC}	
		3.9V	-1	2	<1	μA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	2.0V	-1	1	<1	μA	V _{IN} = 0V, V _{CC}	
		3.9V	-1	1	<1	μA	V _{IN} = 0V, V _{CC}	
I _{IR}	Reset Input Current	2.0V		-130	-25	μA		
		3.9V		-180	-40	μA		
I _{CC}	Supply Current	2.0V		10		mA	@ 8 MHz	[4]
		3.9V		17		mA	@ 8 MHz	[4]
I _{CC1}	Standby Current	2.0V		4.0		mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	[4]
		3.9V		6.0		mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	[4]
		2.0V		3.0		mA	Clock Divide-by-12 @ 8 MHz	[4]
		3.9V		5.0		mA	Clock Divide-by-12 @ 8 MHz	[4]
I _{CC2}	Standby Current	2.0V		8		μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	[6,11]
		3.9V		10		μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	[6,11]
		2.0V		500		μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is Running	[6,11,14]
		3.9V		800		μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is Running	[6,11,14]

DC ELECTRICAL CHARACTERISTICS (Continued)

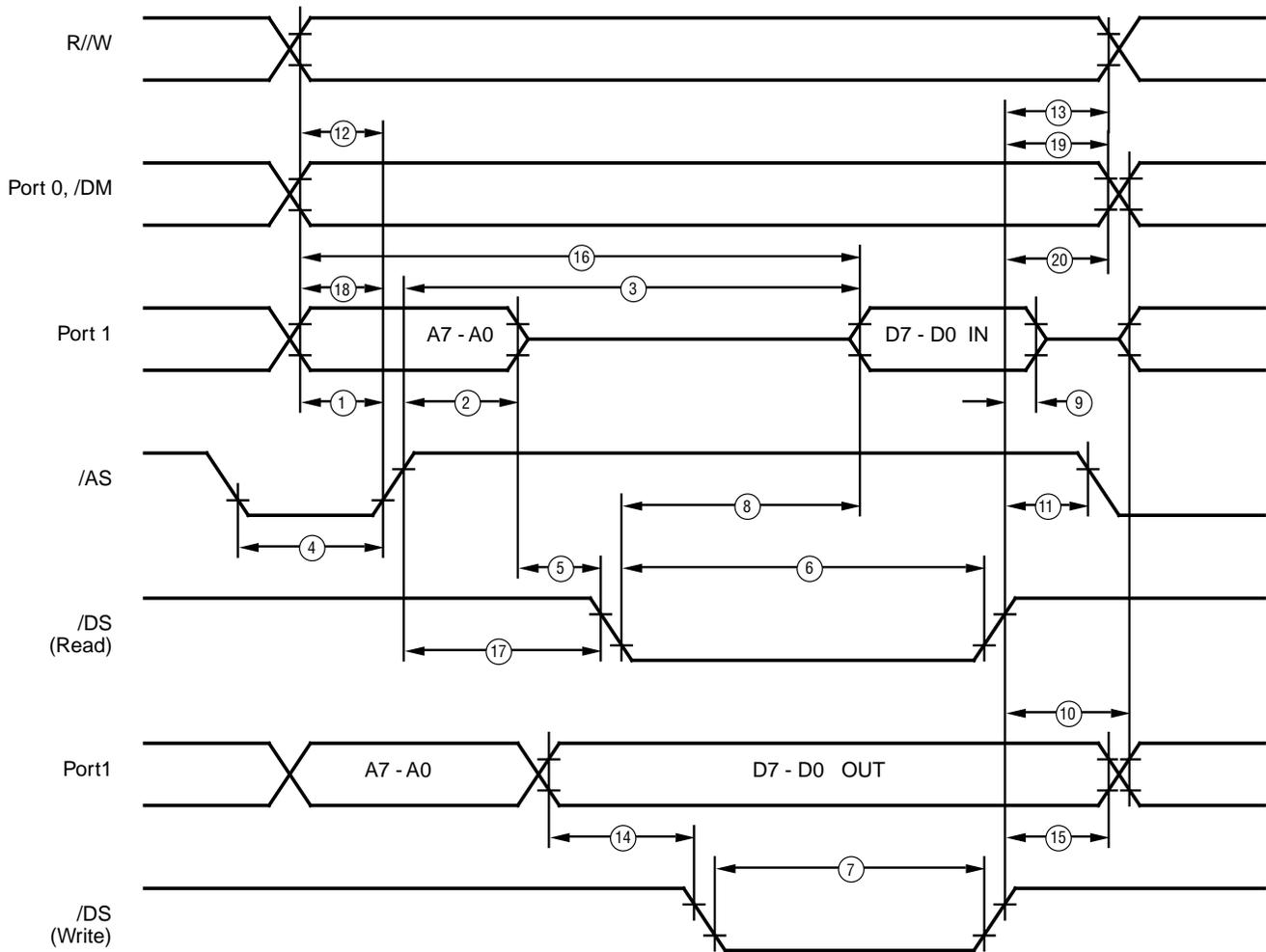
Sym	Parameter	V _{CC} Note [3]	T _A = 0° C to +70° C		Typical [13] @ 25° C	Units	Conditions	Notes
			Min	Max				
V ^{ICR}	Input Common Mode	2.0V	0	V _{CC} -1.0V		V		[10]
	Voltage Range	3.9V	0	V _{CC} -1.0V		V		[10]
I _{ALL}	Auto Latch Low Current	2.0V	0.7	8	2.4	μA	0V < V _{IN} < V _{CC}	[9]
		3.9V	1.4	15	4.7	μA	0V < V _{IN} < V _{CC}	[9]
I _{ALH}	Auto Latch High Current	2.0V	-0.6	-5	-1.8	μA	0V < V _{IN} < V _{CC}	[9]
		3.9V	-1.0	-8	-3.8	μA	0V < V _{IN} < V _{CC}	[9]
V _{LV}	V _{CC} Low Voltage Protection Voltage		1.4	2.15		V	2 MHz max Int. CLK Freq.	[7]
V _{OH}	Output High Voltage (Low EMI Mode)	2.0V	V _{CC} -0.4		3.1	V	I _{OH} = -0.5 mA	
		3.9V	V _{CC} -0.4		4.8	V	I _{OH} = -0.5 mA	
V _{OL}	Output Low Voltage (Low EMI Mode)	2.0V		0.6	0.2	V	I _{OL} = 1.0 mA	
		3.9V		0.4	0.1	V	I _{OL} = 1.0 mA	

Notes:

- | | | | | | |
|-----|----------------------|--------|-----|------|-----------|
| [1] | I _{CC1} | Typ | Max | Unit | Freq |
| | Clock-Driven | 0.3 mA | 5 | mA | 8 MHz |
| | Resonator or Crystal | 3.0 mA | 5 | mA | 8 MHz [5] |
- [2] GND = 0V.
[3] V_{CC} = 2.0V to 3.9V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 10 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{LV} voltage increases as the temperature decreases and will overlap lower V_{CC} operating region.
[8] Standard Mode (not Low EMI).
[9] Auto Latch (Mask Option) selected.
[10] For analog comparator, inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
[12] Excludes clock pins.
[13] Typicals are at V_{CC} = 3.0V.
[14] Internal RC selected.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram (C43 Only)



External I/O or Memory Read/Write Timing
(Z86L43 Only)

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (L43 Only)
(SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	T _A = -0°C to 70°C		Units	Notes
			Note [3] V _{CC}	8 MHz Min Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	2.0	35	ns	[2]
			3.9	35		
2	TdAS(A)	/AS Rise to Address Float Delay	2.0	45	ns	[2]
			3.9	45		
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	2.0	250	ns	[1,2]
			3.9	250		
4	TwAS	/AS Low Width	2.0	55	ns	[2]
			3.9	55		
5	TdAS(DS)	Address Float to /DS Fall	2.0	0	ns	
			3.9	0		
6	TwDSR	/DS (Read) Low Width	2.0	200	ns	[1,2]
			3.9	200		
7	TwDSW	/DS (Write) Low Width	2.0	110	ns	[1,2]
			3.9	110		
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	2.0	150	ns	[1,2]
			3.9	150		
9	ThDR(DS)	Read Data to /DS Rise Hold Time	2.0	0	ns	[2]
			3.9	0		
10	TdDS(A)	/DS Rise to Address Active Delay	2.0	45	ns	[2]
			3.9	55		
11	TdDS(AS)	/DS Rise to /AS Fall Delay	2.0	30	ns	[2]
			3.9	45		
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	2.0	45	ns	[2]
			3.9	45		
13	TdDS(R/W)	/DS Rise to R/W Not Valid	2.0	45	ns	[2]
			3.9	45		
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	2.0	55	ns	[2]
			3.9	55		
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	2.0	45	ns	[2]
			3.9	45		
16	TdA(DR)	Address Valid to Read Data Req'd Valid	2.0	310	ns	[1,2]
			3.9	310		
17	TdAS(DS)	/AS Rise to /DS Fall Delay	2.0	65	ns	[2]
			3.9	65		
18	TdDM(AS)	/DM Valid to /AS Rise Delay	2.0	35	ns	[2]
			3.9	35		
19	TdDS(DM)	/DS Rise to DM Valid Delay		45	ns	
				45		
20	ThDS(AS)	/DS Valid to Address Valid Hold Time		45	ns	
				45		

Notes:

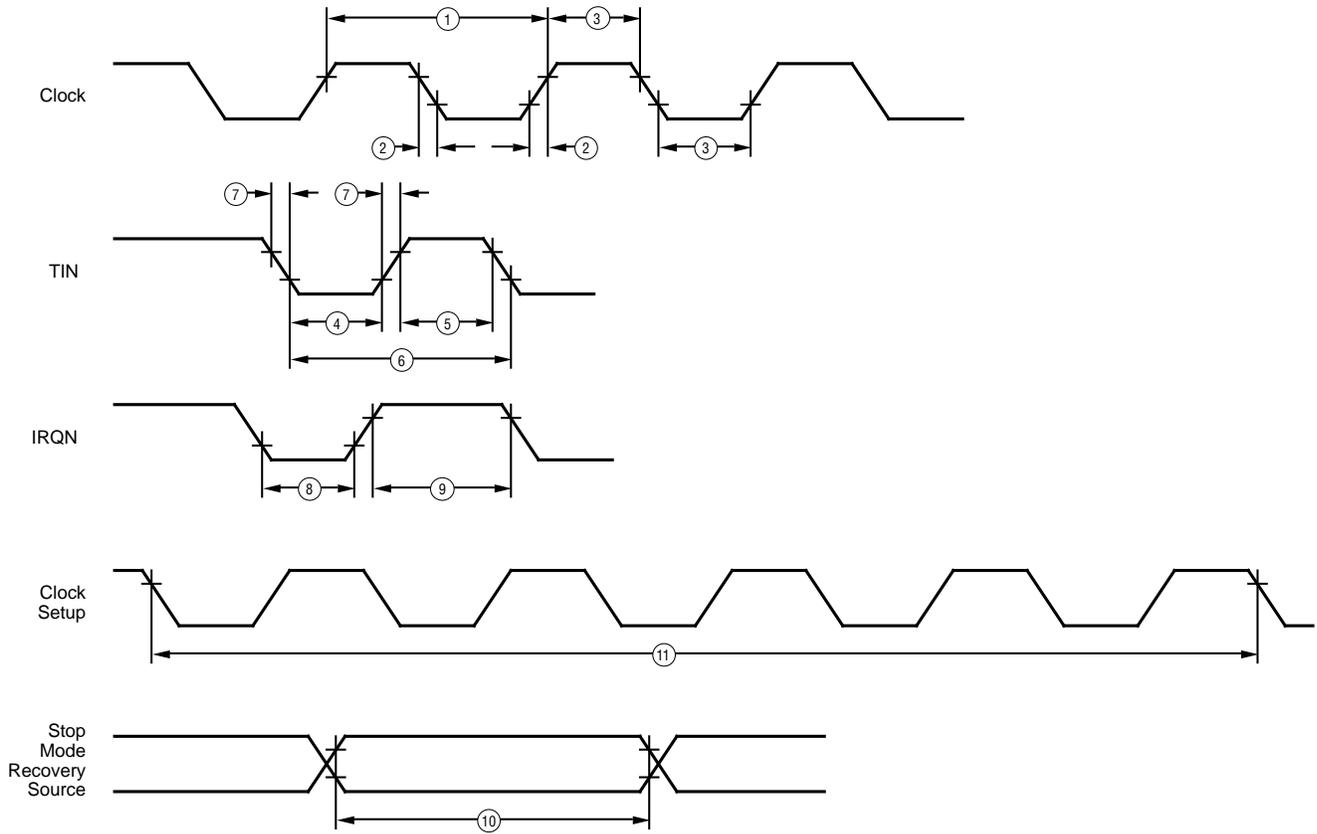
- [1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] V_{CC} = 2.0V to 3.9V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Units	Notes
			V_{CC} Note [6]	8 MHz Min Max		
1	TpC	Input Clock Period	2.0V	83	DC	ns [1]
			3.9V	83	DC	ns [1]
2	TrC,TfC	Clock Input Rise & Fall Times	2.0V		15	ns [1]
			3.9V		15	ns [1]
3	TwC	Input Clock Width	2.0V	41		ns [1]
			3.9V	41		ns [1]
4	TwTinL	Timer Input Low Width	2.0V	100		ns [1]
			3.9V	70		ns [1]
5	TwTinH	Timer Input High Width	2.0V	5TpC		[1]
			3.9V	5TpC		[1]
6	TpTin	Timer Input Period	2.0V	8TpC		[1]
			3.9V	8TpC		[1]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	2.0V		100	ns [1]
			3.9V		100	ns [1]
8A	TwlL	Int. Request Low Time	2.0V	100		ns [1,2]
			3.9V	70		ns [1,2]
8B	TwlL	Int. Request Low Time	2.0V	5TpC		[1,3]
			3.9V	5TpC		[1,3]
9	TwhH	Int. Request Input High Time	2.0V	5TpC		[1,2]
			3.9V	5TpC		[1,2]
10	TwsM	STOP Mode Recovery Width Spec	2.0V	12		ns
			3.9V	12		ns
11	Tost	Oscillator Startup Time	2.0V		5TpC	[4]
			3.9V		5TpC	[4]
12	Twdt	Watch-Dog Timer Delay Time (Before Refresh is Necessary)	2.0V	7		D1, D0 ms 0, 0 [5]
			3.9V	3.5		ms 0, 0 [5]
			2.0V	14		ms 0, 1 [5]
			3.9V	7		ms 0, 1 [5]
			2.0V	28		ms 1, 0 [5]
			3.9V	14		ms 1, 0 [5]
			2.0V	112		ms 1, 1 [5]
			3.9V	56		ms 1, 1 [5]
13	T _{POR}	Power-On Reset Delay	2.0V		45	ms
			3.9V		25	ms

Notes:

- [1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
- [2] Interrupt request via Port 3 (P31-P33).
- [3] Interrupt request via Port 3 (P30).
- [4] SMR-D5 = 0.
- [5] Reg. WDTMR.
- [6] V_{CC} = 2.0V to 3.9V.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

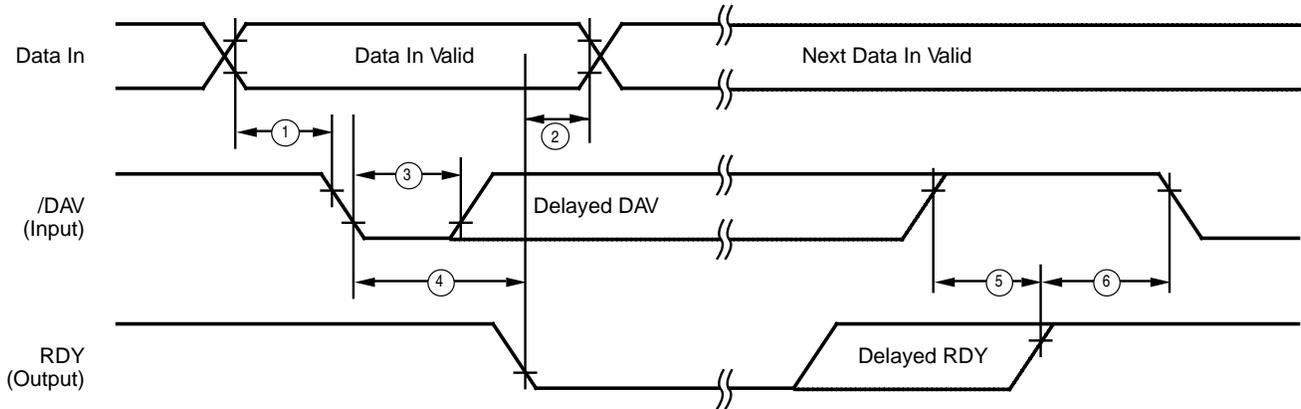
No	Symbol	Parameter	V _{CC} Note [6]	T _A = 0°C to +70°C		Units	Notes
				4 MHz Min	Max		
1	TpC	Input Clock Period	2.0V	250	DC	ns	[1,7,8]
			3.9V	250	DC		
2	TrC,TfC	Clock Input Rise & Fall Times	2.0V		25	ns	[1,7,8]
			3.9V		25		
3	TwC	Input Clock Width	2.0V	125		ns	[1,7,8]
			3.9V	125			
4	TwTinL	Timer Input Low Width	2.0V	100		ns	[1,7,8]
			3.9V	70			
5	TwTinH	Timer Input High Width	2.0V	3TpC			[1,7,8]
			3.9V	3TpC			
6	TpTin	Timer Input Period	2.0V	4TpC			[1,7,8]
			3.9V	4TpC			
7	TrTin, TfTin	Timer Input Rise & Fall Timer	2.0V		100	ns	[1,7,8]
			3.9V		100		
8A	TwIL	Int. Request Low Time	2.0V	100		ns	[1,2,7,8]
			3.9V	70			
8B	TwL	Int. Request Low Time	2.0V	3TpC			[1,3,7,8]
			3.9V	3TpC			
9	TwH	Int. Request Input High Time	2.0V	3TpC			[1,2,7,8]
			3.9V	3TpC			
10	TwsM	STOP Mode Recovery Width Spec	2.0V	12		ns	[4,8]
			3.9V	12			
11	Tost	Oscillator Startup Time	2.0V		5TpC		[4,8,9]
			3.9V		5TpC		

Notes:

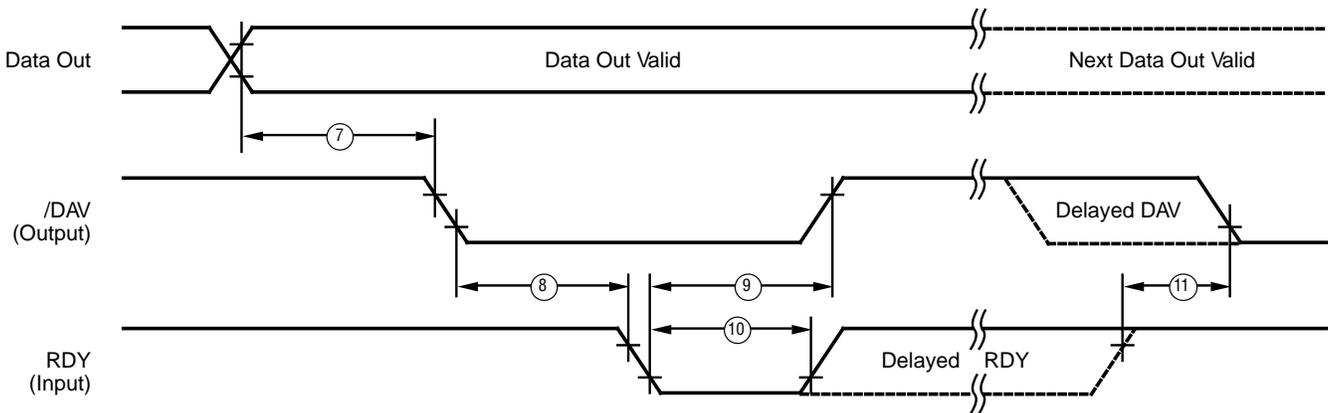
- [1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
- [2] Interrupt request via Port 3 (P31-P33).
- [3] Interrupt request via Port 3 (P30).
- [4] SMR-D5 = 1, POR STOP Mode Delay is on.
- [5] Reg. WDTMR.
- [6] V_{CC} = 2.0V to 3.9V.
- [7] SMR D1 = 0.
- [8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
- [9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Direction Data
			V_{CC} Note [1]	8 MHz Min Max	
1	TsDI(DAV)	Data In Setup Time	2.0V	0	IN
			3.9V	0	IN
2	ThDI(RDY)	Data In Hold Time	2.0V	0	IN
			3.9V	0	IN
3	TwDAV	Data Available Width	2.0V	155	IN
			3.9V	110	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	2.0V	0	IN
			3.9V	0	IN
5	TdDAVI(dRDY)	DAV Out to DAV Fall Delay	2.0V	120	IN
			3.9V	80	IN
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	2.0V	0	IN
			3.9V	0	IN
7	TdDO(DAV)	Data Out to DAV Fall Delay	2.0V	63	OUT
			3.9V	63	OUT
8	TdDAVO(RDY)	DAV Fall to RDY Fall Delay	2.0V	0	OUT
			3.9V	0	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	2.0V	160	OUT
			3.9V	115	OUT
10	TwRDY	RDY Width	2.0V	110	OUT
			3.9V	80	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	2.0V	110	OUT
			3.9V	80	OUT

Notes:

[1] Timing Reference uses $0.7 V_{CC}$ for a logic 1 and $0.2 V_{CC}$ for a logic 0.

[2] $V_{CC} = 2.0\text{V to } 3.9\text{V}$.

© 1996 by Zilog, Inc. All rights reserved. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Zilog, Inc. The information in this document is subject to change without notice. Devices sold by Zilog, Inc. are covered by warranty and patent indemnification provisions appearing in Zilog, Inc. Terms and Conditions of Sale only. Zilog, Inc. makes no warranty, express, statutory, implied or by description, regarding the information set forth herein or regarding the freedom of the described devices from intellectual property infringement. Zilog, Inc. makes no warranty of merchantability or fitness for any purpose. Zilog, Inc. shall not be responsible for any errors that may appear in this document. Zilog, Inc. makes no commitment to update or keep current the information contained in this document.

Zilog's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the customer and Zilog prior to use. Life support devices or systems are those which are intended for surgical implantation into the body, or which sustains life whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

Zilog, Inc. 210 East Hacienda Ave.
 Campbell, CA 95008-6600
 Telephone (408) 370-8000
 FAX 408 370-8056
 Internet: <http://www.zilog.com>