DUAL POLARISATION SWITCH TWIN LNB MULTIPLEX CONTROLLER

ZLNB100

ISSUE 1- NOVEMBER 1998

DEVICE DESCRIPTION

The ZLNB101 dual polarisation switch controller is one of a wide range of satellite receiver LNB support circuits. It features two completely independent channels, each providing two logic outputs under the control of a voltage sensitive input. It is intended for use in Twin LNB designs, replacing many dlscrete components to save both manufacturing cost and PCB size whilst improving reliability.

The two inputs of the ZLNB101 have a nominal threshold of 14.5V. Their threshold is temperature compensated to minimise drift. Each features a low and stable input current that enables transient protection to be achieved with the addition of only a single resistor per channel.

Normal and an inverted outputs are provided for each input. All outputs can source 15mA and sink 10mA making them suitable to drive TTL and CMOS logic, pin diodes and for IF-amp supply switching.

The ZLNB101 operates from a single supply of between 5-12V. Its quiescent current is typically only 4mA and this does not change significantly with load or logic state. It is available in either the standard SO8 or space saving MSOP8 surface mount packages. Device operating temperature is -40°C to +85°C to suit a wide range of environmental conditions.

FEATURES

- provides polarity detection and control
- transient resistant
- low input current
- low supply current
- temperature compensated input threshold
- standard and inverted output available simultaneously wide supply operating range
- dual polarisation switch
- eliminates external components
- simplifies design

APPLICATIONS

- twin LNBs
- IF switch box
- LNB switch boxes

ZLNB100

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.6V to 15V
Supply Current	50mA
V_{POL1} and V_{POL2} Input Voltage	25V Continuous
Operating Temperature	-40 to 85°C
Storage Temperature	-40 to 85°

Power Dissipation (T_{amb}= 25°C)

SO8	500mW
MSOP8	500mW

ELECTRICAL CHARACTERISTICS TEST CONDITIONS (Unless otherwise stated): T_{amb}= 25°C, V_{CC}=5V, I_D=10mA (R_{CAL1}=33kΩ)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{CC}	Supply Voltage		5		12	V
I_{CC}	Supply Current	All inputs and outputs open circuit			10	mA
		I_{VERT1} = I_{VERT2} = 10mA, V_{POL1} = V_{POL2} = 14V			30	mA
		I_{HOR1} = I_{HOR2} = 10mA, V_{POL1} = V_{POL2} = 15.0V			30	mA
	V_{POL1} and V_{POL2} Inputs					
I_{POL}	Current	V_{POL1} = V_{POL2} = 25V (Note 4)	10	20	40	µA
V_{TPOL}	Threshold Voltage	(Note 1) (Note 4)	14.0	14.5	15.0	
T_{SPOL}	Switching Speed				100	µs
	Vert 1/2 Outputs					
V_{VHIGH}	Voltage High	I_{VERT1}=I_{VERT2}=10mA, V_{POL1} = V_{POL2} = 14V	V_{CC}-1.0	V_{CC}-0.8	V_{CC}	V
V_{VHIGH}	Voltage High	I_{VERT1}=I_{VERT2}=15mA, V_{POL1} = V_{POL2} = 14V	V_{CC}-1.2	V_{CC}-0.9	V_{CC}	V
V_{VHIGH}	Voltage High	I_{VERT1}=I_{VERT2}=10µA, V_{POL1} = V_{POL2} = 14V	V_{CC}-0.2	V_{CC}-0.1	V_{CC}	V
V_{VLOW}	Voltage Low	I_{VERT1}=I_{VERT2}=-10mA, V_{POL1} = V_{POL2} = 15.0V	0	0.25	0.5	V
	Hor 1/2 Outputs					
V_{VHIGH}	Voltage High	I_{HOR1}=I_{HOR2}=10mA, V_{POL1} = V_{POL2} = 15.0V	V_{CC}-1.0	V_{CC}-0.8	V_{CC}	V
V_{VHIGH}	Voltage High	I_{HOR1}=I_{HOR2}=15mA, V_{POL1} = V_{POL2} = 15.0V	V_{CC}-1.2	V_{CC}-0.9	V_{CC}	V
V_{VHIGH}	Voltage High	I_{HOR1}=I_{HOR2}=10µA, V_{POL1} = V_{POL2} = 15.0V	V_{CC}-0.2	V_{CC}-0.1	V_{CC}	V
V_{VLOW}	Voltage Low	I_{HOR1}=I_{HOR2}=-10mA, V_{POL1} = V_{POL2} = 14V	0	0.25	0.5	V

Note:-

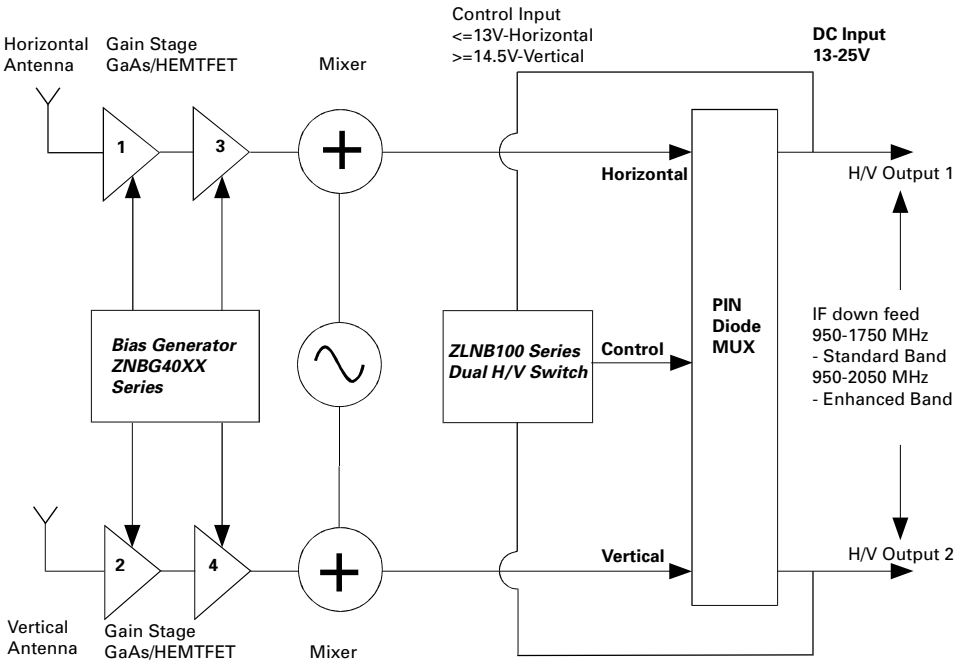
1) V_{POL1} and V_{POL2} switching thresholds apply over the whole operating temperature range specified above.

2) Inputs V_{POL1} and V_{POL2} are designed to be wired to the power input of an LNB via high value (10k) resistors. Input V_{POL1} controls outputs Vert1 and Hor1. Input V_{POL2} controls outputs Vert2 and Hor2. With either input voltage set at or below 14V, the corresponding Vert pin will be high and Hor pin low. With either input voltage at or above 15.0V, the corresponding Vert pin will be low and Hor pin high. Any input or output not required may be left open-circuit.

3) All outputs are designed to be compatible with TTL, CMOS, pin diode and IF Amp loads.

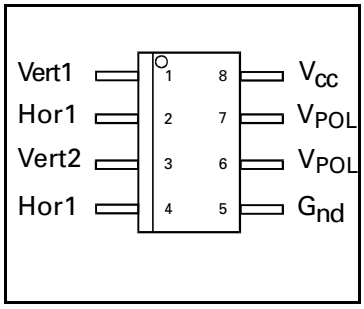
4) Applied via 10k resistors

The following block diagram shows a typical block diagram twin LNB design. The ZLNB100 provides the two polarity switches required to decode the two independent receiver feeds. Additionally the front end bias requirements of the LNB are provided by the ZNBG4000 or ZNBG6000 offering a very efficient and cost effective solution.



ZLNB100

CONNECTION DIAGRAMS



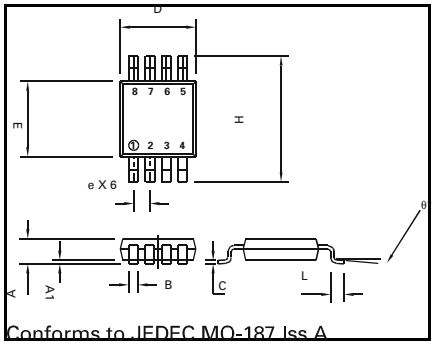
ORDERING INFORMATION

Part Number	Package	Part Mark
ZLNB100X	MSOP8	ZLNB100
ZLNB100N8	SO8	ZLNB100

PACKAGE DIMENSIONS

MSOP8

DIM	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A	0.91	1.11	0.036	0.044
A1	0.10	0.20	0.004	0.008
B	0.25	0.36	0.010	0.014
C	0.13	0.18	0.005	0.007
D	2.95	3.05	0.116	0.120
e	0.65	NOM	0.0256	NOM
e1	0.33	NOM	0.0128	NOM
E	2.95	3.05	0.116	0.120
H	4.78	5.03	0.188	0.198
L	0.41	0.66	0.016	0.026
θ°	0°	6°	0°	6°



Conforms to JEDEC MO-187 Iss A

SO8

DIM	Millimetres		Inches	
	Min	Max	Min	Max
A	4.80	4.98	0.189	0.196
B	1.27 BSC		0.05 BSC	
C	0.53 REF		0.02 REF	
D	0.36	0.46	0.014	0.018
E	3.81	3.99	0.15	0.157
F	1.35	1.75	0.05	0.07
G	0.10	0.25	0.004	0.010
J	5.80	6.20	0.23	0.24
K	0°	8°	0°	8°
L	0.41	1.27	0.016	0.050