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GEC PLESSEY SEMICONDUCTORS

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MAY 1994

DS3008-2.0

ZN429E8/ZN429D

LOW COST 8-BIT D-A CONVERTER

The ZN429 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

FEATURES

- Linearity Error $\pm^1/_2$ LSB
- Single +5V Supply
- Low Power Consumption 25mW Typical
- Settling Time 1 Microsecond Typical
- TTL and 5V CMOS Compatible
- Designed for Low Cost Applications

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	+5.5V
Storage temperature range	-55°C to +125°C

ORDERING INFORMATION

Ambient operating temperature	-40°C to +85°C
Package, ZN429D	MP14
Package, ZN429E8	DP14

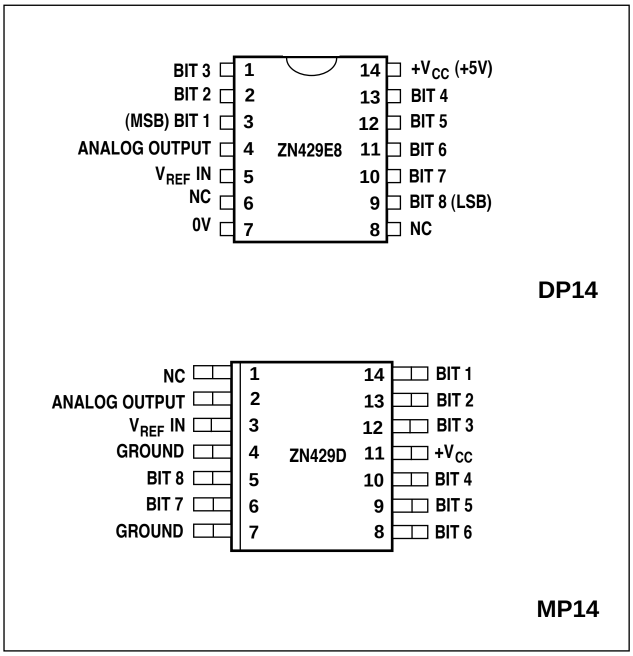
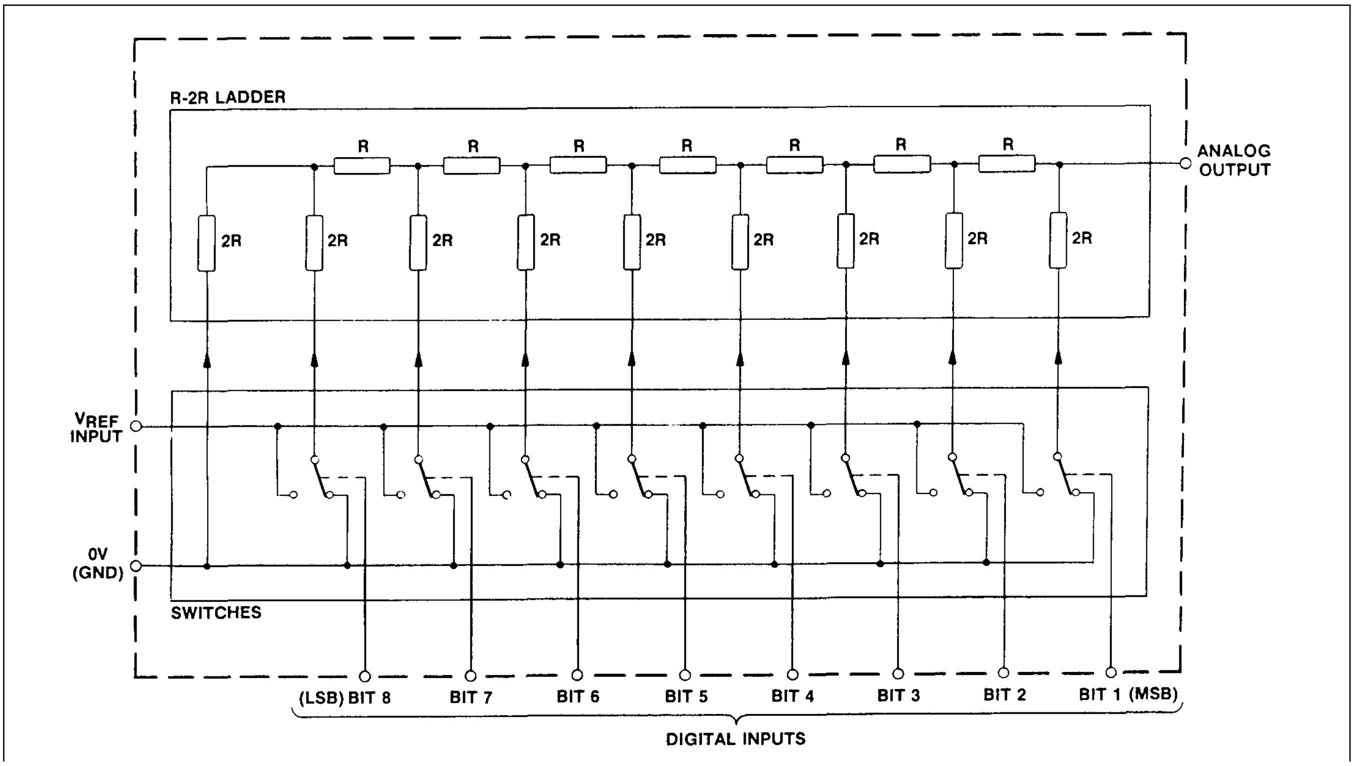


Fig.1 Pin connections (not to scale) - top view



ELECTRICAL CHARACTERISTICS

(at T_{amb} = 25°C and V_{CC} = +5V unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	-	-	bits	
Accuracy		8	-	-	bits	
Non-linearity		-	-	±0.5	LSB	
Differential non-linearity		-	±0.5	-	LSB	Note 1
Settling time to 0.5LSB		-	1.0	-	µs	1 LSB step
Settling time to 0.5LSB		-	2.0	-	µs	All bits ON to OFF or OFF to ON
Offset voltage ZN429E8, ZN429D	V_{OS}	-	3.0	5.0	mV	All bits OFF
V_{OS} temperature coefficient		-	5	-	µV/°C	
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. V_{REF} = 2.56V
Full-scale temp. coefficient		-	3	-	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coefficient		-	7.5	-	ppm/°C	Relative to F.S.R.
Analog output resistance	R_O	-	10	-	kΩ	
External reference voltage		0	-	3.0	V	
Supply voltage	V_{CC}	4.5	-	5.5	V	
Supply current	I_S	-	5	9	mA	
High level input voltage	V_{IH}	2.0	-	-	V	
Low level input voltage	V_{IL}	-	-	0.7	V	
High level input current	I_{IH}	-	-	10	µA	V_{CC} = max. V_I = 2.4V
		-	-	100	µA	V_{CC} = max. V_I = 5.5V
Low level input current	I_{IL}	-	-	-0.18	mA	V_{CC} = max. V_I = 0.3V

NOTE 1: Monotonic over full temperature range.

INTRODUCTION

The ZN429 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of the ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig.3.

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2Ω.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

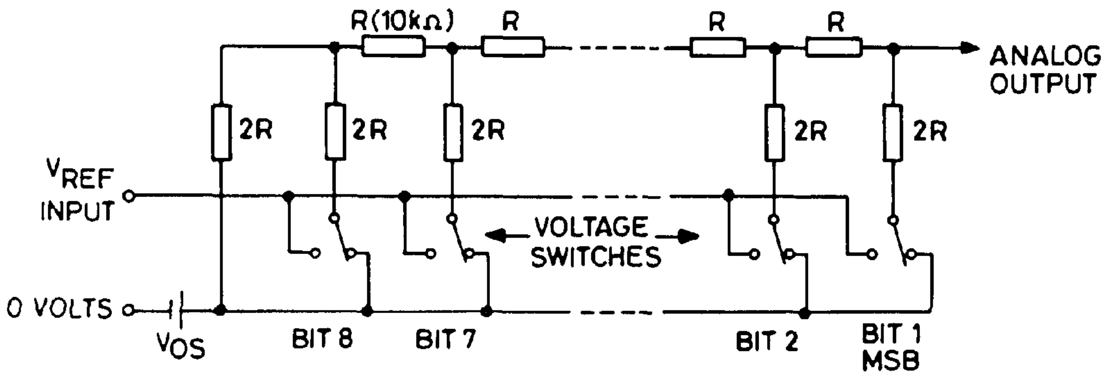


Fig.3 The R-2R ladder network

APPLICATIONS

(1) Unipolar D-A Converter

The nominal output range of the ZN429 is 0 to $V_{REF\ IN}$ through a 10Ω resistance. Other output ranges can readily be obtained by using an external amplifier.

The resulting full-scale range is given by

$$V_{OUT\ FS} = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (10kΩ). The required nominal values of R1 and R2 are given by

R1 = 10GkΩ and R_2 = 10G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5V.

Output Range	G	R_1	R_2
+5V	2	20kΩ	20kΩ
+10V	4	40kΩ	13.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig.5. Settling time for a major transition is 2.5µs typical.

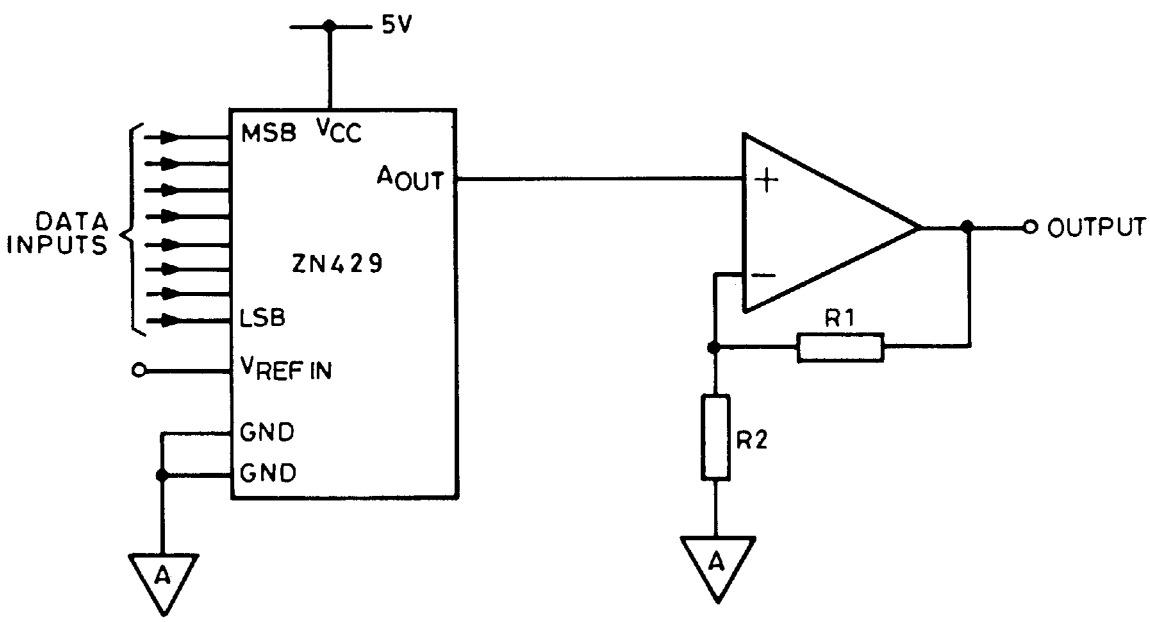


Fig.4 Unipolar operation - basic circuit

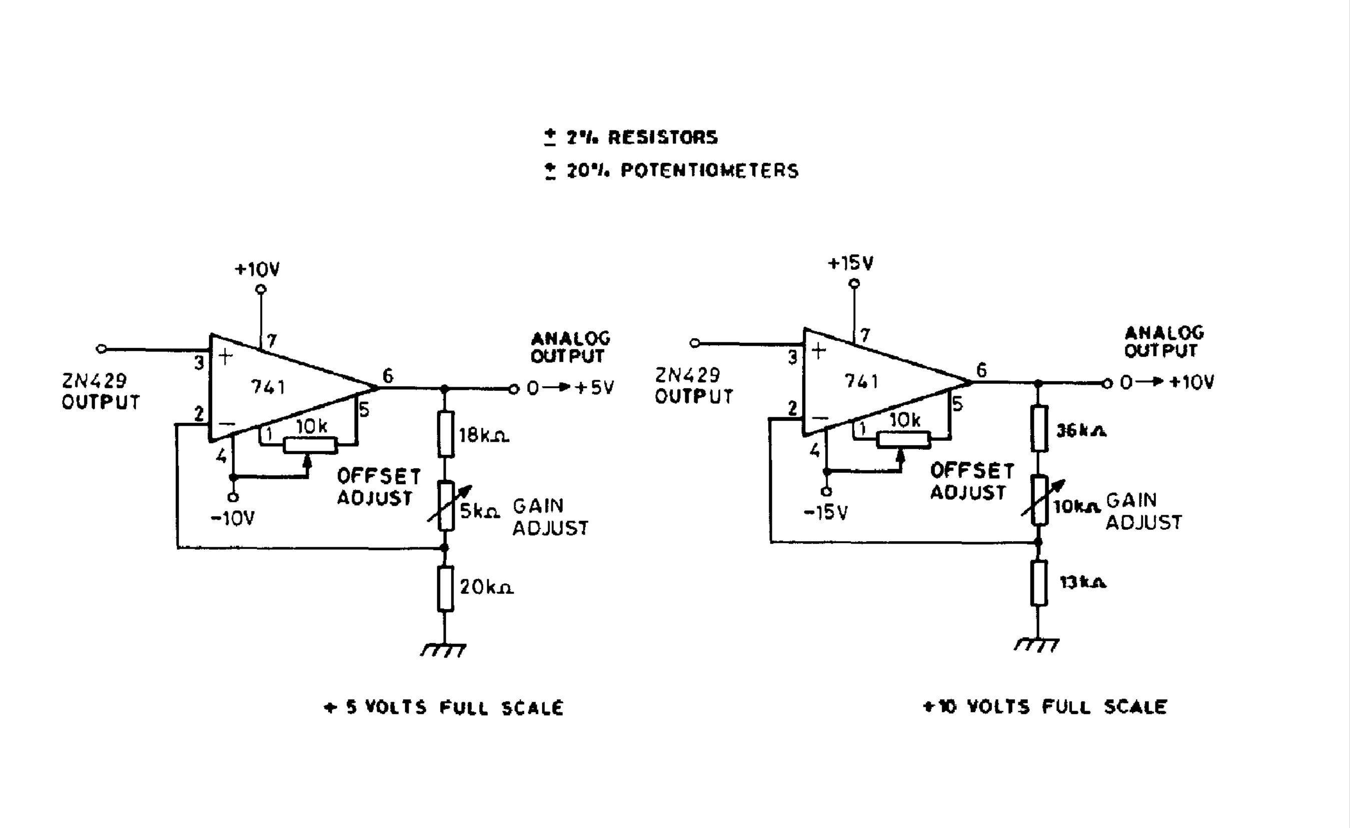


Fig.5 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust zero until V_{OUT} = 0.0000V.

(ii) Set all bits ON (HIGH) and adjust gain until V_{OUT} = FS - 1LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS - 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1mV	9.9609V

$1LSB = \frac{FS}{256}$

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analog Output (Nominal Value)
11111111	FS - 1LSB
11111110	FS - 2 LSB
11000000	$^3/_4$ FS
10000001	$^1/_2$ FS + 1LSB
10000000	$^1/_2$ FS
01111111	$^1/_2$ FS - 1LSB
01000000	$^1/_4$ FS
00000001	1LSB
00000000	0

(2) Bipolar D-A Converter

For bipolar operation the output from the ZN429 is offset by half full-scale by connecting a resistor R3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig.6).

When the digital input of the ZN429 is zero the analog output is zero and the amplifier output should be -full-scale. An input of all ones to the D-A will give a ZN429 output of ≙ $V_{REF\ IN}$ and the amplifier output required is +full-scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 10kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

R1 = 20GkΩ, R2 = 20G/(G-1)kΩ and R3 = 20kΩ.

where the resultant output range is $\pm G.V_{REF\ IN}$.

Assuming that $V_{REF\ IN}$ = 2.5V the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
±5V	2	40kΩ	40kΩ	20kΩ
±10V	4	80kΩ	26.67kΩ	20kΩ

Minus full scale (0FFSET) is set by adjusting R1 about its nominal value relative to R3. Plus full-scale (GAIN) is set by adjusting R2 relative to R1.

Settling time for a major transistion is 2.5µs typical.

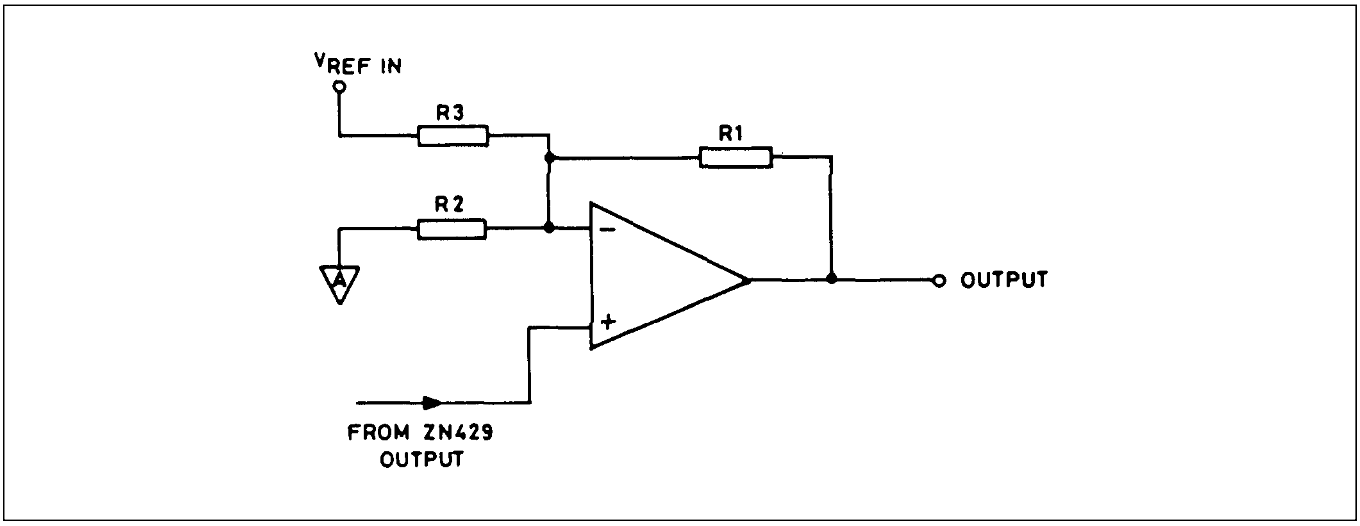


Fig.6 Bipolar operation - basic circuit

BIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust OFFSETuntil the amplifier output reads -FULL-SCALE.

(ii) Set all bits ON (HIGH) and adjust gain until the amplifier reads +(FULL-SCALE - 1LSB).

BIPOLAR SETTING UP POINTS

Input Range, ± FS	LSB	-FS	+(FS - 1LSB)
±5V	39.1 mV	-5.0000V	+4.9609V
±10V	78.1mV	-10.0000V	9.9219V

$1LSB = \frac{2FS}{256}$

BIPOLAR LOGIC CODING

Input Code (Offset Binary)	Analog Output (Nominal Value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2 LSB)
11000000	$+^1/_2$ FS
10000001	+ 1LSB
10000000	0
01111111	-1 LSB
01000000	$-^1/_2$ FS
00000001	-(FS - 1LSB)
00000000	-FS

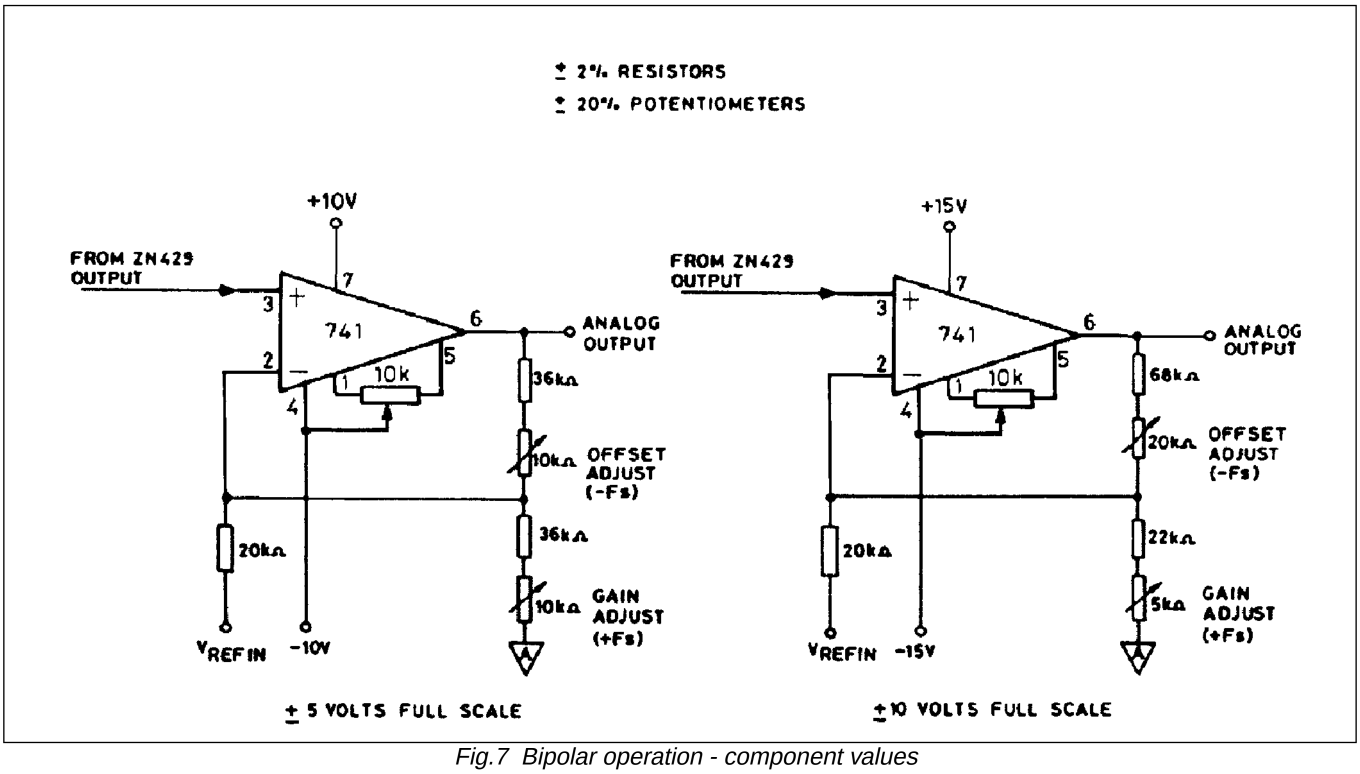


Fig.7 Bipolar operation - component values

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