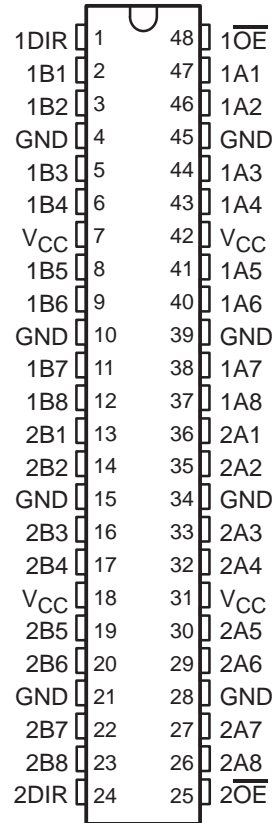


SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

- **Members of the Texas Instruments Widebus™ Family**
- **A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVTH162245 . . . WD PACKAGE
SN74LVTH162245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'LVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-----------------------|------------------|---------------|-----------------------|-------------------|
| –40°C to 85°C | SSOP – DL | Tube | SN74LVTH162245DL | LVTH162245 |
| | | Tape and reel | SN74LVTH162245DLR | |
| | TSSOP – DGG | Tape and reel | SN74LVTH162245DGGR | LVTH162245 |
| | VFBGA – GQL | Tape and reel | SN74LVTH162245KR | LL2245 |
| VFBGA – ZQL (Pb-free) | 74LVTH162245ZQLR | | | |
| –55°C to 125°C | CFP – WD | Tube | SNJ54LVTH162245WD | SNJ54LVTH162245WD |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS260O – JUNE 1993 – REVISED SEPTEMBER 2003

description/ordering information (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

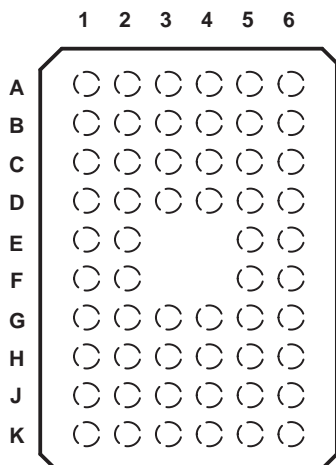
The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------|-----|----------|----------|-----|------------------|
| A | 1DIR | NC | NC | NC | NC | $\overline{1OE}$ |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | V_{CC} | V_{CC} | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | V_{CC} | V_{CC} | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | $\overline{2OE}$ |

NC – No internal connection

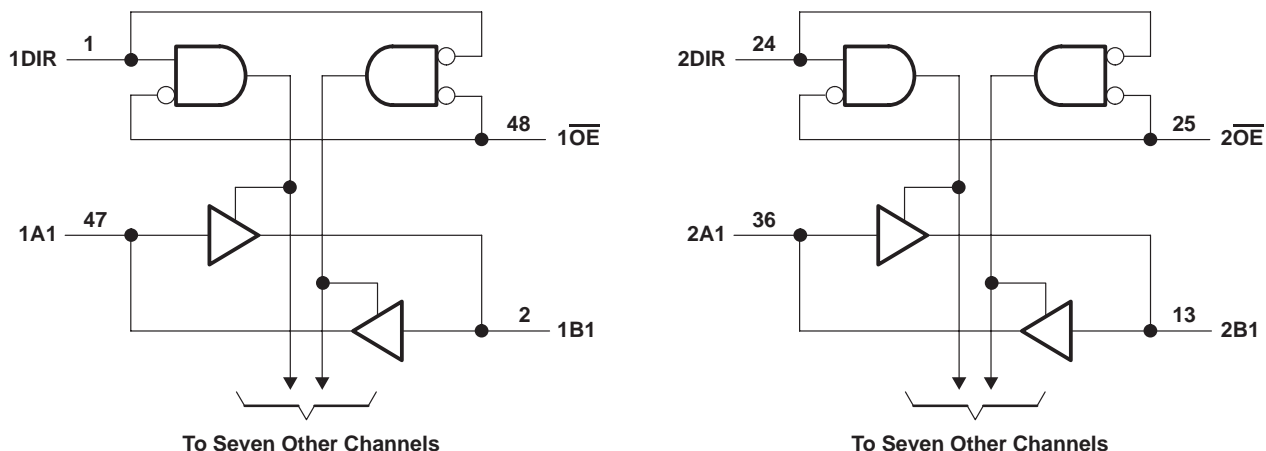
FUNCTION TABLE (each 8-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_{OL} : SN54LVTH162245 (B port) | 96 mA |
| SN74LVTH162245 (B port) | 128 mA |
| A port | 30 mA |
| Current into any output in the high state, I_{OH} (see Note 2): SN54LVTH162245 (B port) | 48 mA |
| SN74LVTH162245 (B port) | 64 mA |
| A port | 30 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DGG package | 70°C/W |
| DL package | 63°C/W |
| GQL/ZQL package | 42°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54LVTH162245, SN74LVTH162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

recommended operating conditions (see Note 4)

| | | SN54LVTH162245 | | SN74LVTH162245 | | UNIT |
|---------------------|------------------------------------|-----------------|-----|----------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | | 5.5 | | 5.5 | V |
| I _{OH} | High-level output current | A port | | -12 | | mA |
| | | B port | | -32 | | |
| I _{OL} | Low-level output current | A port | | 12 | | mA |
| | | B port | | 64 | | |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | | ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN54LVTH162245 | | | SN74LVTH162245 | | | UNIT | |
|--------------------------|--|--|----------------------------------|------|------|----------------------|------|-----|------|----|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | | |
| V _{IK} | | V _{CC} = 2.7 V, I _I = -18 mA | -1.2 | | | -1.2 | | | V | |
| V _{OH} | A port | V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA | V _{CC} -0.2 | | | V _{CC} -0.2 | | | V | |
| | | V _{CC} = 3 V, I _{OH} = -12 mA | 2 | | | 2 | | | | |
| | B port | V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA | V _{CC} -0.2 | | | V _{CC} -0.2 | | | | |
| | | V _{CC} = 2.7 V, I _{OH} = -8 mA | 2.4 | | | 2.4 | | | | |
| | | V _{CC} = 3 V | I _{OH} = -24 mA | 2 | | | | | | |
| I _{OH} = -32 mA | | | | 2 | | | | | | |
| V _{OL} | A port | V _{CC} = 2.7 V to 3.6 V, I _{OL} = 100 μA | 0.2 | | | 0.2 | | | V | |
| | | V _{CC} = 3 V, I _{OL} = 12 mA | 0.8 | | | 0.8 | | | | |
| | B port | V _{CC} = 2.7 V | I _{OL} = 100 μA | 0.2 | | | 0.2 | | | |
| | | | I _{OL} = 24 mA | 0.5 | | | 0.5 | | | |
| | | V _{CC} = 3 V | I _{OL} = 16 mA | 0.4 | | | 0.4 | | | |
| | | | I _{OL} = 32 mA | 0.5 | | | 0.5 | | | |
| | | | I _{OL} = 48 mA | 0.55 | | | | | | |
| I _{OL} = 64 mA | | | | 0.55 | | | | | | |
| I _I | Control inputs | V _{CC} = 3.6 V, V _I = V _{CC} or GND | ±1 | | | ±1 | | | μA | |
| | | V _{CC} = 0 or 3.6 V, V _I = 5.5 V | 10 | | | 10 | | | | |
| | A or B ports‡ | V _{CC} = 3.6 V | V _I = 5.5 V | 20 | | | 20 | | | |
| | | | V _I = V _{CC} | 5 | | | 5 | | | |
| V _I = 0 | -10 | | | -10 | | | | | | |
| I _{off} | V _{CC} = 0, V _I or V _O = 0 to 4.5 V | | | | ±100 | | | μA | | |
| I _I (hold) | A or B ports | V _{CC} = 3 V | V _I = 0.8 V | 75 | | | 75 | | | μA |
| | | | V _I = 2 V | -75 | | | -75 | | | |
| | | V _{CC} = 3.6 V§, V _I = 0 to 3.6 V | | | | 500 -750 | | | | |
| I _{OZPU} | V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care | ±100* | | | ±100 | | | μA | | |
| I _{OZPD} | V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care | ±100* | | | ±100 | | | μA | | |
| I _{CC} | V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | 0.19 | | | 0.19 | | | mA | |
| | | Outputs low | 5 | | | 5 | | | | |
| | | Outputs disabled | 0.19 | | | 0.19 | | | | |
| ΔI _{CC} ¶ | V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 0.3 | | | 0.2 | | | mA | | |
| C _i | V _I = 3 V or 0 | 4 | | | 4 | | | pF | | |
| C _{io} | V _O = 3 V or 0 | 10 | | | 10 | | | pF | | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused pins at V_{CC} or GND.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



SN54LVTH162245, SN74LVTH162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS2600 – JUNE 1993 – REVISED SEPTEMBER 2003

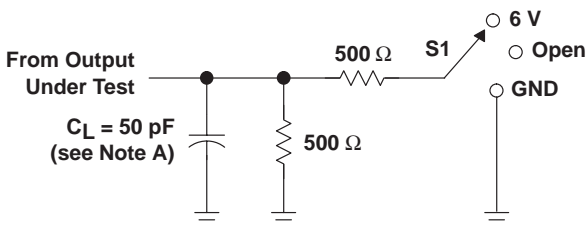
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH162245 | | | | SN74LVTH162245 | | | | UNIT | |
|-------------|-----------------|-------------|--|-----|-------------------------|-----|--|------|-----|-------------------------|------|-----|
| | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | | MAX |
| t_{PLH} | A | B | 1 | 3.5 | 4 | | 1 | 2.3 | 3.3 | 3.7 | | ns |
| t_{PHL} | | | 1 | 3.5 | 3.9 | | 1 | 2.2 | 3.3 | 3.5 | | |
| t_{PLH} | B | A | 1 | 4.3 | 5.3 | | 1 | 2.8 | 4 | 4.6 | | ns |
| t_{PHL} | | | 1 | 4.2 | 4.5 | | 1 | 2.5 | 3.4 | 3.6 | | |
| t_{PZH} | \overline{OE} | B | 1 | 4.8 | 5.9 | | 1 | 2.8 | 4.6 | 5.4 | | ns |
| t_{PZL} | | | 1 | 4.8 | 5.5 | | 1 | 3 | 4.6 | 5.2 | | |
| t_{PZH} | \overline{OE} | A | 1 | 5.5 | 7.2 | | 1 | 3.3 | 5.3 | 6.3 | | ns |
| t_{PZL} | | | 1 | 5.4 | 6.4 | | 1 | 3.3 | 5.1 | 5.8 | | |
| t_{PHZ} | \overline{OE} | B | 1.5 | 5.5 | 5.8 | | 1.5 | 3.8 | 5.2 | 5.5 | | ns |
| t_{PLZ} | | | 1.5 | 5.5 | 5.8 | | 1.5 | 3.5 | 5.1 | 5.4 | | |
| t_{PHZ} | \overline{OE} | A | 1.5 | 5.8 | 6.5 | | 1.5 | 4 | 5.6 | 5.9 | | ns |
| t_{PLZ} | | | 1.2 | 6.3 | 6.3 | | 1.5 | 3.8 | 5.5 | 5.5 | | |
| $t_{sk(o)}$ | | | | | | | | 0.5 | | | ns | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

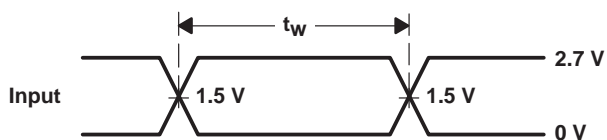


PARAMETER MEASUREMENT INFORMATION

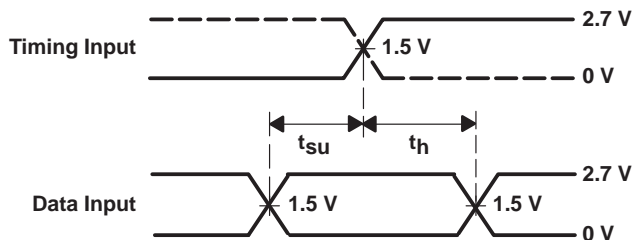


LOAD CIRCUIT

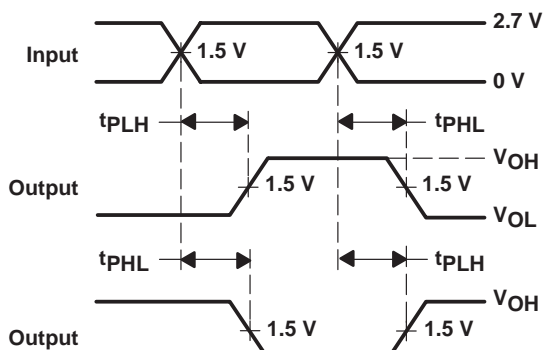
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



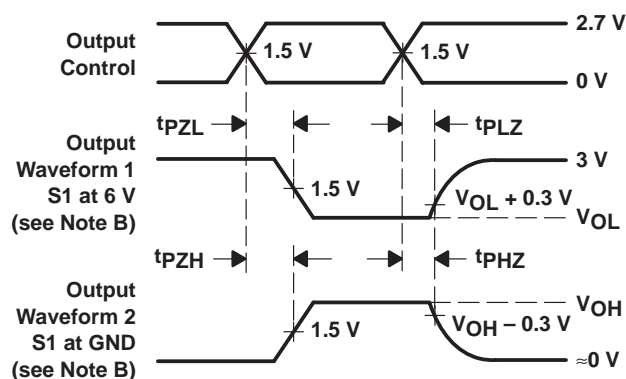
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9678001QXA | ACTIVE | CFP | WD | 48 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 5962-9678001VXA | ACTIVE | CFP | WD | 48 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 74LVTH162245DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH162245DLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH162245GRDR | ACTIVE | LFBGA | GRD | 54 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| 74LVTH162245GRE4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH162245ZQLR | ACTIVE | VFBGA | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| 74LVTH162245ZRDR | ACTIVE | LFBGA | ZRD | 54 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| SN74LVTH162245DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH162245DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH162245DLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH162245DLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH162245KR | ACTIVE | VFBGA | GQL | 56 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| SNJ54LVTH162245WD | ACTIVE | CFP | WD | 48 | 1 | TBD | Call TI | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

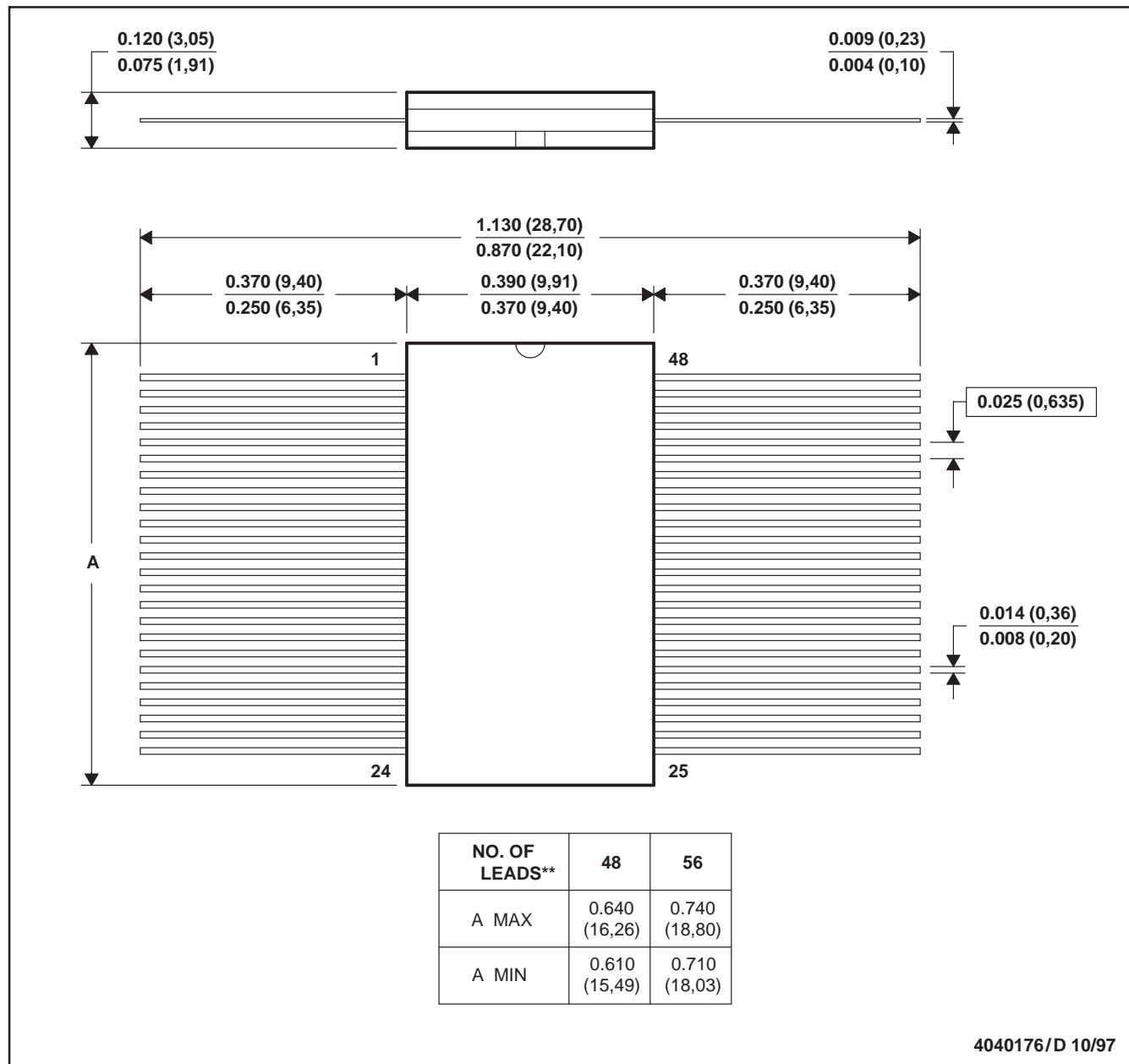
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

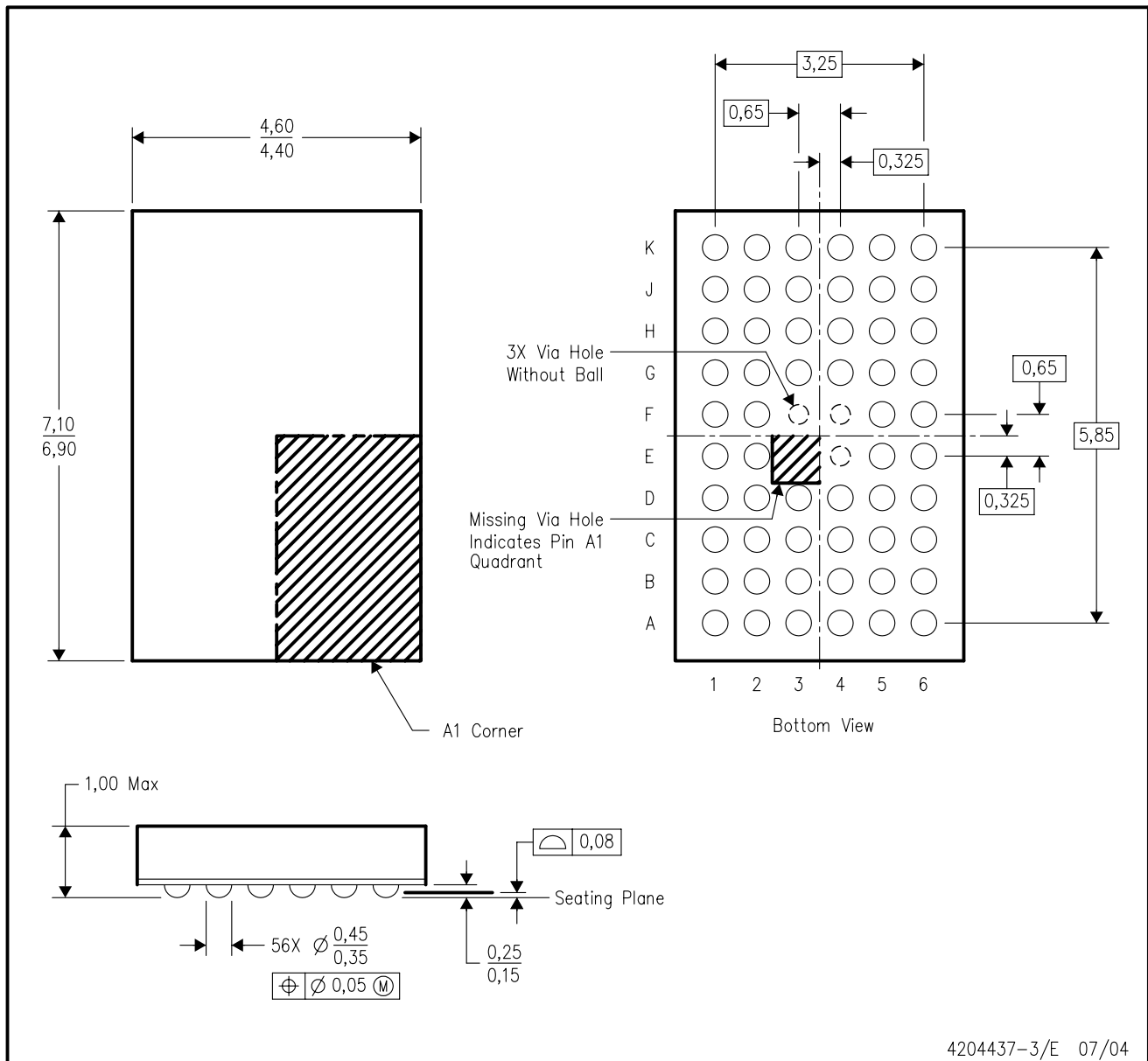
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

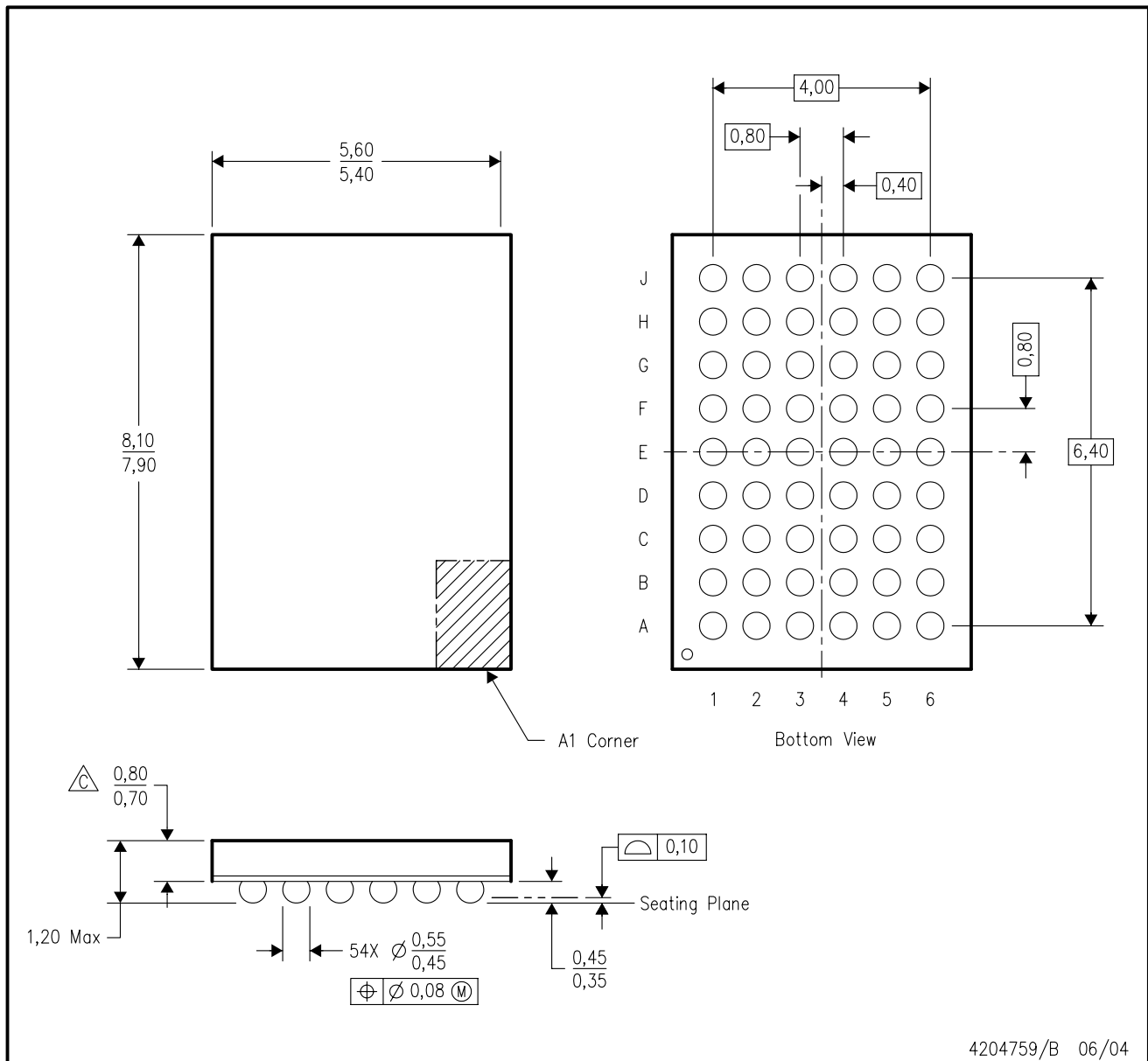


4204437-3/E 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GRD (R-PBGA-N54)

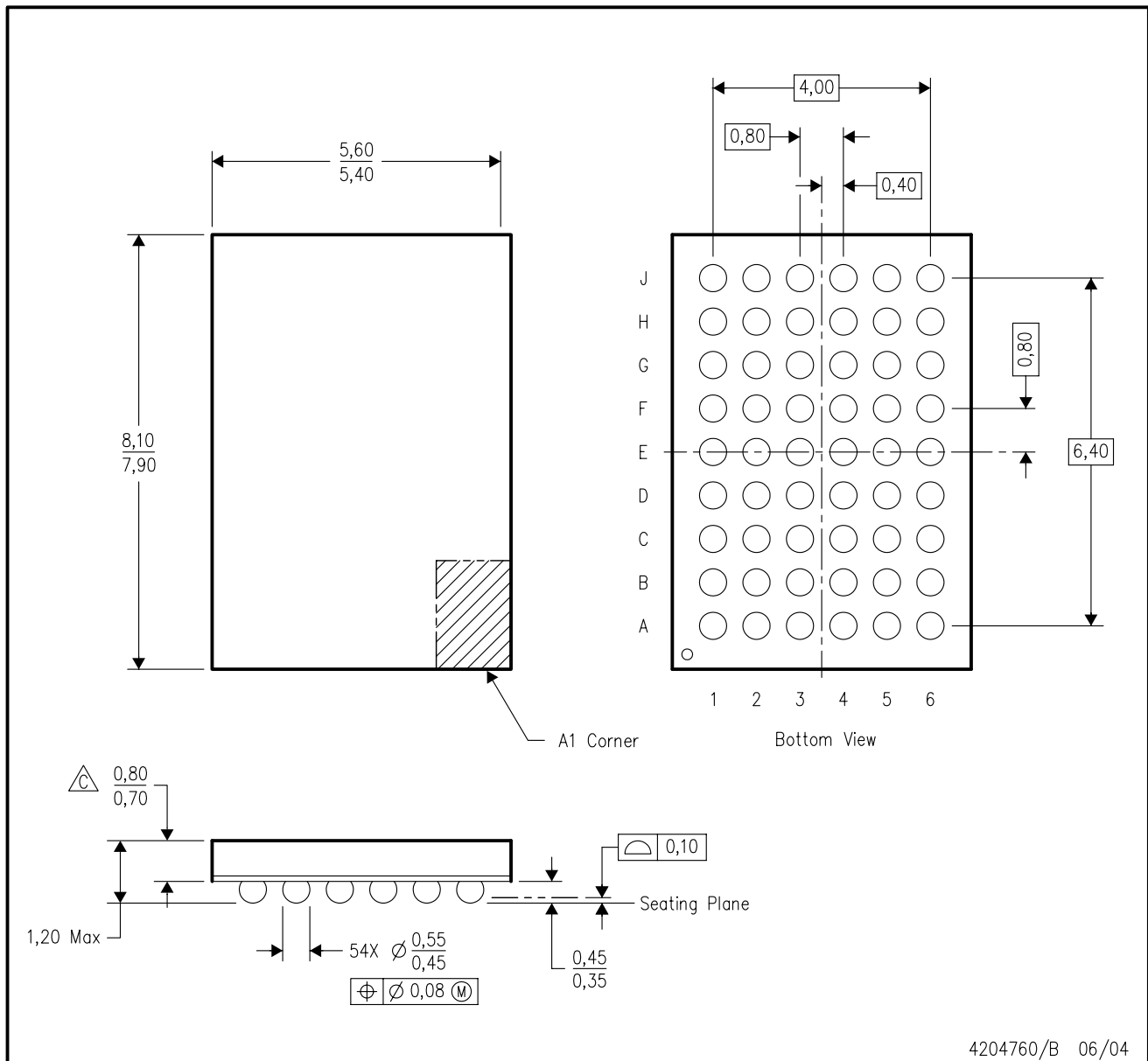
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MO-205 variation DD.
 - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

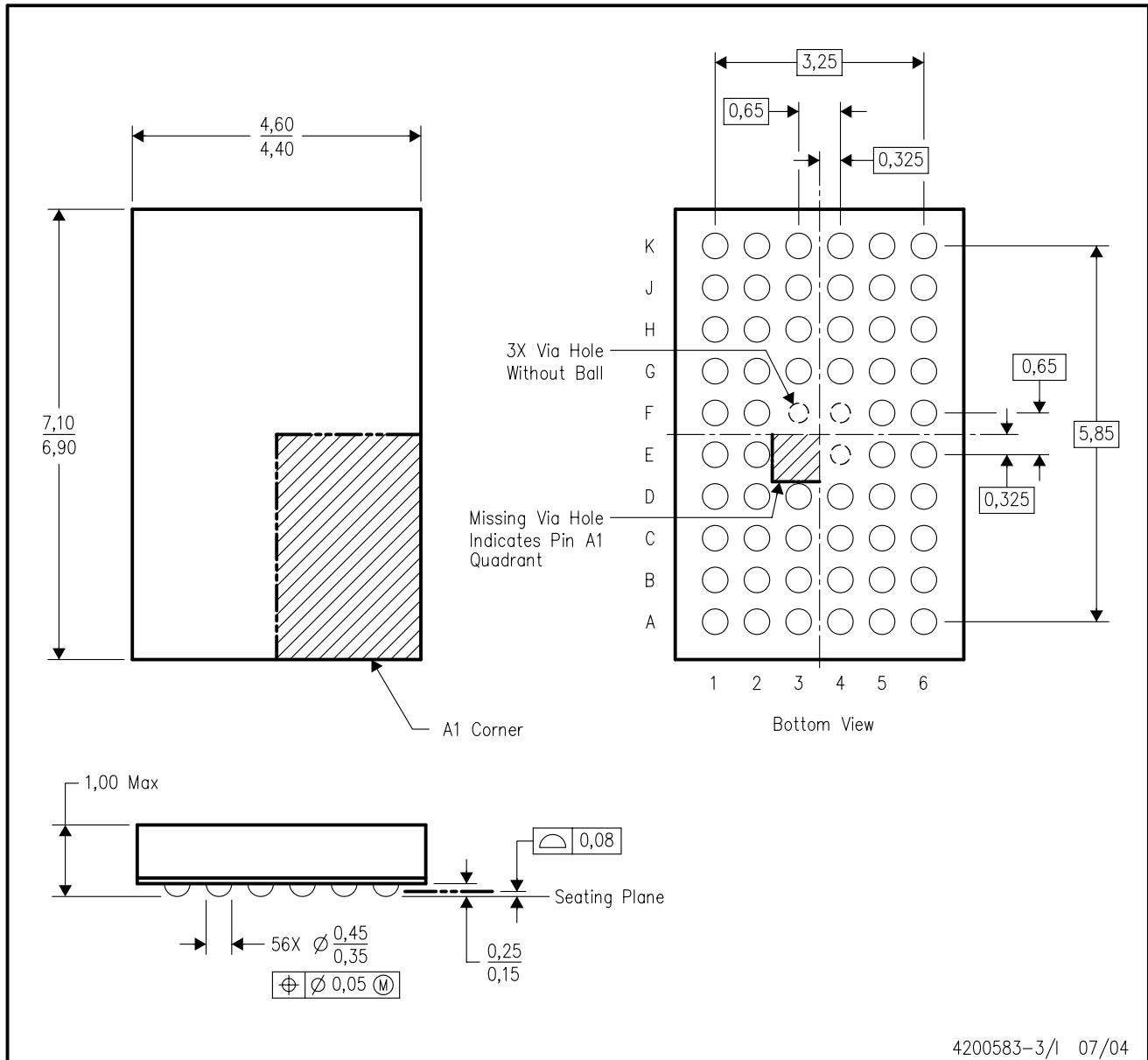
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



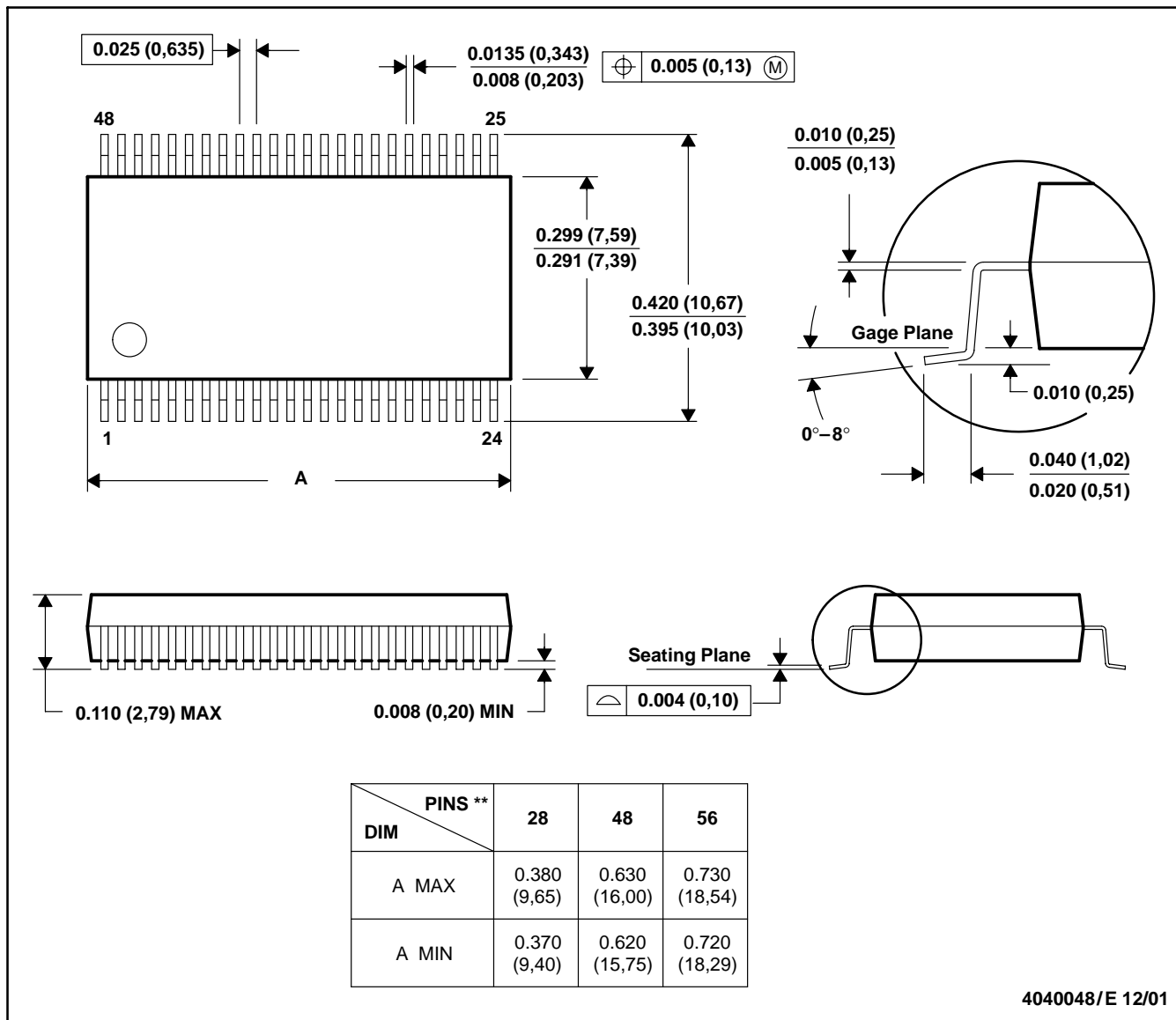
4200583-3/1 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

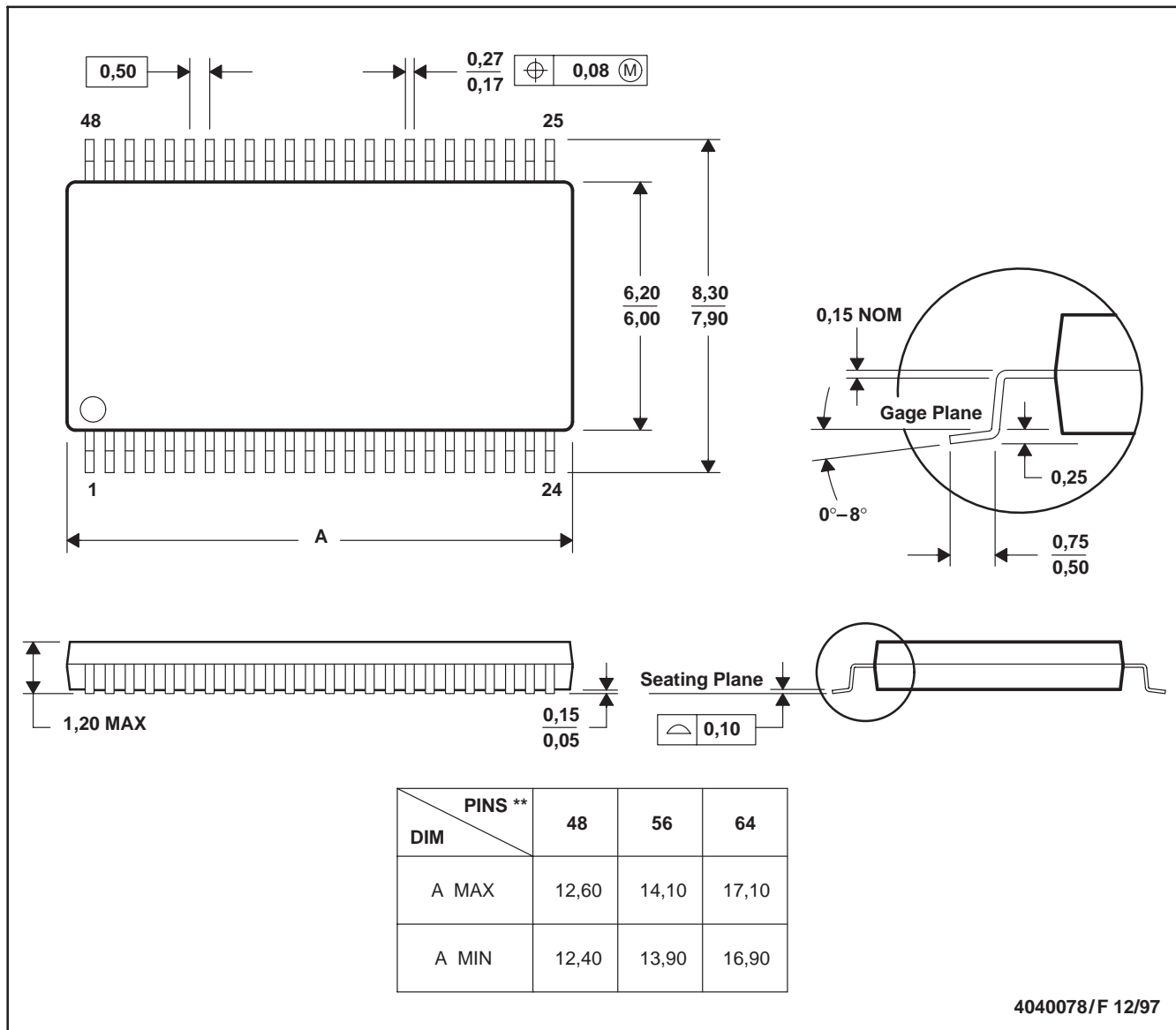


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|------------------|--|---------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

www.AllDataSheet.com

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

www.AllDataSheet.com