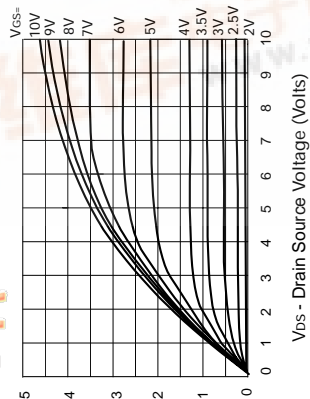


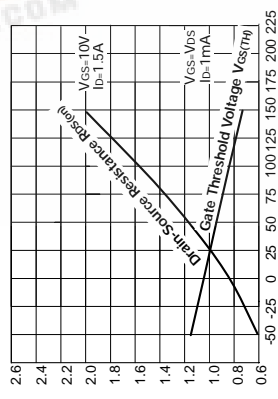


ZVN4210G

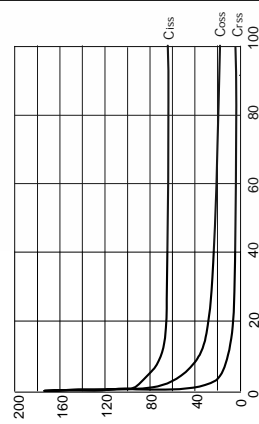
TYPICAL CHARACTERISTICS



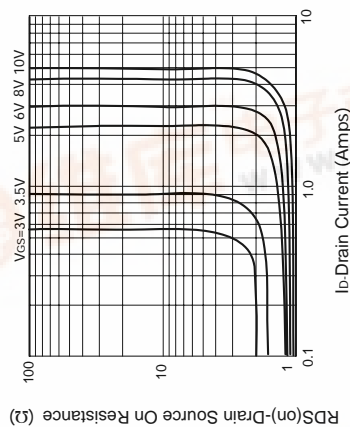
Saturation Characteristics



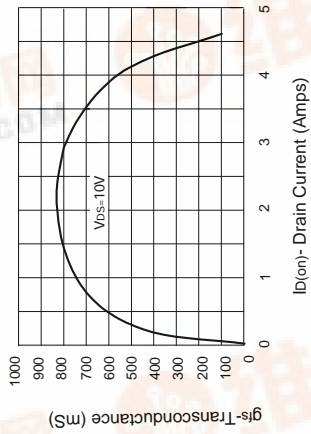
Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v Temperature



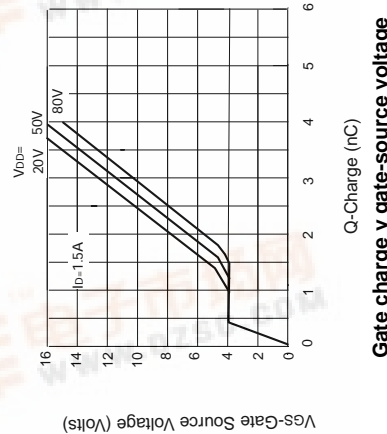
Capacitance v drain-source voltage



On-resistance v drain current



Transconductance v drain current



Gate charge v gate-source voltage

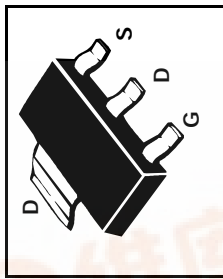
SOT223 N-CHANNEL ENHANCEMENT
MODE VERTICAL DMOS FET

ZVN4210G

ISSUE 2 - NOVEMBER 1995

FEATURES

- * Low $R_{DS(on)} = 1.5\Omega$
- PARTMARKING DETAIL - ZVN4210



查询ZVN4210G供应商

捷多邦, 专业PCB打样工厂, 24小时加急出货

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	0.8	A
Pulsed Drain Current	I_{DM}	6	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	2	W
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	100		V	$I_D=1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.8	2.4	V	$I_D=1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}		10 100	μA μA	$V_{DS}=100V, V_{GS}=0$ $V_{DS}=80V, V_{GS}=0V, T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_D(on)$	2.5		A	$V_{DS}=25V, V_{GS}=10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		1.5 1.8	Ω Ω	$V_{GS}=10V, I_D=1.5A$ $V_{GS}=5V, I_D=500mA$
Forward Transconductance(1)(2)	g_{fs}	250		mS	$V_{DS}=25V, I_D=1.5A$
Input Capacitance (2)	C_{iss}		100	pF	
Common Source Output Capacitance (2)	C_{oss}		40	pF	$V_{DS}=25V, V_{GS}=0V, f=1MHz$
Reverse Transfer Capacitance (2)	C_{rss}		12	pF	
Turn-On Delay Time (2)(3)	$t_d(on)$		4	ns	
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_d(off)$		20	ns	$V_{DS}=25V, I_D=1.5A$
Fall Time (2)(3)	t_f		30	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.
(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator. Spice parameter data is available upon request for this device.

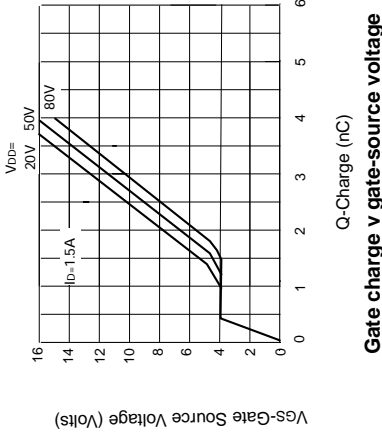
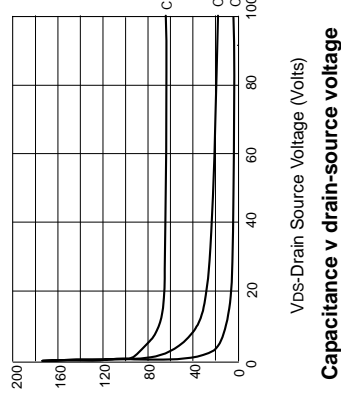
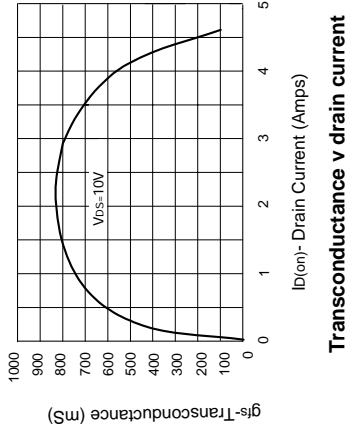
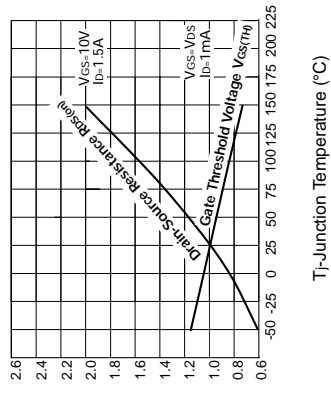
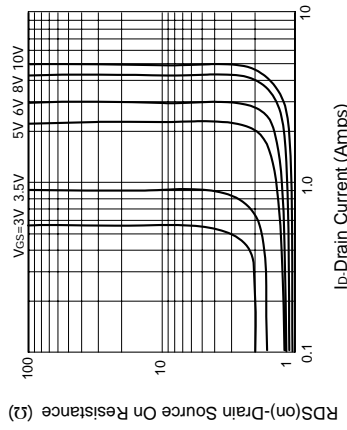
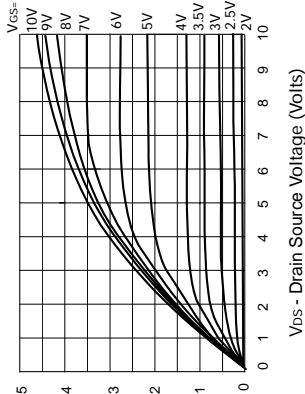
**SOT223 N-CHANNEL ENHANCEMENT
MODE VERTICAL DMOS FET**

ISSUE 2 - NOVEMBER 1995

FEATURES

- * Low $R_{DS(on)}$ = 1.5 Ω
- PARTMARKING DETAIL - ZVN4210

TYPICAL CHARACTERISTICS



ABSOLUTE MAXIMUM RATINGS.

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Power Dissipation at T _{amb} =25 $^{\circ}C$	P _{tot}	2	W
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PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
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Zero Gate Voltage Drain Current	I _{DSS}		10 100	μA μA	V _{DS} =100V, V _{GS} =0 V _{DS} =80V, V _{GS} =0V, T=125 $^{\circ}C$ (2)
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Static Drain-Source On-State Resistance (1)	R _{DS(on)}		1.5 1.8	Ω Ω	V _{GS} =10V, I _D =1.5A V _{GS} =5V, I _D =500mA
Forward Transconductance(1)(2)	g _{fs}	250		mS	V _{DS} =25V, I _D =1.5A
Input Capacitance (2)	C _{iss}		100	pF	
Common Source Output Capacitance (2)	C _{oss}		40	pF	V _{DS} =25V, V _{GS} =0V, f=1MHz
Reverse Transfer Capacitance (2)	C _{rss}		12	pF	
Turn-On Delay Time (2)(3)	t _{d(on)}		4	ns	
Rise Time (2)(3)	t _r		8	ns	
Turn-Off Delay Time (2)(3)	t _{d(off)}		20	ns	V _{DD} =25V, I _D =1.5A
Fall Time (2)(3)	t _f		30	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.
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