

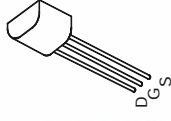
N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ISSUE 2 - MARCH 94

FEATURES

- * 100 Volt V_{DS}
- * $R_{DS(on)}=3\Omega$
- * Low threshold voltage

ZVNL110A



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current at $T_{amb}=25^{\circ}\text{C}$	I_D	320	mA
Pulsed Drain Current	I_{DM}	6	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}\text{C}$	P_{Tot}	700	mW
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	100		V	$I_D=1\text{mA}, V_{GS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.75	1.5	V	$I_D=1\text{mA}, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		100	nA	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}		10 500	μA μA	$V_{DS}=100\text{V}, V_{GS}=0$ $V_{DS}=80\text{V}, V_{GS}=0\text{V}, T=125^{\circ}\text{C}$ (2)
On-State Drain Current(1)	$I_{D(on)}$	750		mA	$V_{DS}=25\text{V}, V_{GS}=5\text{V}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		4.5 3.0	Ω Ω	$V_{GS}=5\text{V}, I_D=250\text{mA}$ $V_{GS}=10\text{V}, I_D=500\text{mA}$
Forward Transconductance (1)(2)	g_{fs}	225		mS	$V_{DS}=25\text{V}, I_D=500\text{mA}$
Input Capacitance (2)	C_{iss}		75	pF	
Common Source Output Capacitance (2)	C_{oss}		25	pF	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$
Reverse Transfer Capacitance (2)	C_{rss}		8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	
Rise Time (2)(3)	t_r		12	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		15	ns	$V_{DD}=25\text{V}, V_{GS}=10\text{V}, I_D=1\text{A}$
Fall Time (2)(3)	t_f		13	ns	

查询ZVNL110A供应商

捷多邦, 专业PCB打样工厂, 24小时加急出货

