SOT223 N-CHANNEL ENHANCEMENT MODE LOW THRESHOLD VERTICAL DMOS FET

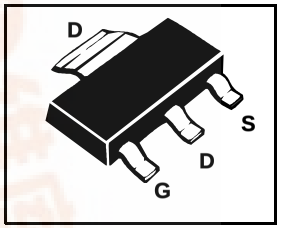
ZVNL110G

ISSUE 2 - FEBRUARY 1996 ✪

FEATURES

* LOW $R_{DS(ON)}$ - 3Ω

PARTMARKING DETAIL - ZVNL110



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current at T_{amb}=25°C	I_D	600	mA
Pulsed Drain Current	I_{DM}	6	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	2	W
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	100		V	I_D=1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.75	1.5	V	I_D=1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}		100	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}		10 100	µA µA	V_{DS}=100V, V_{GS}=0V V_{DS}=80V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	750		mA	V_{DS}=25V, V_{GS}=5V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		4.5 3.0	Ω Ω	V_{GS}=5V, I_D=250mA V_{GS}=10V, I_D=500mA
Forward Transconductance(1)(2)	g_{fs}	225		mS	V_{DS}=25V, I_D=500mA
Input Capacitance (2)	C_{iss}		75	pF	V_{DS}=25V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		25	pF	
Reverse Transfer Capacitance (2)	C_{rss}		8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	V_{DD}≈25V, I_D=1A, V_{GS} =10V
Rise Time (2)(3)	t_r		12	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		15	ns	
Fall Time (2)(3)	t_f		13	ns	

(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2% (2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator