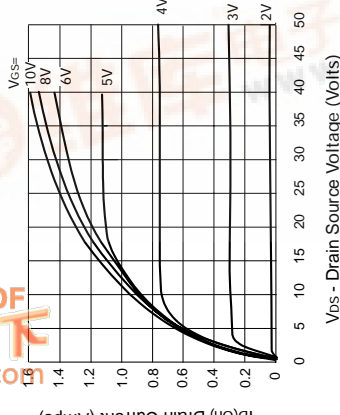


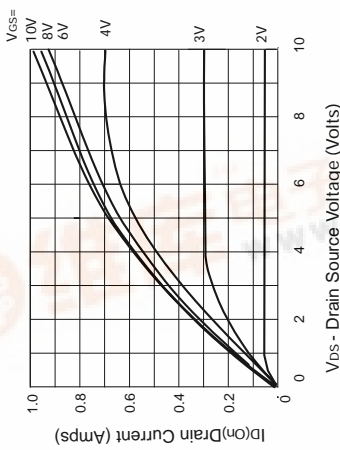


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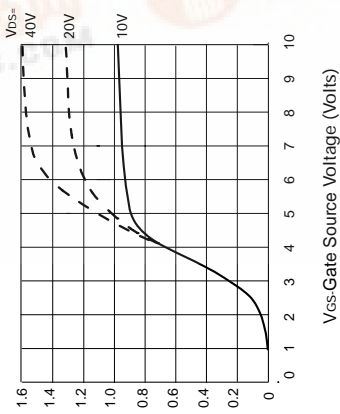
**TYPICAL CHARACTERISTICS**



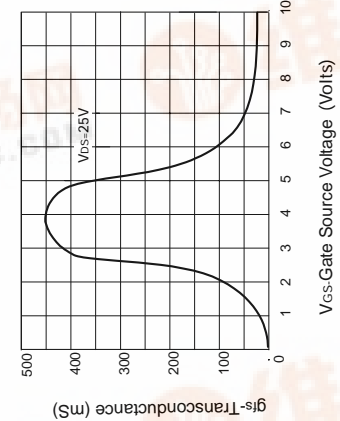
**Output Characteristics**



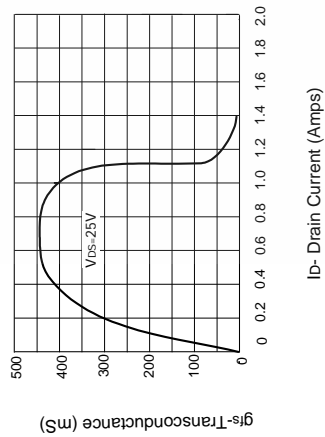
**Saturation Characteristics**



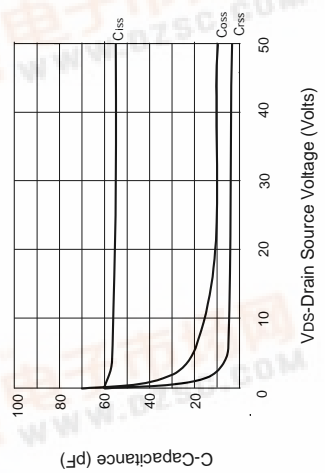
**Transfer Characteristics**



**Transconductance v gate-source voltage**



**Transconductance v drain current**



**Capacitance v drain-source voltage**

**N-CHANNEL ENHANCEMENT  
MODE VERTICAL DMOS FET**

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**FEATURES**

- \* 200 Volt  $V_{DS}$
- \*  $R_{DS(on)}=10\Omega$
- \* Low threshold

**APPLICATIONS**

- \* Telephone handsets

**ABSOLUTE MAXIMUM RATINGS.**

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	200	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	$I_D$	180	mA
Pulsed Drain Current	$I_{DM}$	2	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation at $T_{amb}=25^{\circ}C$	$P_{Tot}$	700	mW
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^{\circ}C$

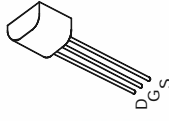
**ELECTRICAL CHARACTERISTICS (at  $T_{amb} = 25^{\circ}C$  unless otherwise stated).**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	200		V	$I_D=1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.5	1.5	V	$I_D=1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	$I_{GSS}$		100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	$I_{DSS}$		10 100	$\mu A$ $\mu A$	$V_{DS}=200V, V_{GS}=0$ $V_{DS}=160V, V_{GS}=0V, T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	500		mA	$V_{DS}=25V, V_{GS}=5V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		10 10	$\Omega$ $\Omega$	$V_{GS}=5V, I_D=250mA$ $V_{GS}=3V, I_D=125mA$
Forward Transconductance (1)(2)	$g_{fs}$	200		mS	$V_{DS}=25V, I_D=250mA$
Input Capacitance (2)	$C_{iss}$		85	pF	$V_{DS}=25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	$C_{oss}$		20	pF	
Reverse Transfer Capacitance (2)	$C_{rss}$		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	ns	
Rise Time (2)(3)	$t_r$		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		20	ns	
Fall Time (2)(3)	$t_f$		12	ns	

(1) Measured under pulsed conditions. Width=300 $\mu s$ . Duty cycle  $\leq 2\%$  (2) Sample test.

(3) Switching times measured with 50 $\Omega$  source impedance and <5ns rise time on a pulse generator

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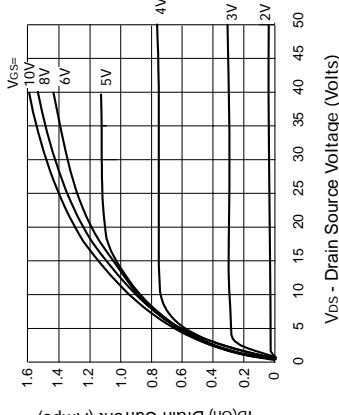


E-Line  
TO92 Compatible

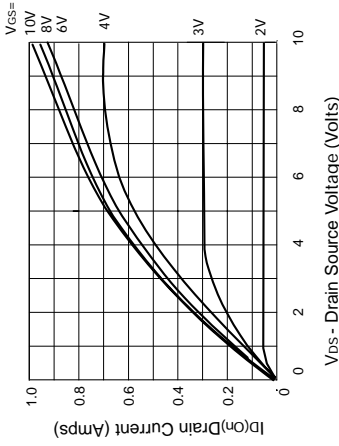
# ZVNL120A

# N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

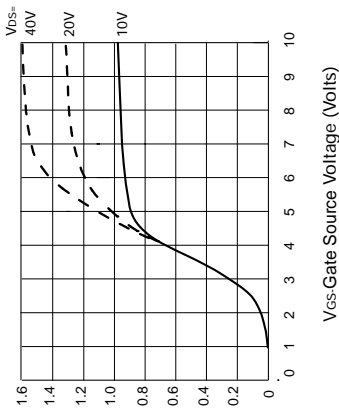
## TYPICAL CHARACTERISTICS



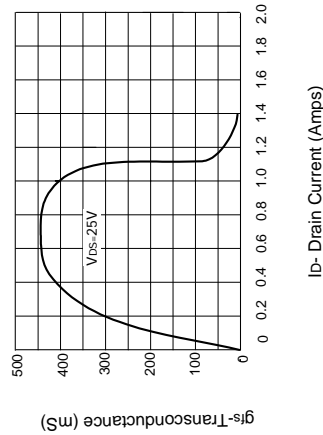
**Output Characteristics**



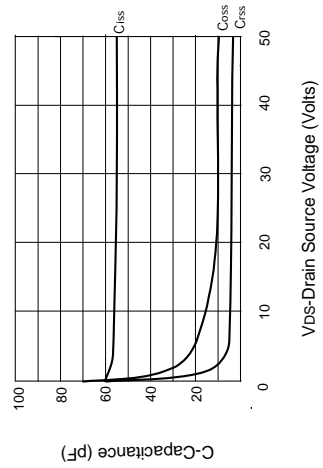
**Saturation Characteristics**



**Transfer Characteristics**



**Transconductance v drain current**



**Capacitance v drain-source voltage**

# ZVNL120A

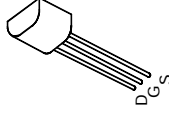
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## FEATURES

- \* 200 Volt V<sub>DS</sub>
- \* R<sub>DS(on)</sub> = 10Ω
- \* Low threshold

## APPLICATIONS

- \* Telephone handsets



E-Line  
TO92 Compatible

## ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V <sub>DS</sub>	200	V
Continuous Drain Current at T <sub>amb</sub> =25°C	I <sub>D</sub>	180	mA
Pulsed Drain Current	I <sub>DM</sub>	2	A
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Power Dissipation at T <sub>amb</sub> =25°C	P <sub>Tot</sub>	700	mW
Operating and Storage Temperature Range	T <sub>J</sub> ; T <sub>stg</sub>	-55 to +150	°C

## ELECTRICAL CHARACTERISTICS (at T<sub>amb</sub> = 25°C unless otherwise stated).

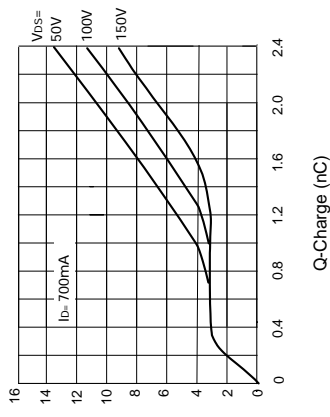
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	200		V	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	0.5	1.5	V	I <sub>D</sub> = 1mA, V <sub>DS</sub> = V <sub>GS</sub>
Gate-Body Leakage	I <sub>GSS</sub>		100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		10	μA	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0
			100	μA	V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0V, T = 125°C(2)
On-State Drain Current(1)	I <sub>D(on)</sub>	500		mA	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 5V
Static Drain-Source On-State Resistance (1)	R <sub>DS(on)</sub>		10	Ω	V <sub>GS</sub> = 5V, I <sub>D</sub> = 250mA
			10	Ω	V <sub>GS</sub> = 3V, I <sub>D</sub> = 125mA
Forward Transconductance (1)(2)	g <sub>fs</sub>	200		mS	V <sub>DS</sub> = 25V, I <sub>D</sub> = 250mA
Input Capacitance (2)	C <sub>iss</sub>		85	pF	
Common Source Output Capacitance (2)	C <sub>oss</sub>		20	pF	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0V, f = 1MHz
Reverse Transfer Capacitance (2)	C <sub>rss</sub>		7	pF	
Turn-On Delay Time (2)(3)	t <sub>d(on)</sub>		8	ns	
Rise Time (2)(3)	t <sub>r</sub>		8	ns	
Turn-Off Delay Time (2)(3)	t <sub>d(off)</sub>		20	ns	V <sub>DD</sub> = 25V, I <sub>D</sub> = 250mA
Fall Time (2)(3)	t <sub>f</sub>		12	ns	

(1) Measured under pulsed conditions. Width=300μs. Duty cycle ≤2% (2) Sample test.

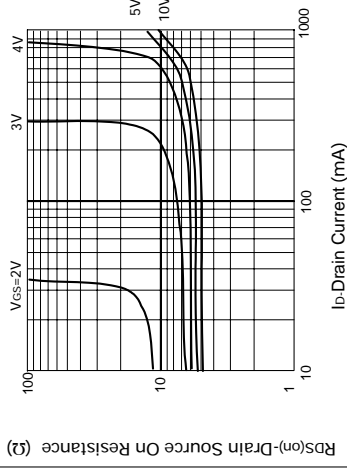
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator

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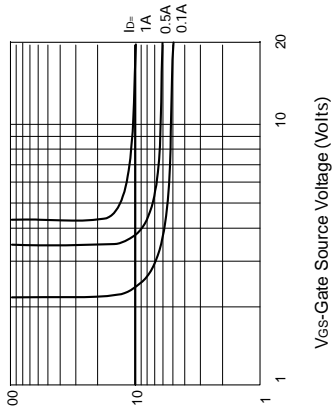
## TYPICAL CHARACTERISTICS



Gate charge v gate-source voltage



On-resistance v drain current



On-resistance vs gate-source voltage

Normalised  $R_{ds(on)}$  and  $V_{gs(th)}$  vs Temperature