

SOT223 P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

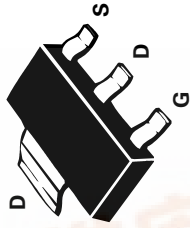
ZVP2120G

ISSUE 3 - OCTOBER 1995

FEATURES

- * 200 Volt V_{DS}
- * $R_{DS(on)}=25\Omega$

PARTMARKING DETAIL – ZVP2120
COMPLEMENTARY TYPE – ZVN2120G



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-200	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	-200	mA
Pulsed Drain Current	I_{DM}	-1.2	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	2	W
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-200		V	$I_D=-1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D=-1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		-20	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}		-10 -100	μA μA	$V_{DS}=200V, V_{GS}=0$ $V_{DS}=160V, V_{GS}=0V, T=125^{\circ}C$ (2)
On-State Drain Current(1)	$I_{D(on)}$	-300		mA	$V_{DS}=25V, V_{GS}=-10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		25	Ω	$V_{GS}=-10V, I_D=-150mA$
Forward Transconductance (1)(2)	g_{fs}	50		mS	$V_{DS}=25V, I_D=-150mA$
Input Capacitance (2)	C_{iss}		100	pF	
Common Source Output Capacitance (2)	C_{oss}		25	pF	$V_{DS}=25V, V_{GS}=0V, f=1MHz$
Reverse Transfer Capacitance (2)	C_{rss}		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	
Rise Time (2)(3)	t_r		15	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		12	ns	
Fall Time (2)(3)	t_f		15	ns	$V_{DD}=-25V, I_D=-150mA$

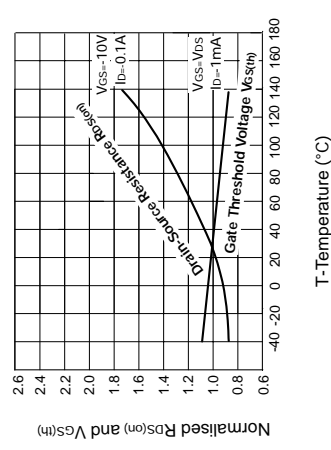
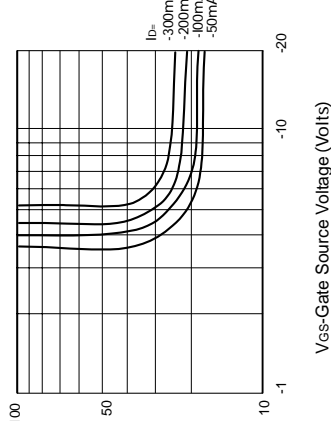
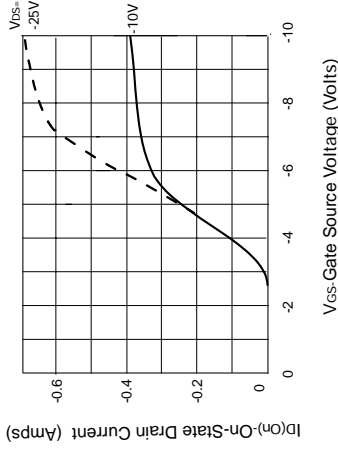
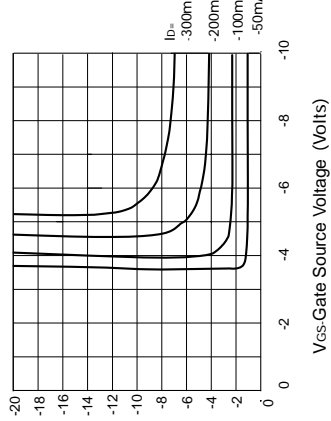
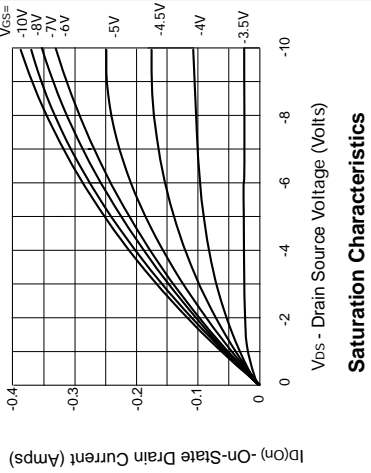
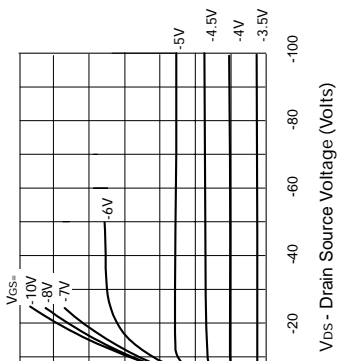
(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.

(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator

查询ZVP2120G供应商

捷多邦, 专业PCB打样工厂, 24小时加急出货

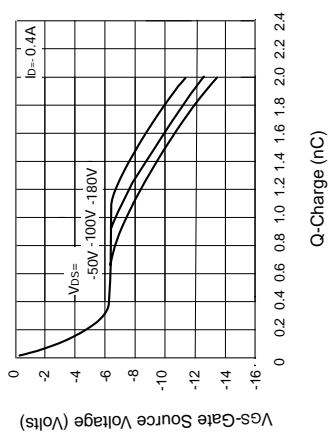
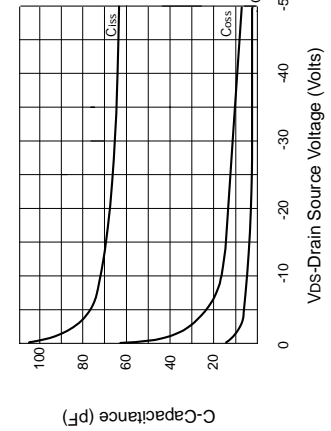
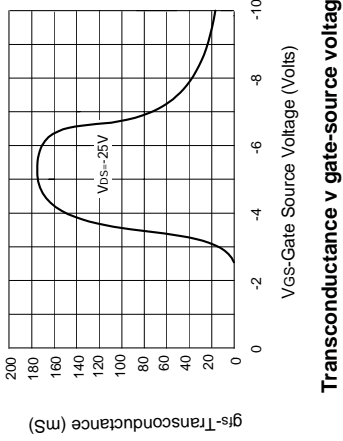
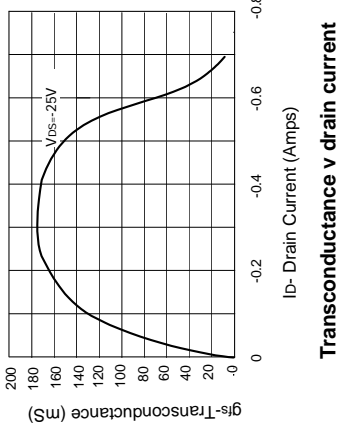
TYPICAL CHARACTERISTICS



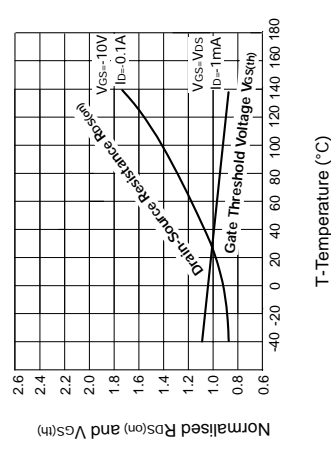
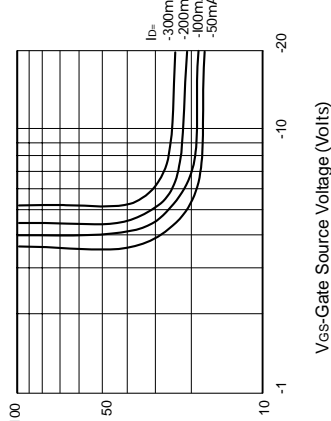
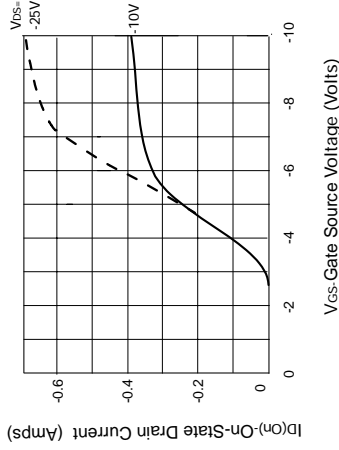
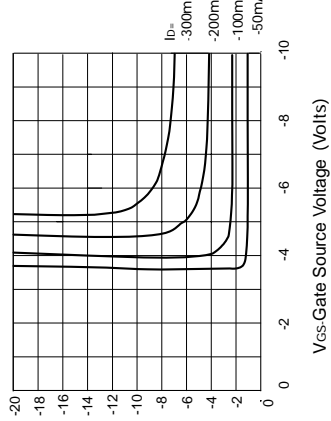
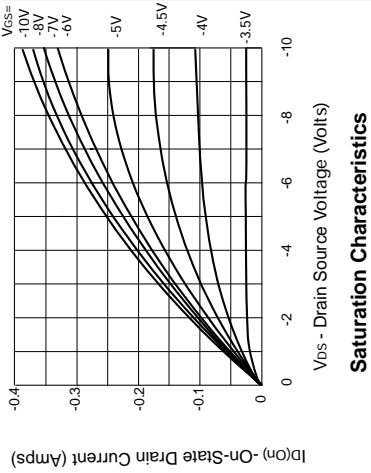
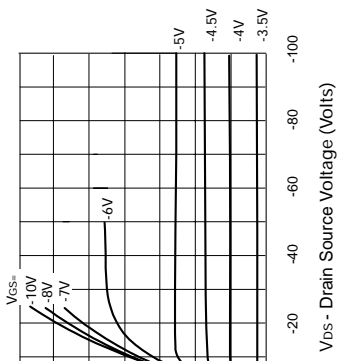
On-resistance vs gate-source voltage

Normalized $R_{DS(on)}$ and $V_{GS(th)}$ vs Temperature

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