

ZXM64N035L3

35V N-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

$V_{(BR)DSS} = 35V$; $R_{DS(on)} = 0.060\Omega$; $I_D = 13A$

DESCRIPTION

This new generation of high cell density planar MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

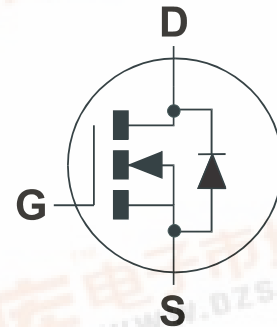


FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- TO220 package

APPLICATIONS

- 100W Class D Audio Output Stage
- Motor Control

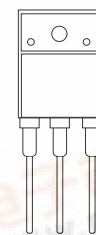


ORDERING INFORMATION

DEVICE	MULTIPLES
ZXM64N035L3	1000

DEVICE MARKING

- ZXM6
4N035



G D S
Front View

ZXM64N035L3

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DSS}	35	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current (V _{GS} =10V; T _C =25°C)(a) (V _{GS} =10V; T _A =25°C)(b)	I _D	13 3.5	A
Pulsed Drain Current (b)	I _{DM}	30	A
Continuous Source Current (Body Diode)(b)	I _S	2.4	A
Pulsed Source Current (Body Diode)(b)	I _{SM}	30	A
Power Dissipation at T _A =25°C (a) Linear Derating Factor	P _D	20 160	W mW/°C
Power Dissipation at T _A =25°C (b) Linear Derating Factor	P _D	1.5 12	W mW/°C
Operating and Storage Temperature Range	T _j ;T _{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Case (a)	R _{θJC}	6.25	°C/W
Junction to Ambient (b)	R _{θJA}	83.3	°C/W

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ELECTRICAL CHARACTERISTICS (at $T_A = 25^\circ\text{C}$ unless otherwise stated).

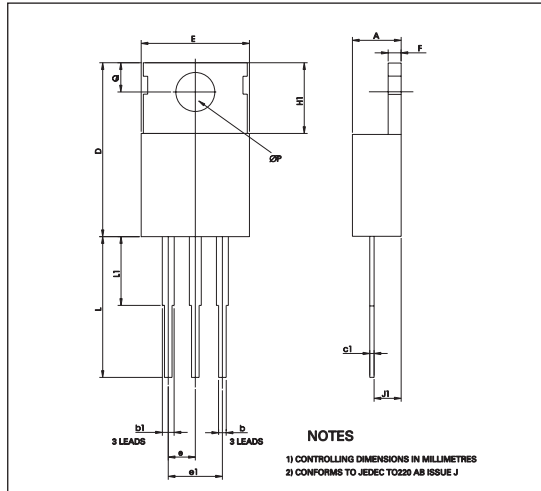
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	35			V	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	$V_{DS}=35\text{V}$, $V_{GS}=0\text{V}$
Gate-Body Leakage	I_{GSS}			100	nA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0			V	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.060 0.070	Ω Ω	$V_{GS}=10\text{V}$, $I_D=3.7\text{A}$ $V_{GS}=4.5\text{V}$, $I_D=1.9\text{A}$
Forward Transconductance (1)(3)	g_{fs}	4.3			S	$V_{DS}=10\text{V}$, $I_D=1.9\text{A}$
DYNAMIC (3)						
Input Capacitance	C_{iss}		950		pF	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$
Output Capacitance	C_{oss}		200		pF	
Reverse Transfer Capacitance	C_{rss}		50		pF	
SWITCHING(2) (3)						
Turn-On Delay Time	$t_{d(on)}$		4.2		ns	$V_{DD}=15\text{V}$, $I_D=3.7\text{A}$ $R_G=6.0\Omega$, $V_{GS}=10\text{V}$
Rise Time	t_r		4.5		ns	
Turn-Off Delay Time	$t_{d(off)}$		20.5		ns	
Fall Time	t_f		8		ns	
Total Gate Charge	Q_g			27	nC	$V_{DS}=24\text{V}$, $V_{GS}=10\text{V}$, $I_D=3.7\text{A}$
Gate-Source Charge	Q_{gs}			5	nC	
Gate-Drain Charge	Q_{gd}			4.5	nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}			0.95	V	$T_J=25^\circ\text{C}$, $I_S=3.7\text{A}$, $V_{GS}=0\text{V}$
Reverse Recovery Time (3)	t_{rr}		24.5		ns	$T_J=25^\circ\text{C}$, $I_F=3.7\text{A}$, $di/dt=100\text{A}/\mu\text{s}$
Reverse Recovery Charge (3)	Q_{rr}		19.1		nC	

NOTES

- (1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$.
(2) Switching characteristics are independent of operating junction temperature.
(3) For design aid only, not subject to production testing.

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Package Outline



Package Dimensions

DIM	Millimetres		Inches	
	Min	Max	Min	Max
A	3.56	4.82	0.140	0.189
b	0.38	1.01	0.015	0.040
b1	1.15	1.77	0.045	0.070
c1	0.41	0.50	0.016	0.020
D	14.23	16.51	0.560	0.650
E	9.66	10.66	0.380	0.419
e	2.29	2.79	0.090	0.110
e1	4.83	5.33	0.190	0.210
F	0.51	1.39	0.20	0.055
H1	5.58	6.85	0.230	0.270
J1	2.04	2.92	0.080	0.115
L	12.70	14.73	0.500	0.580
L1	—	6.35	—	0.250
ØP	3.54	4.08	0.139	0.160
Q	2.54	3.42	0.100	0.134

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