

## Dual 8-Bit Parity Generator/Checker

### Features

- Function, pinout and drive compatible with FCT and F logic
- FCT-A speed at 7.5 ns max. (Com'I)
- FCT-B speed at 5.6 ns max. (Com'I)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V
- Fully compatible with TTL input and output logic levels
- Sink Current 64 mA (Com'I), 32 mA (Mil)
- Source Current 32 mA (Com'I), 12 mA (Mil)

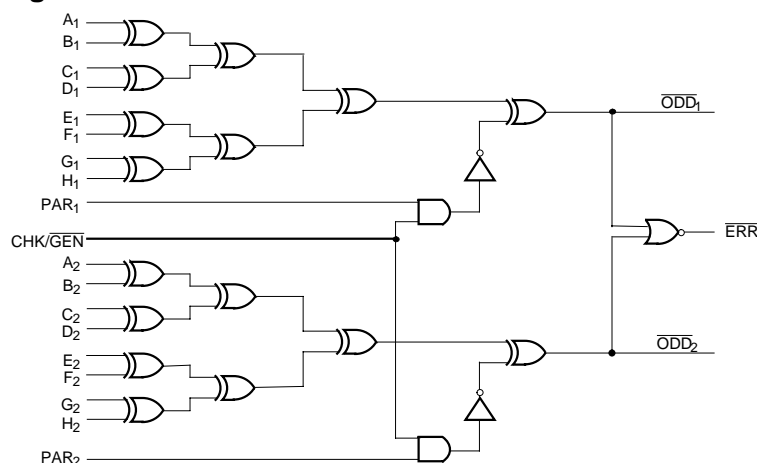
- Two 8-bit parity generator/checkers
- Open drain Active LOW parity error output
- Expandable for larger word widths

### Functional Description

The FCT480T is a high-speed dual 8-bit parity generator/checker. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a sum and parity error output. The FCT480T can be used in ODD parity systems. The parity error output is open-drain, designed for easy expansion of the word width by a wired-OR connection of several FCT480T type devices. Since additional logic is not needed, the parity generation or checking times remain the same as for an individual FCT480T device.

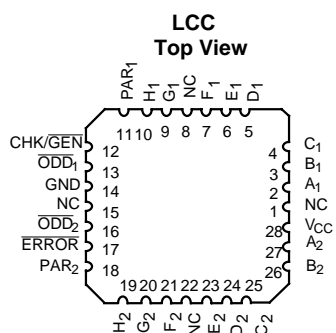
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

### Logic Block Diagram

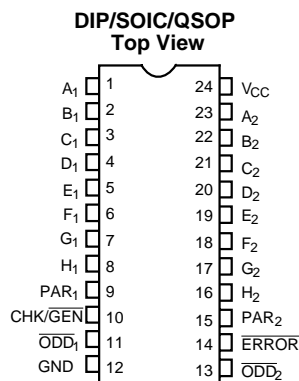


FCT480T-1

### Pin Configurations



FCT480T2



FCT480T3

**Function Table**

Inputs					Outputs		
A <sub>1</sub> to H <sub>1</sub>	A <sub>2</sub> to H <sub>2</sub>	CHK/GEN	PAR <sub>1</sub>	PAR <sub>2</sub>	ODD <sub>1</sub>	ODD <sub>2</sub>	ERROR
Number of A <sub>1</sub> to H <sub>1</sub> Inputs HIGH is EVEN	Number of A <sub>2</sub> to H <sub>2</sub> Inputs HIGH is EVEN	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L
	Number of Inputs HIGH A <sub>2</sub> to H <sub>2</sub> is ODD	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
Number of A <sub>1</sub> to H <sub>1</sub> Inputs HIGH is ODD	Number of A <sub>2</sub> to H <sub>2</sub> Inputs HIGH is EVEN	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
	Number of A <sub>2</sub> to H <sub>2</sub> Inputs HIGH is ODD	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H

**Maximum Ratings**<sup>[1, 2]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with  
Power Applied .....–65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation .....0.5W

Static Discharge Voltage.....>2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	All	–40°C to +85°C	5V ± 5%
Military <sup>[3]</sup>	All	–55°C to +125°C	5V ± 10%

**Notes:**

1. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
3. T<sub>A</sub> is the “instant on” case temperature.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -32 mA	Com'l	2.0			V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -15 mA	Com'l	2.4	3.3		V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -12 mA	Mil	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 64 mA	Com'l		0.3	0.55	V
		V <sub>CC</sub> = Min., I <sub>OL</sub> = 32 mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage			2.0			V
V <sub>IL</sub>	Input LOW Voltage					0.8	V
V <sub>H</sub>	Hysteresis <sup>[5]</sup>	All inputs			0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-0.7	-1.2	V
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>				5	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7V				±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.5V				±1	μA
I <sub>OZH</sub>	Off State HIGH-Level Output Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 2.7V				10	μA
I <sub>OZL</sub>	Off State LOW-Level Output Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V				-10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[6]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V		-60	-120	-225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> = 0V, V <sub>OUT</sub> = 4.5V				±1	μA

**Capacitance<sup>[5]</sup>**

Parameter	Description	Typ. <sup>[4]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Notes:**

4. Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC}-0.2V$	0.1	0.2	mA
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}, V_{IN}=3.4V,$ <sup>[7]</sup> $f_1=0$ , Outputs Open	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[8]</sup>	$V_{CC}=\text{Max.}$ , One Bit Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	0.06	0.12	mA/ MHz
$I_C$	Total Power Supply Current <sup>[9]</sup>	$V_{CC}=\text{Max.}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=2.5$ MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	0.7	1.4	mA
		$V_{CC}=\text{Max.}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=2.5$ MHz, $V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	1.0	2.4	mA
		$V_{CC}=\text{Max.}$ , 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling at $f_1=2.5$ MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	2.5	5.0 <sup>[10]</sup>	mA
		$V_{CC}=\text{Max.}$ , 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling at $f_1=2.5$ MHz, $V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	6.5	21.0 <sup>[10]</sup>	mA

## Switching Characteristics Over the Operating Range

	Description	FCT480AT	FCT480BT		Unit
		Com'l	Military	Com'l	
$t_{PLH}$ $t_{PHL}$	Propagation Delay A to EVEN/ODD	7.5 7.0	7.0 6.6	5.6 5.6	ns
$t_{PLH}$ <sup>[11]</sup> $t_{PHL}$	Propagation Delay A to ERROR	7.0 8.5	7.0 8.1	5.6 6.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay CHK/GEN to EVEN/ODD	6.5 7.5	6.3 7.4	5.9 5.9	ns
$t_{PLH}$ <sup>[11]</sup> $t_{PHL}$	Propagation Delay CHK/GEN to ERROR	7.5 7.0	7.1 6.9	5.7 5.5	ns

### Notes:

- Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamperes and all frequencies are in megahertz.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.
- $t_{PLH}$  is measured up to  $V_{OUT}=V_{OL}+0.3V$

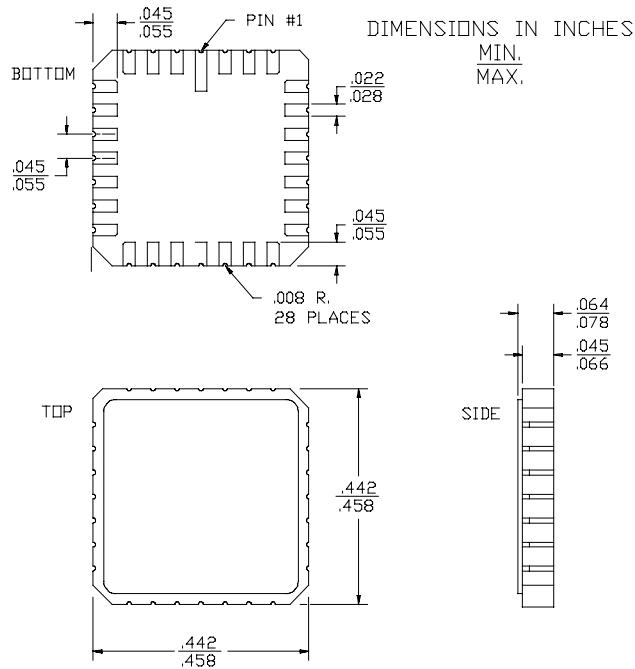
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.6	CY74FCT480BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480BTQCT	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT480BTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
7.0	CY54FCT480BTLMB	L64	28-Square Leadless Chip Carrier	Military
7.5	CY74FCT480ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT480ATQCT	Q13	24-Lead (150-Mil) QSOP	

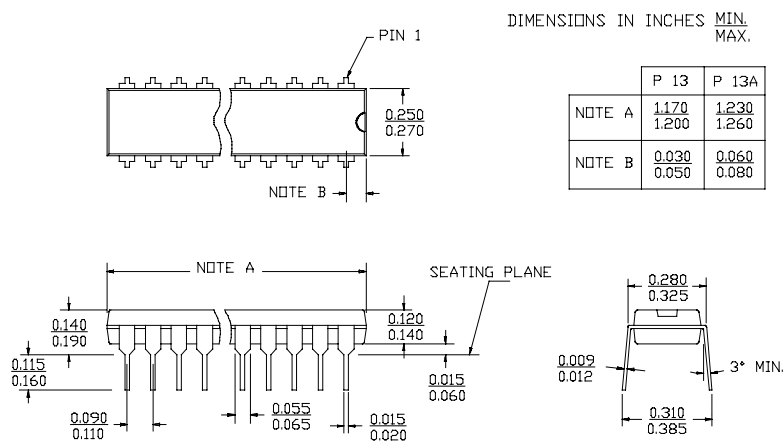
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## Package Diagrams

### 28-Square Leadless Chip Carrier L64 MIL-STD-1835 C-4

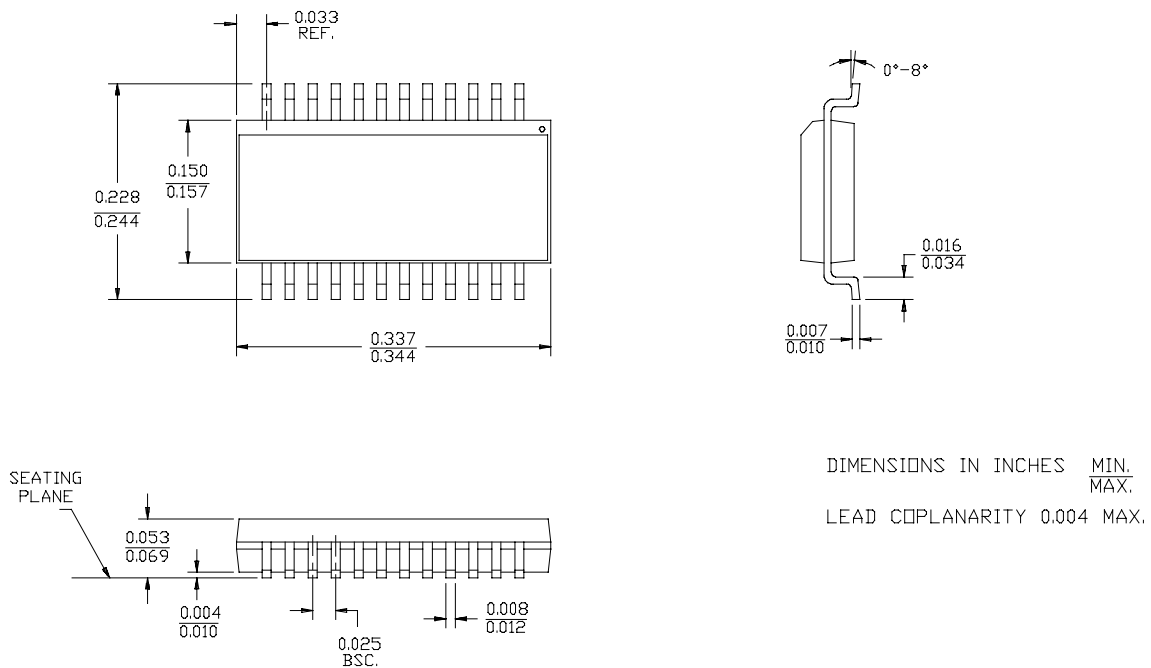


### 24-Lead (300-Mil) Molded DIP P13/P13A

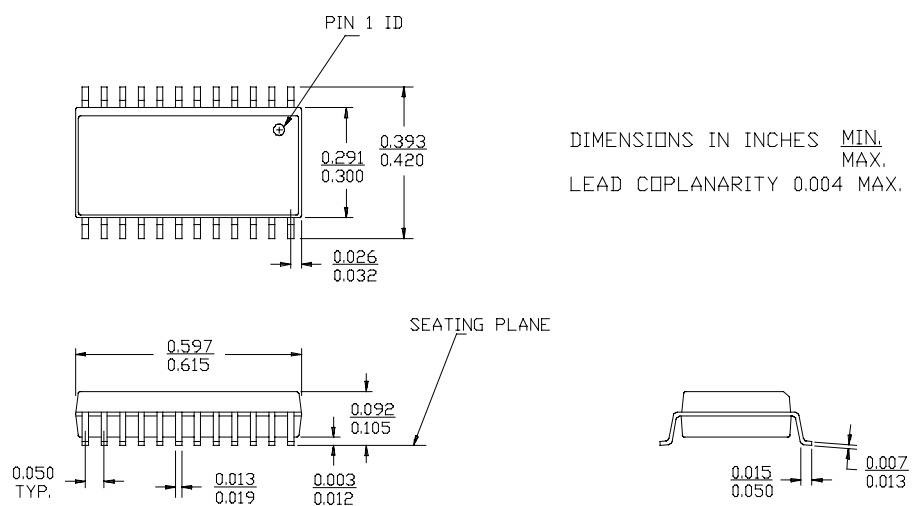


**Package Diagrams** (continued)

**24-Lead Quarter Size Outline Q13**



**24-Lead (300-Mil) Molded SOIC S13**



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