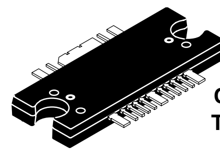
Freescale Semiconductor
Technical Data

Document Number: MW6IC2015N
Rev. 2, 2/2007

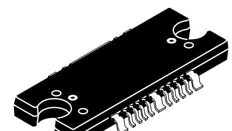
RF LDMOS Wideband Integrated Power Amplifiers

MW6IC2015NBR1
MW6IC2015GNBR1

1805-1990 MHz, 15 W, 26 V
GSM/GSM EDGE, CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS



CASE 1329-09
TO-272 WB-16
PLASTIC
MW6IC2015NBR1



CASE 1329A-03
TO-272 WB-16 GULL
PLASTIC
MW6IC2015GNBR1

The MW6IC2015N wideband integrated circuit is designed for base station applications. It uses Freescale's newest High Voltage (26 to 32 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband on-chip design makes it usable from 1805 to 1990 MHz. The linearity performances cover all modulation formats for cellular applications: GSM, GSM EDGE, PHS, TDMA, CDMA, W-CDMA and TD-SCDMA.

Final Application

- Typical Two-Tone Performance: V_{DD} = 26 Volts, I_{DQ1} = 100 mA, I_{DQ2} = 170 mA, P_{out} = 15 Watts PEP, Full Frequency Band (1805-1880 MHz or 1930-1990 MHz)
  Power Gain — 26 dB
  Power Added Efficiency — 28%
  IMD — -30 dBc

Driver Application

- Typical GSM EDGE Performance: V_{DD} = 26 Volts, I_{DQ1} = 130 mA, I_{DQ2} = 170 mA, P_{out} = 3 Watts Avg., Full Frequency Band (1805-1880 MHz or 1930-1990 MHz)
  Power Gain — 27 dB
  Power Added Efficiency — 19%
  Spectral Regrowth @ 400 kHz Offset = -69 dBc
  Spectral Regrowth @ 600 kHz Offset = -78 dBc
  EVM — 0.8% rms
- Capable of Handling 3:1 VSWR, @ 26 Vdc, 1990 MHz, 15 Watts CW Output Power
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 8 W CW P_{out}.

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- Integrated ESD Protection
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

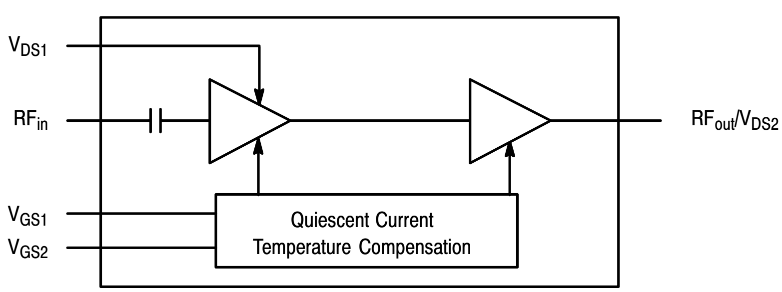
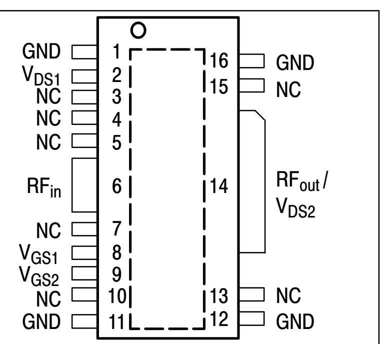


Figure 1. Functional Block Diagram



(Top View)
Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +6	Vdc
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature	T_J	200	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Final Application (P_{out} = 15 W CW)	Stage 1, 26 Vdc, I_{DQ1} = 100 mA		4.3	
	Stage 2, 26 Vdc, I_{DQ2} = 170 mA		1.2	
Driver Application (P_{out} = 3 W CW)	Stage 1, 26 Vdc, I_{DQ1} = 130 mA		4.3	
	Stage 2, 26 Vdc, I_{DQ2} = 170 mA		1.3	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale 1930-1990 MHz Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 100 mA, I_{DQ2} = 170 mA, P_{out} = 15 W PEP, f1 = 1930 MHz, f2 = 1930.1 MHz and f1 = 1990 MHz, f2 = 1990.1 MHz, Two-Tone CW					
Power Gain	G_{ps}	24	26	—	dB
Power Added Efficiency	PAE	26	28	—	%
Intermodulation Distortion	IMD	—	-30	-27	dBc
Input Return Loss	IRL	—	—	-10	dB
Typical Two-Tone Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 100 mA, I_{DQ2} = 170 mA, P_{out} = 15 W PEP, 1805-1880 MHz, Two-Tone CW, 100 kHz Tone Spacing					
Power Gain	G_{ps}	—	26	—	dB
Power Added Efficiency	PAE	—	28	—	%
Intermodulation Distortion	IMD	—	-30	—	dBc
Input Return Loss	IRL	—	-10	—	dB

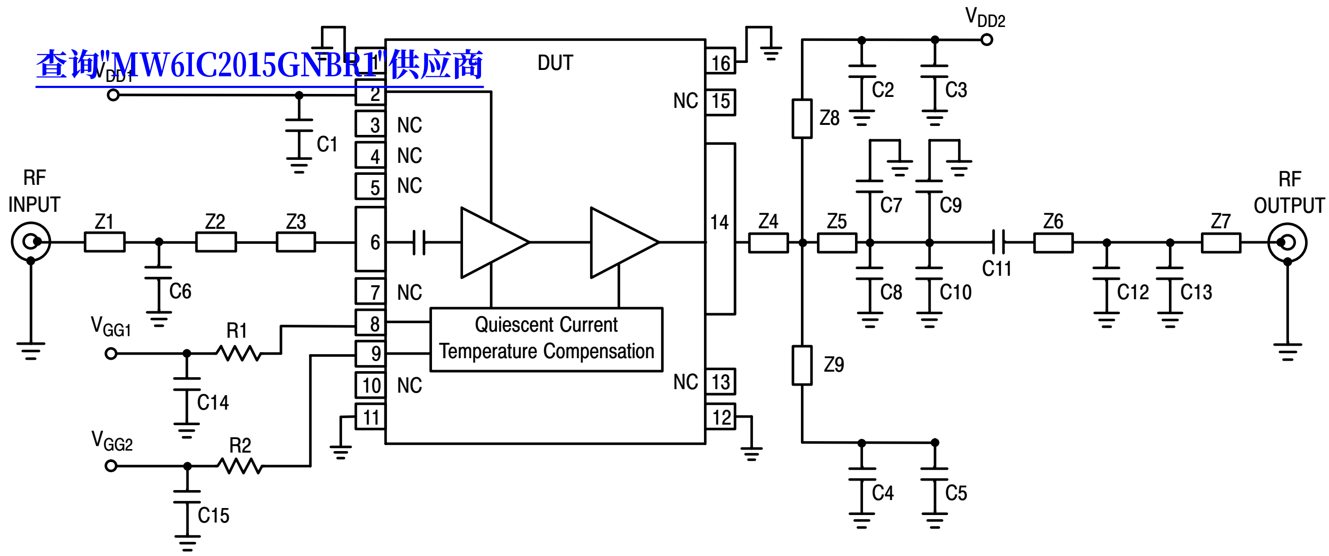
1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 100 mA, I_{DQ2} = 170 mA, 1805-1880 MHz and 1930-1990 MHz					
Saturated Pulsed Output Power, CW (8 μsec(on), 1 msec(off))	P_{sat}	—	35	—	W
Quiescent Current Accuracy over Temperature with 1.8 kΩ Gate Feed Resistors (-10 to 85°C) (1)	ΔI_{QT}	—	±3	—	%
Gain Flatness in 30 MHz Bandwidth @ P_{out} = 3 W CW	G_F	—	0.3	—	dB
Average Deviation from Linear Phase in 30 MHz Bandwidth @ P_{out} = 3 W CW	Φ	—	±1	—	°
Average Group Delay @ P_{out} = 3 W CW Including Output Matching	Delay	—	2.7	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 3 W CW, Six Sigma Window	ΔΦ	—	±15	—	°
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 130 mA, I_{DQ2} = 170 mA, P_{out} = 3 W Avg., 1805-1990 MHz and 1930-1990 MHz EDGE Modulation					
Power Gain	G_{ps}	—	27	—	dB
Power Added Efficiency	PAE	—	19	—	%
Error Vector Magnitude	EVM	—	0.8	—	%
Spectral Regrowth at 400 kHz Offset	SR1	—	-69	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-78	—	dBc

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977.



Z1*	1.68″ x 0.08″ Microstrip	Z6*	0.61″ x 0.04″ Microstrip
Z2	0.50″ x 0.08″ Microstrip	Z7	1.30″ x 0.04″ Microstrip
Z3	0.15″ x 0.04″ Microstrip	Z8, Z9	1.18″ x 0.08″ Microstrip
Z4	0.13″ x 0.35″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z5	0.10″ x 0.35″ Microstrip		

* Variable for tuning.

Figure 3. MW6IC2015NBR1(GNBR1) Test Circuit Schematic — 1930-1990 MHz

Table 6. MW6IC2015NBR1(GNBR1) Test Circuit Component Designations and Values — 1930-1990 MHz

Part	Description	Part Number	Manufacturer
C1, C14, C15	2.2 μF Chip Capacitors	C3225X5R1H225MT	TDK
C2, C4, C11	5.6 pF Chip Capacitors	ATC100B5R6CT500XT	ATC
C3, C5	10 μF Chip Capacitors	C5750X5R1H106MT	TDK
C6	1 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C7, C8	2.2 pF Chip Capacitors	ATC100B2R2BT500XT	ATC
C9, C10	0.5 pF Chip Capacitors	ATC100B0R5BT500XT	ATC
C12	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C13	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
R1	10 kΩ, 1/4 W Chip Resistor	CRCW12061001FKTA	Vishay
R2	18 Ω, 1/4 W Chip Resistor	CRCW120618R0FKTA	Vishay

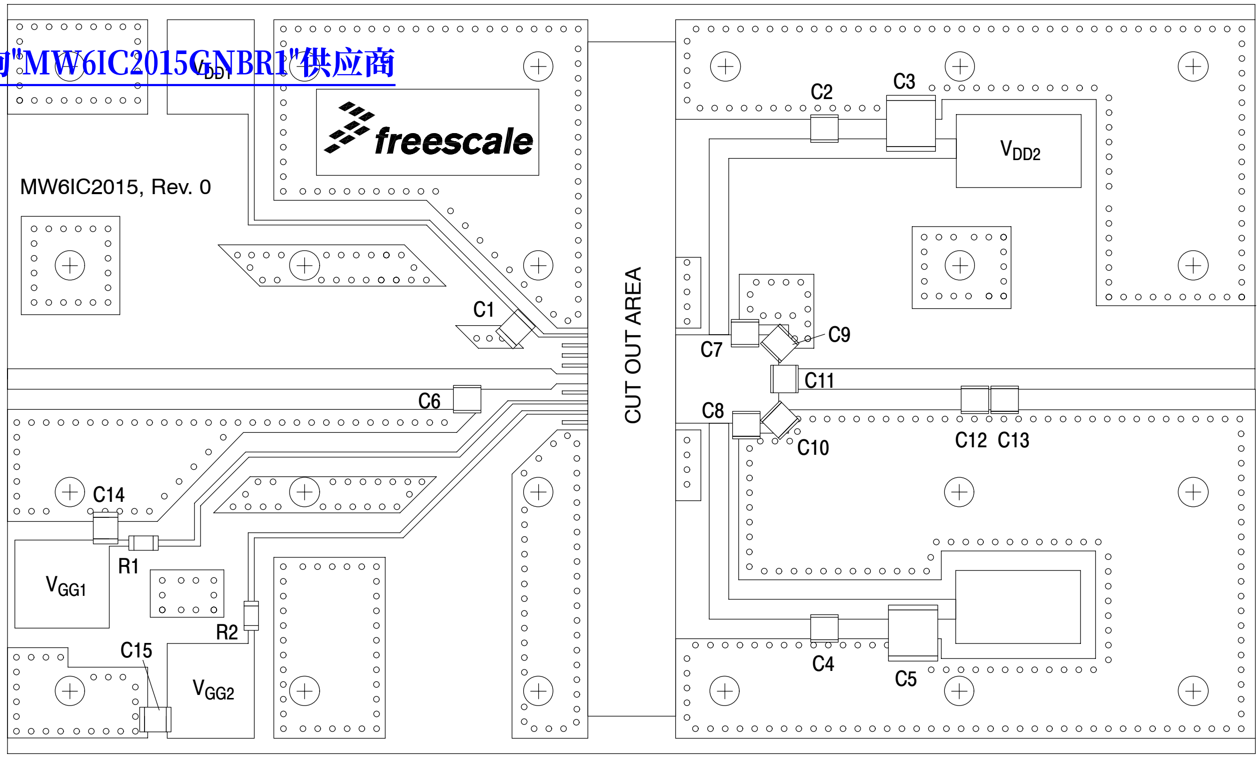


Figure 4. MW6IC2015NBR1(GNBR1) Test Circuit Component Layout — 1930-1990 MHz

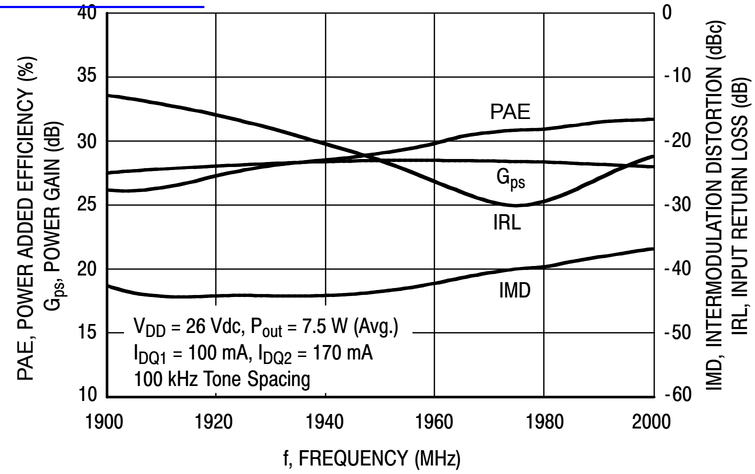


Figure 5. Two-Tone Wideband Performance @ P_{out} = 7.5 Watts Avg.

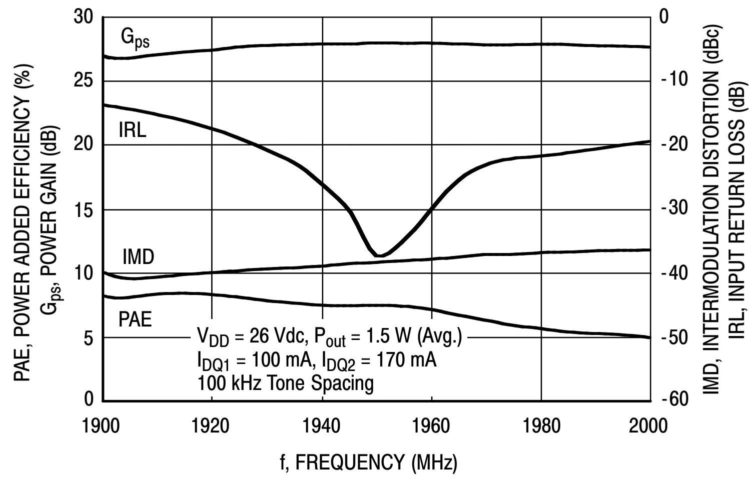


Figure 6. Two-Tone Wideband Performance @ P_{out} = 1.5 Watts Avg.

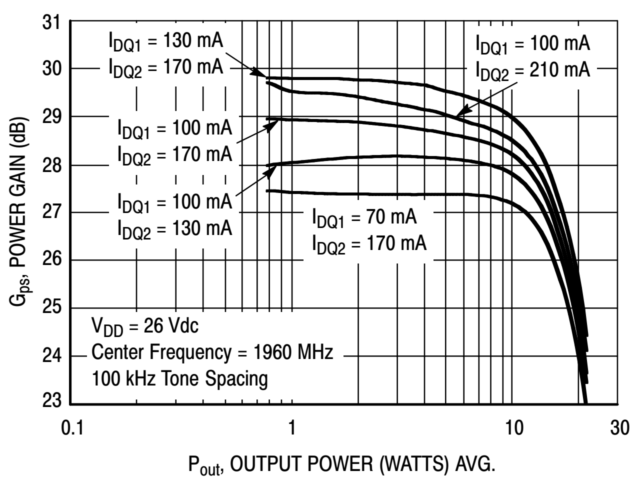


Figure 7. Two-Tone Power Gain versus Output Power

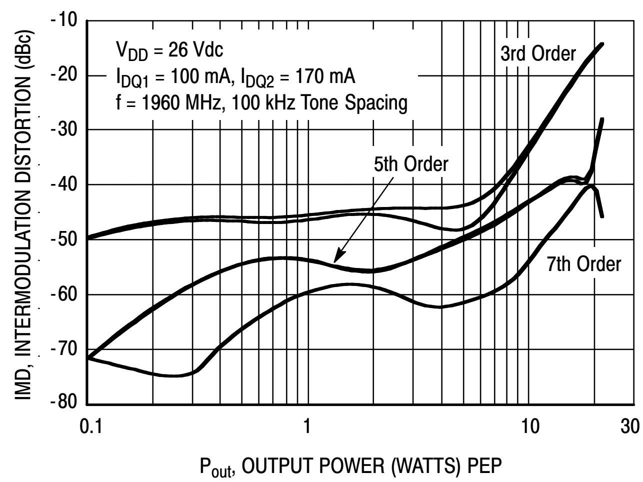


Figure 8. Intermodulation Distortion Products versus Output Power

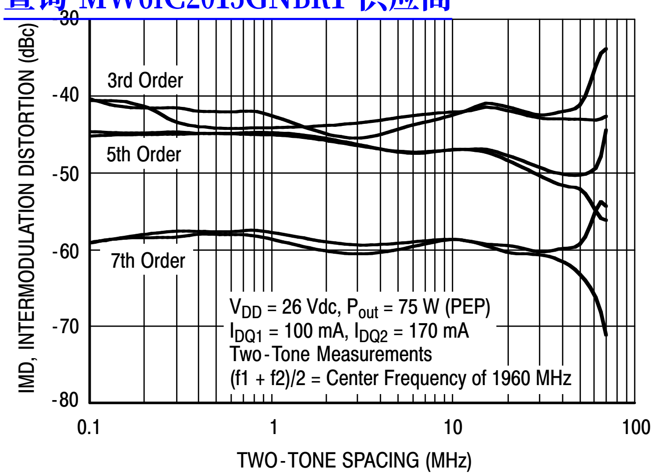


Figure 9. Intermodulation Distortion Products versus Tone Spacing

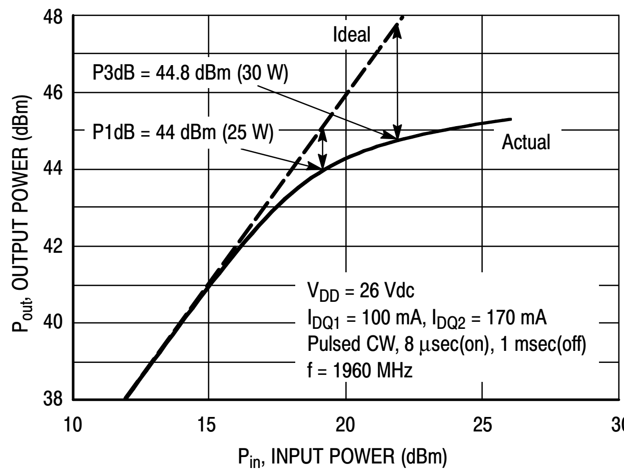


Figure 10. Pulsed CW Output Power versus Input Power

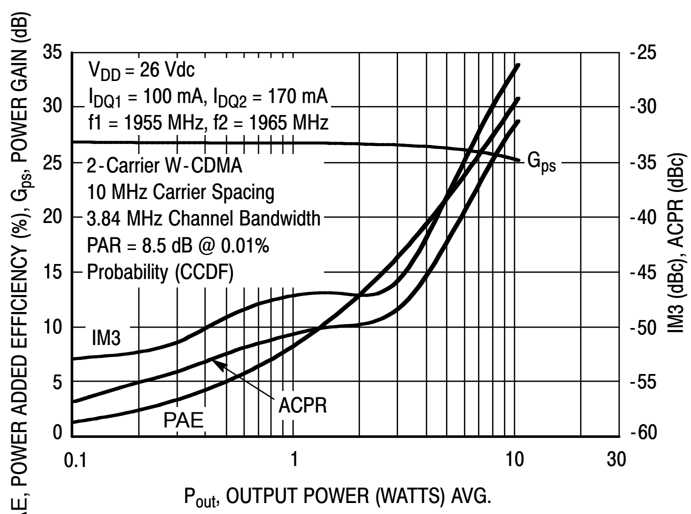


Figure 11. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Power Added Efficiency versus Output Power

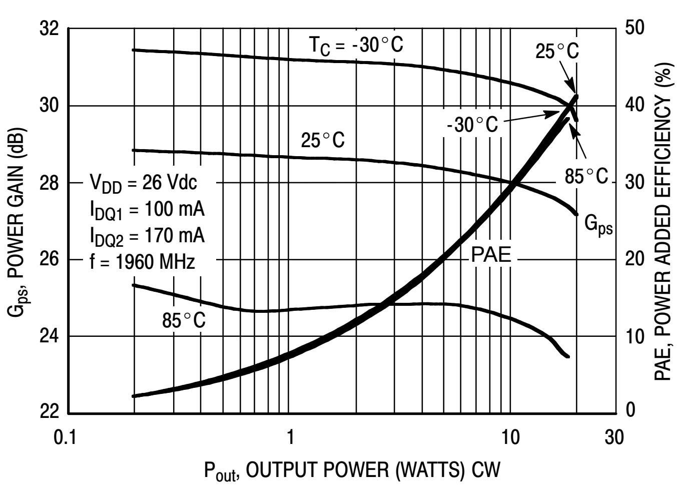


Figure 12. Power Gain and Power Added Efficiency versus CW Output Power

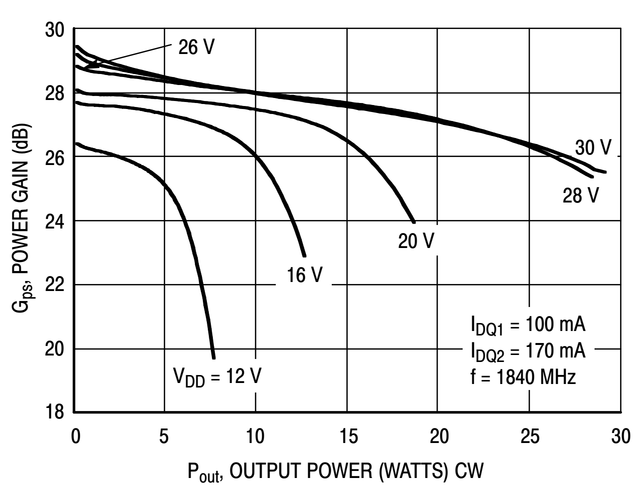


Figure 13. Power Gain versus Output Power

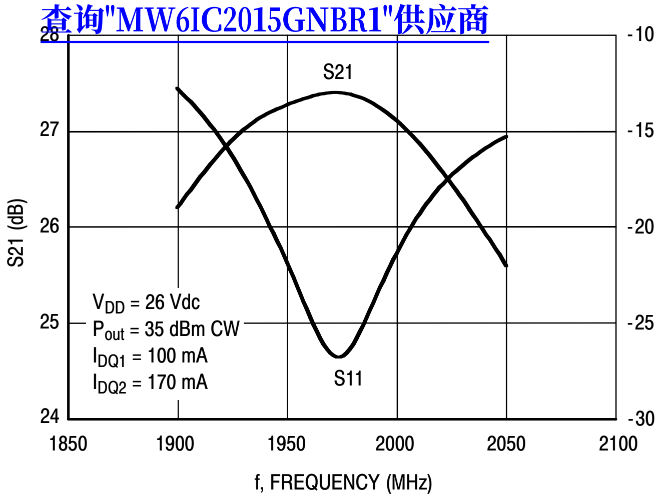


Figure 14. Broadband Frequency Response

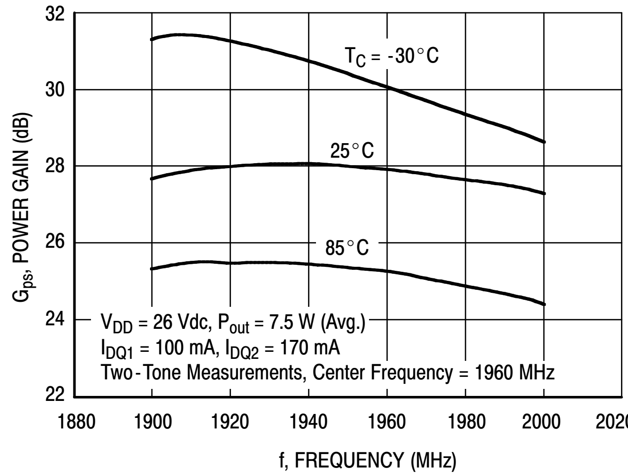


Figure 15. Power Gain versus Frequency

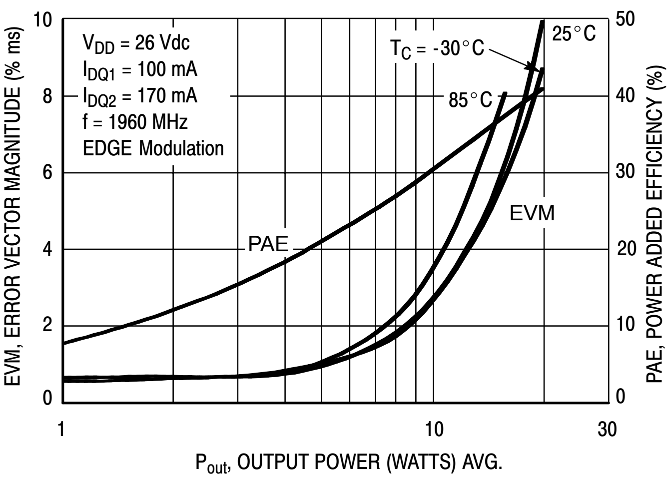


Figure 16. EVM and Power Added Efficiency versus Output Power

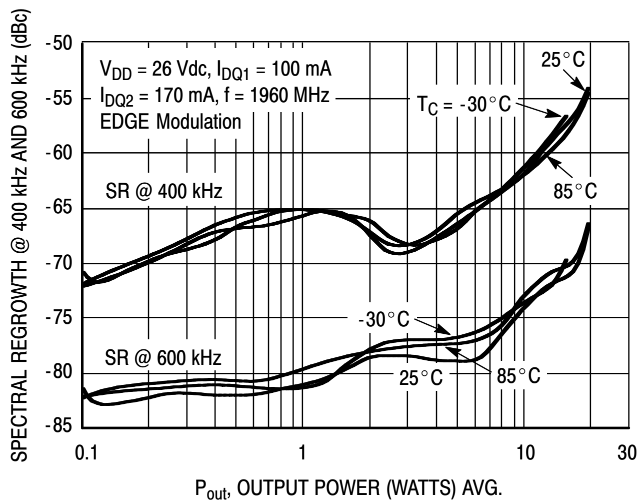
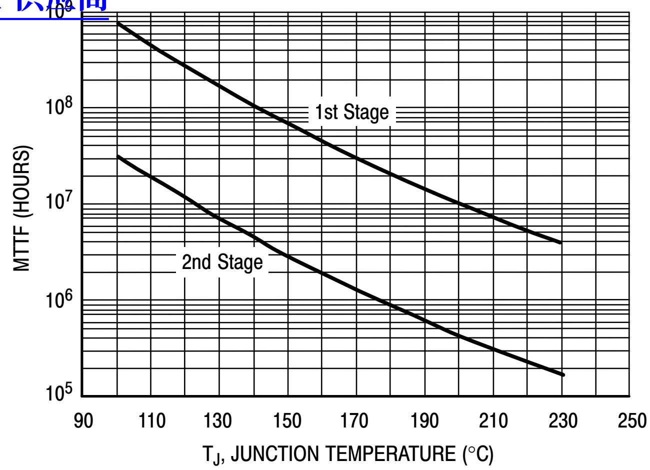


Figure 17. Spectral Regrowth at 400 and 600 kHz versus Output Power

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 26 Vdc, P_{out} = 15 W PEP, and PAE = 28%.

MTTF calculator available at http:/www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 18. MTTF versus Junction Temperature

GSM TEST SIGNAL

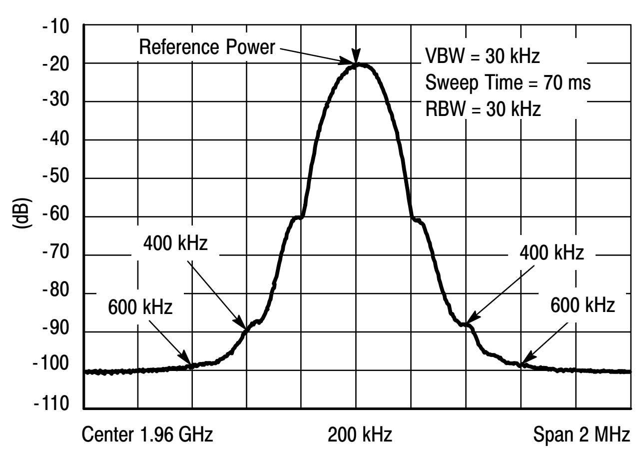
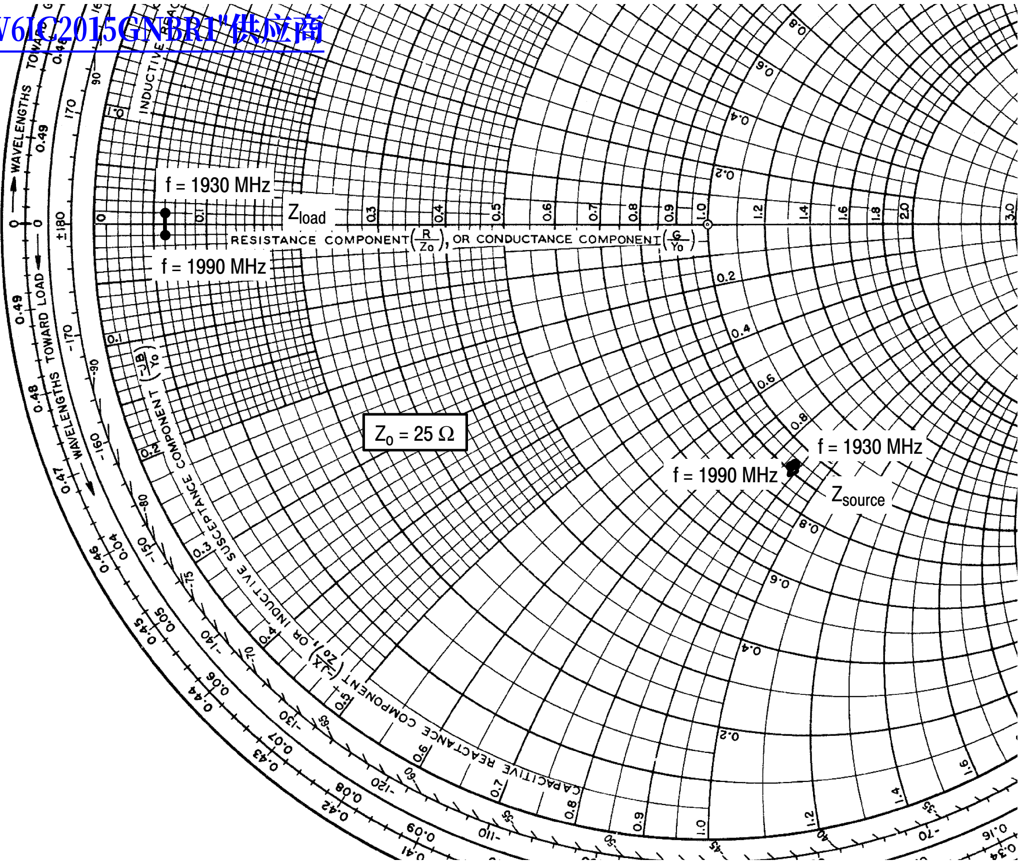


Figure 19. EDGE Spectrum



V_{DD} = 26 Vdc, I_{DQ1} = 100 mA, I_{DQ2} = 170 mA, P_{out} = 15 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
1930	23.37 - j21.93	1.62 + j0.26
1950	22.77 - j22.53	1.59 + j0.04
1970	22.19 - j22.20	1.57 - j0.16
1990	22.64 - j21.84	1.54 - j0.36

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

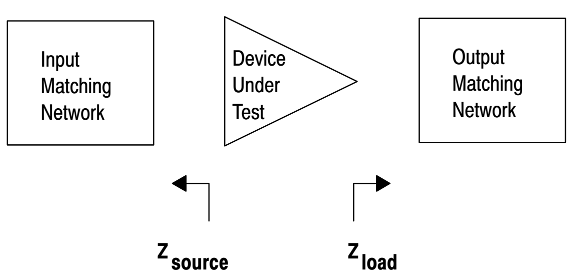
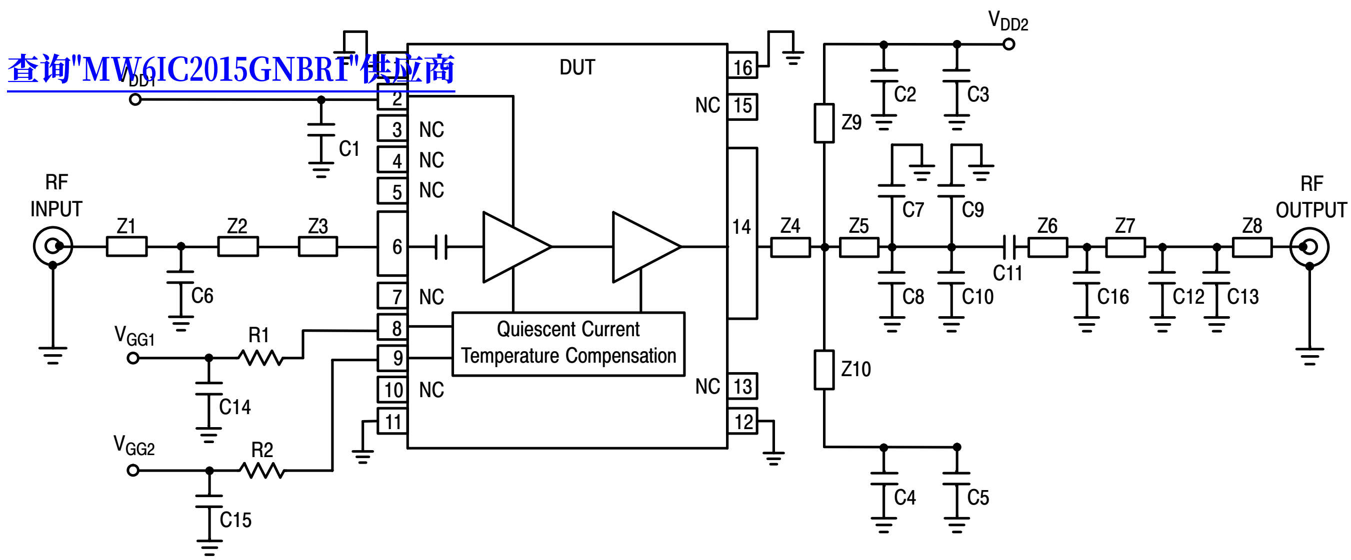


Figure 20. Series Equivalent Source and Load Impedance — 1930-1990 MHz



Z1*	1.64″ x 0.08″ Microstrip	Z7*	0.41″ x 0.04″ Microstrip
Z2	0.54″ x 0.08″ Microstrip	Z8	1.18″ x 0.04″ Microstrip
Z3	0.15″ x 0.04″ Microstrip	Z9, Z10	1.18″ x 0.08″ Microstrip
Z4	0.13″ x 0.35″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z5	0.10″ x 0.35″ Microstrip		* Variable for tuning.
Z6*	0.26″ x 0.04″ Microstrip		

Figure 21. MW6IC2015NBR1(GNBR1) Test Circuit Schematic — 1805-1880 MHz

Table 7. MW6IC2015NBR1(GNBR1) Test Circuit Component Designations and Values — 1805-1880 MHz

Part	Description	Part Number	Manufacturer
C1, C14, C15	2.2 μF Chip Capacitors	C3225X5R1H225MT	TDK
C2, C4, C11	5.6 pF Chip Capacitors	ATC100B5R6CT500XT	ATC
C3, C5	10 μF Chip Capacitors	C5750X5R1H106MT	TDK
C6	1.5 pF Chip Capacitor	ATC100A1R5BT500XT	ATC
C7, C8	2.7 pF Chip Capacitors	ATC100B2R7BT500XT	ATC
C9, C10, C12	0.8 pF Chip Capacitors	ATC100B0R8BT500XT	ATC
C13	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
C16	1 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
R1	10 kΩ, 1/4 W Chip Resistor	CRCW12061001FKTA	Vishay
R2	18 Ω, 1/4 W Chip Resistor	CRCW120618R0FKTA	Vishay

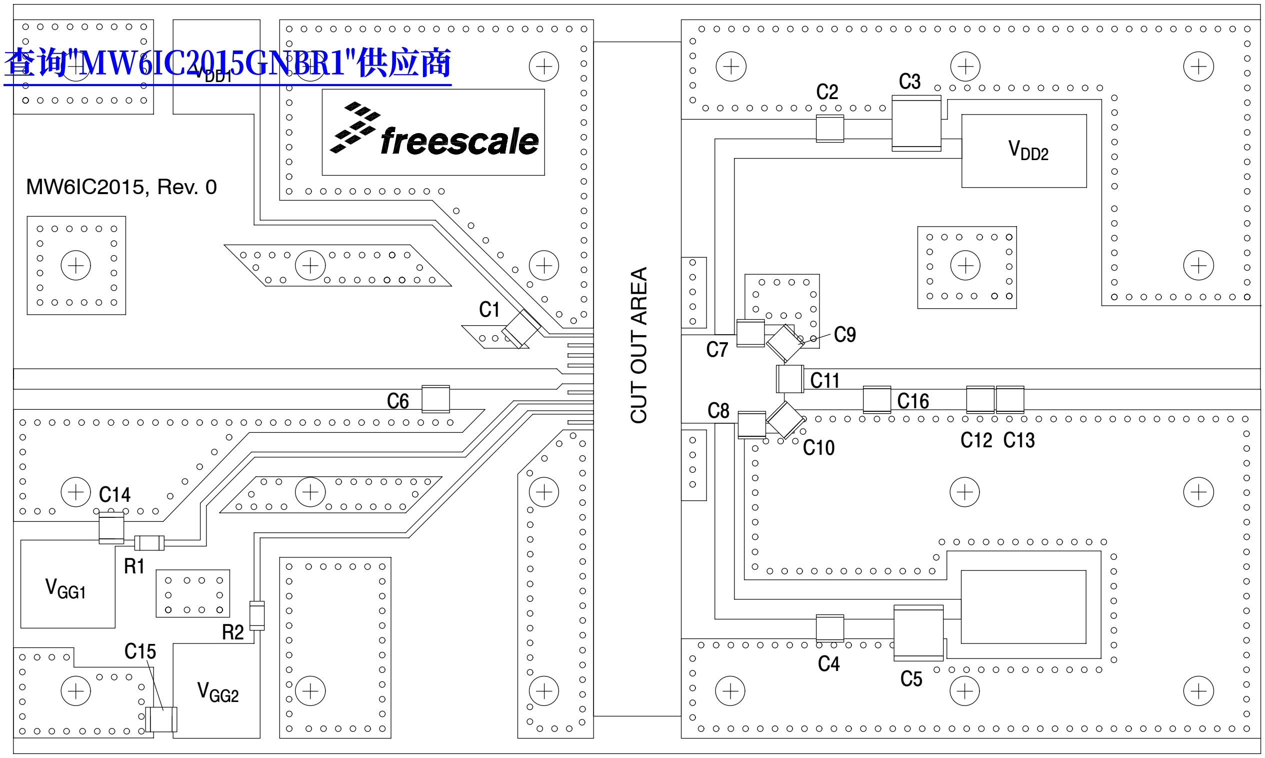


Figure 22. MW6IC2015NBR1(GNBR1) Test Circuit Component Layout — 1805-1880 MHz

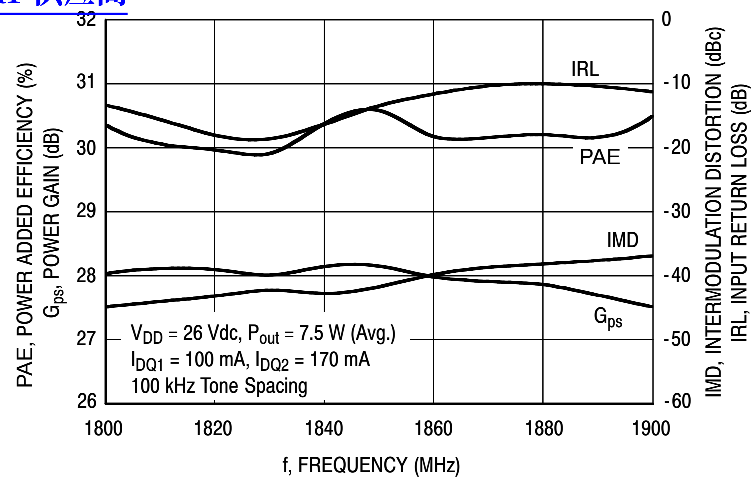


Figure 23. Two-Tone Wideband Performance @ P_{out} = 7.5 Watts Avg.

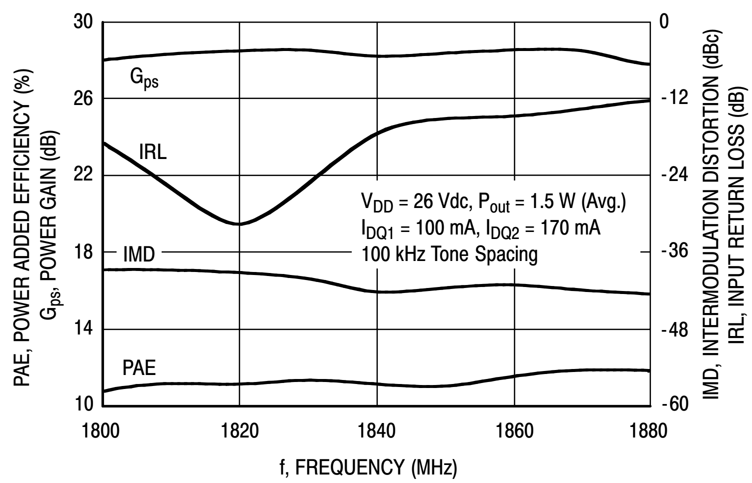


Figure 24. Two-Tone Wideband Performance @ P_{out} = 1.5 Watts Avg.

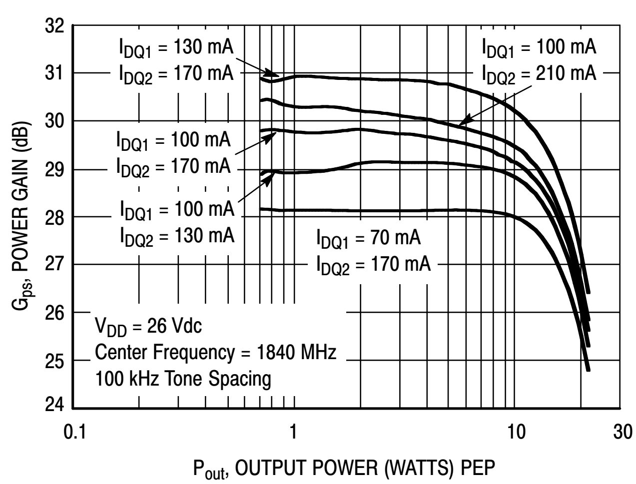


Figure 25. Two-Tone Power Gain versus Output Power

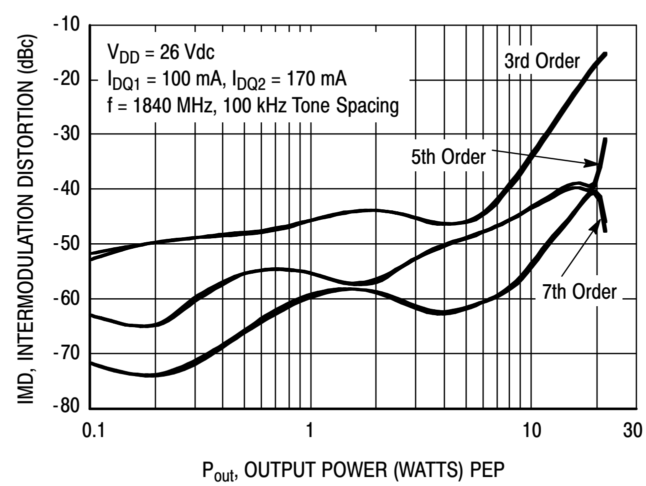


Figure 26. Intermodulation Distortion Products versus Output Power

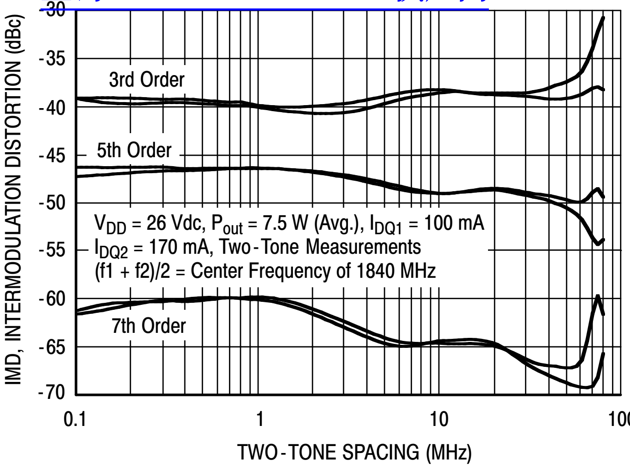


Figure 27. Intermodulation Distortion Products versus Tone Spacing

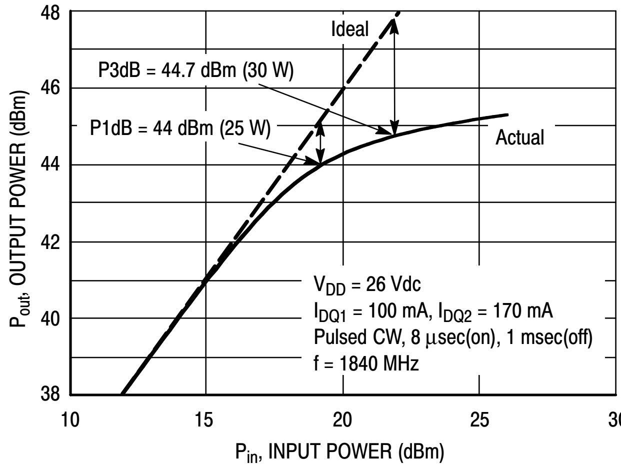


Figure 28. Pulsed CW Output Power versus Input Power

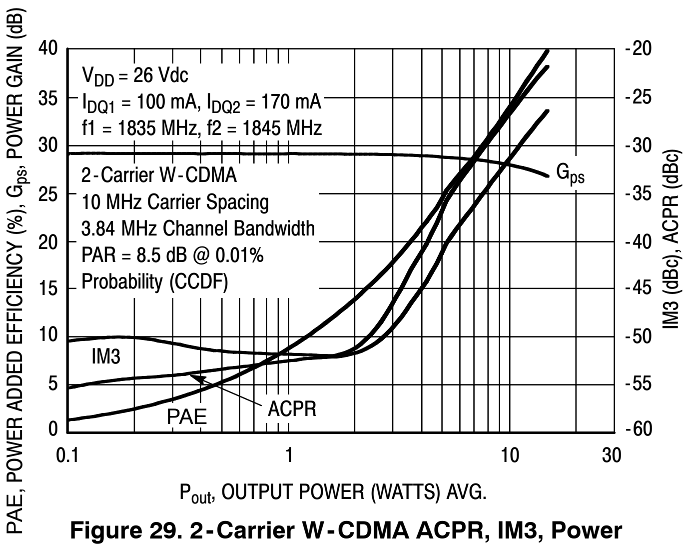


Figure 29. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Power Added Efficiency versus Output Power

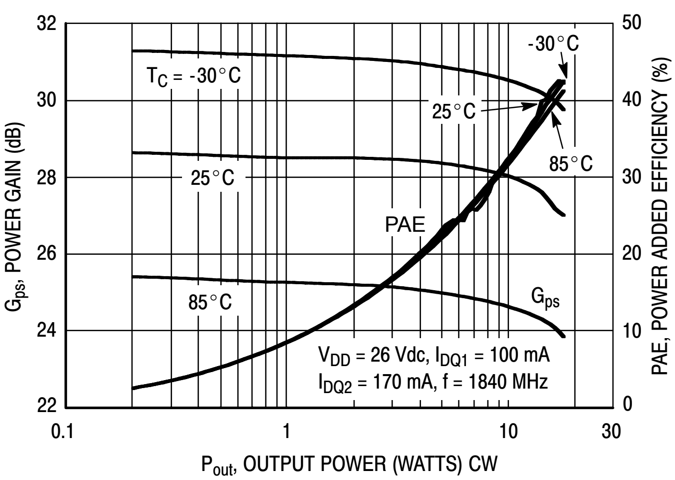


Figure 30. Power Gain and Power Added Efficiency versus CW Output Power

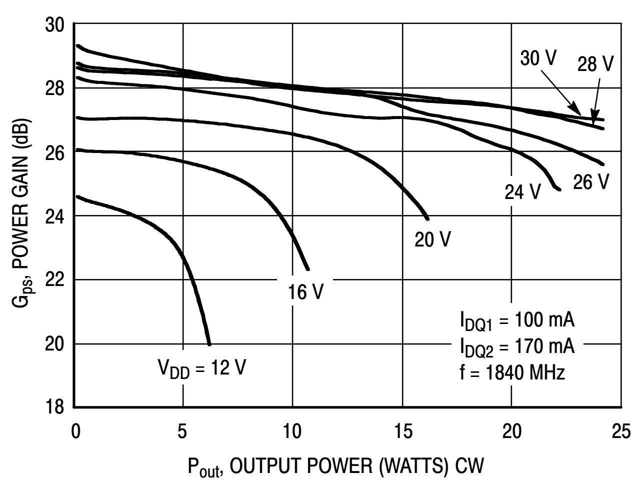


Figure 31. Power Gain versus Output Power

TYPICAL CHARACTERISTICS — 1805-1880 MHz

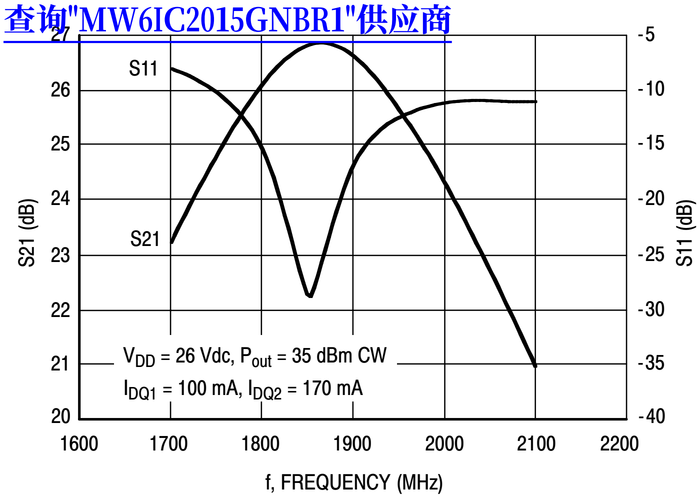


Figure 32. Broadband Frequency Response

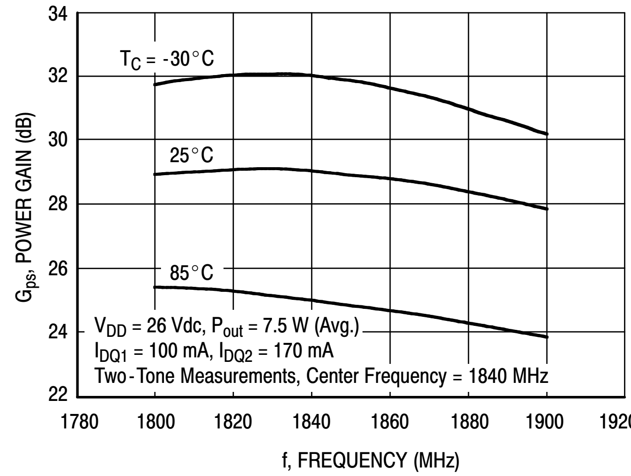


Figure 33. Power Gain versus Frequency

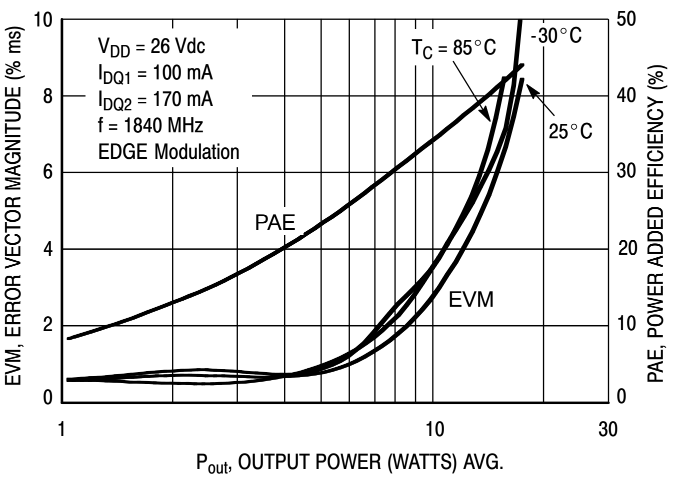


Figure 34. EVM and Power Added Efficiency versus Output Power

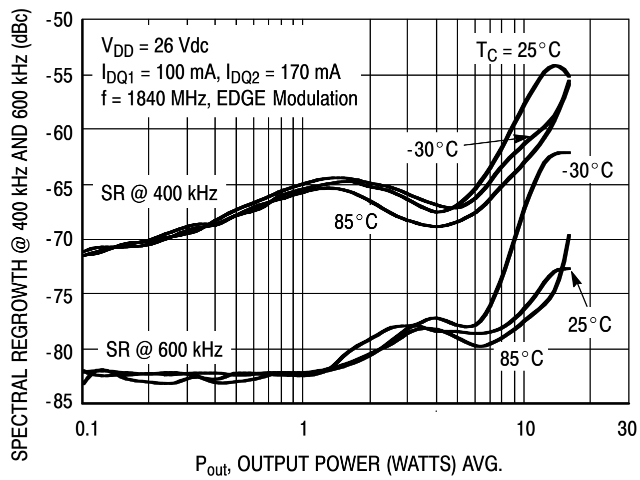
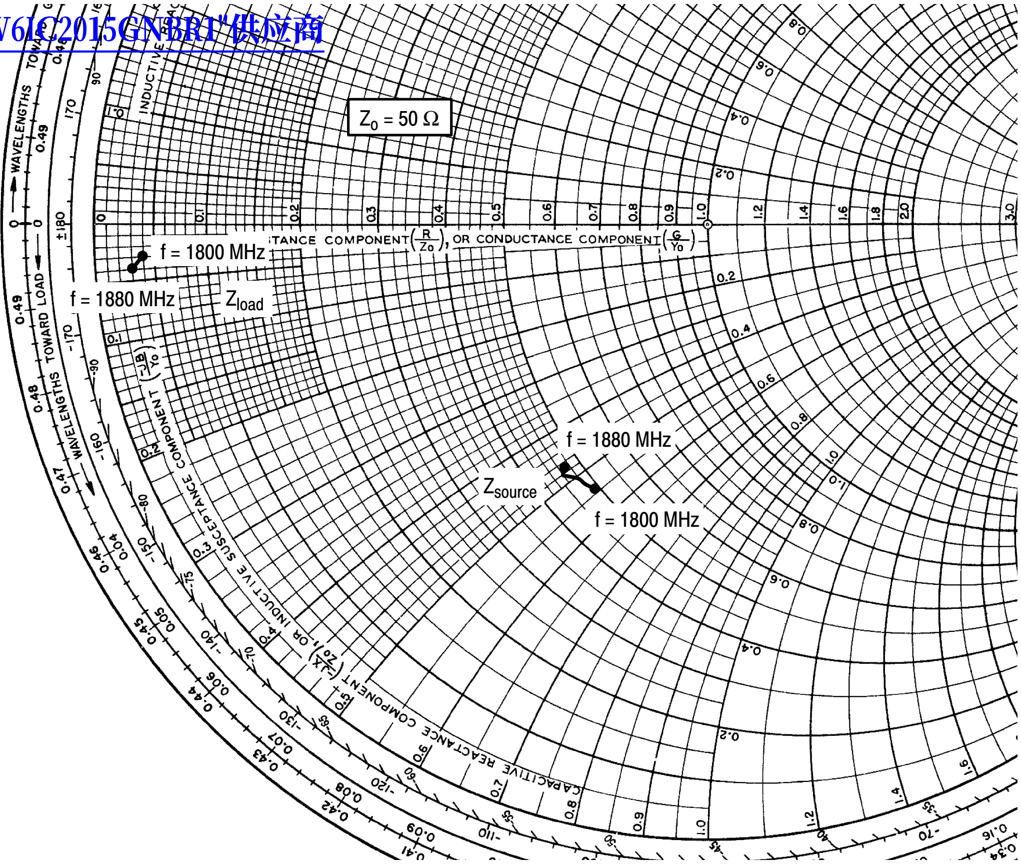


Figure 35. Spectral Regrowth at 400 and 600 kHz versus Output Power



V_{DD} = 26 Vdc, I_{DQ1} = 130 mA, I_{DQ2} = 170 mA, P_{out} = 3 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1800	24.32 - j26.99	1.94 - j1.29
1820	23.96 - j25.93	1.88 - j1.42
1840	23.86 - j25.63	1.83 - j1.54
1860	23.01 - j24.23	1.79 - j1.64
1880	23.55 - j23.33	1.74 - j1.75

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

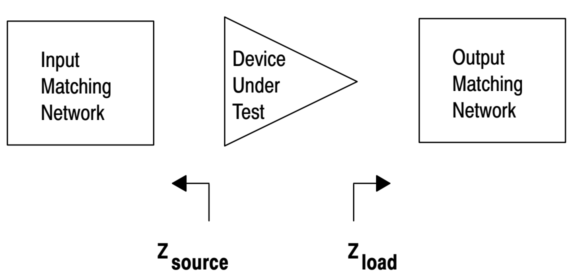
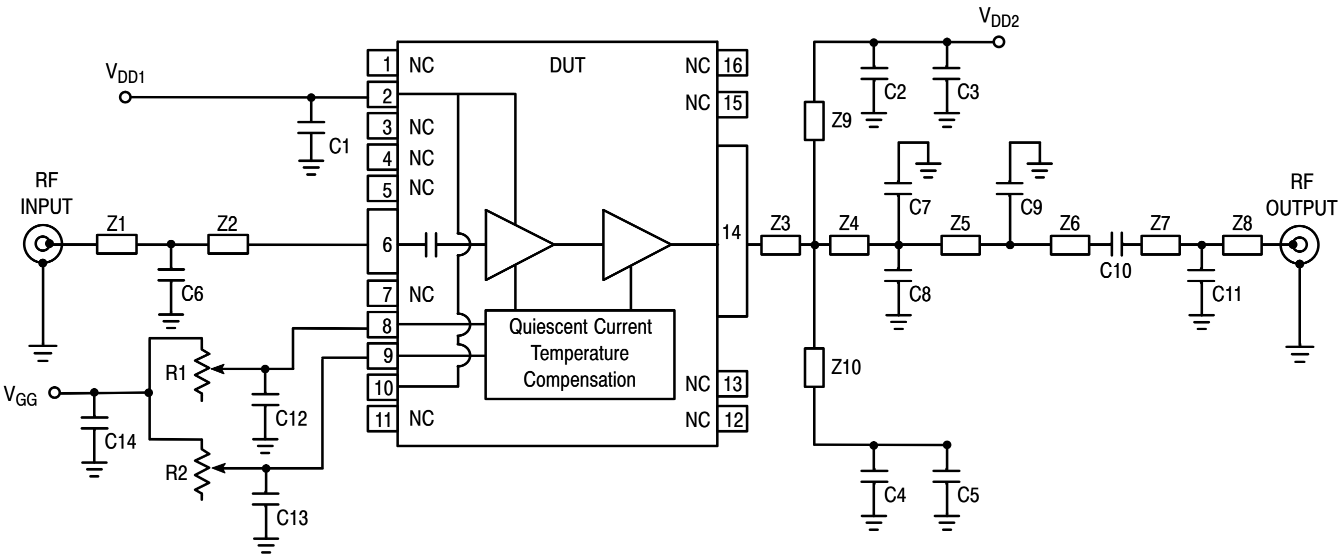


Figure 36. Series Equivalent Source and Load Impedance — 1805-1880 MHz



Z1	0.772″ x 0.056″ Microstrip	Z6	0.060″ x 0.237″ Microstrip
Z2	0.409″ x 0.056″ Microstrip	Z7	0.539″ x 0.056″ Microstrip
Z3	0.138″ x 0.237″ Microstrip	Z8	0.190″ x 0.056″ Microstrip
Z4	0.148″ x 0.237″ Microstrip	Z9, Z10	1.066″ x 0.078″ Microstrip
Z5	0.064″ x 0.237″ Microstrip	PCB	Taconic TLX8, 0.020″, ε_r = 2.55

Figure 37. MW6IC2015NBR1(GNBR1) Test Circuit Schematic — TD-SCDMA

Table 8. MW6IC2015NBR1(GNBR1) Test Circuit Component Designations and Values — TD-SCDMA

Part	Description	Part Number	Manufacturer
C1, C3, C5, C14	2.2 μF Chip Capacitors	C3225X5R1H225MT	TDK
C2, C4, C10	5.6 pF Chip Capacitors	08051J5R6CBS	ATC
C6	1 pF Chip Capacitor	08051J1R0BBS	ATC
C7, C8	2.7 pF Chip Capacitors	08051J2R7CBS	ATC
C9, C11	0.5 pF Chip Capacitors	08051J0R5BBS	ATC
C12, C13	100 nF Chip Capacitors	C1206CK104K5RC	Kemet
R1, R2	5 kΩ Potentiometer CMS Cermet Multi-turn	3224W	Bourns

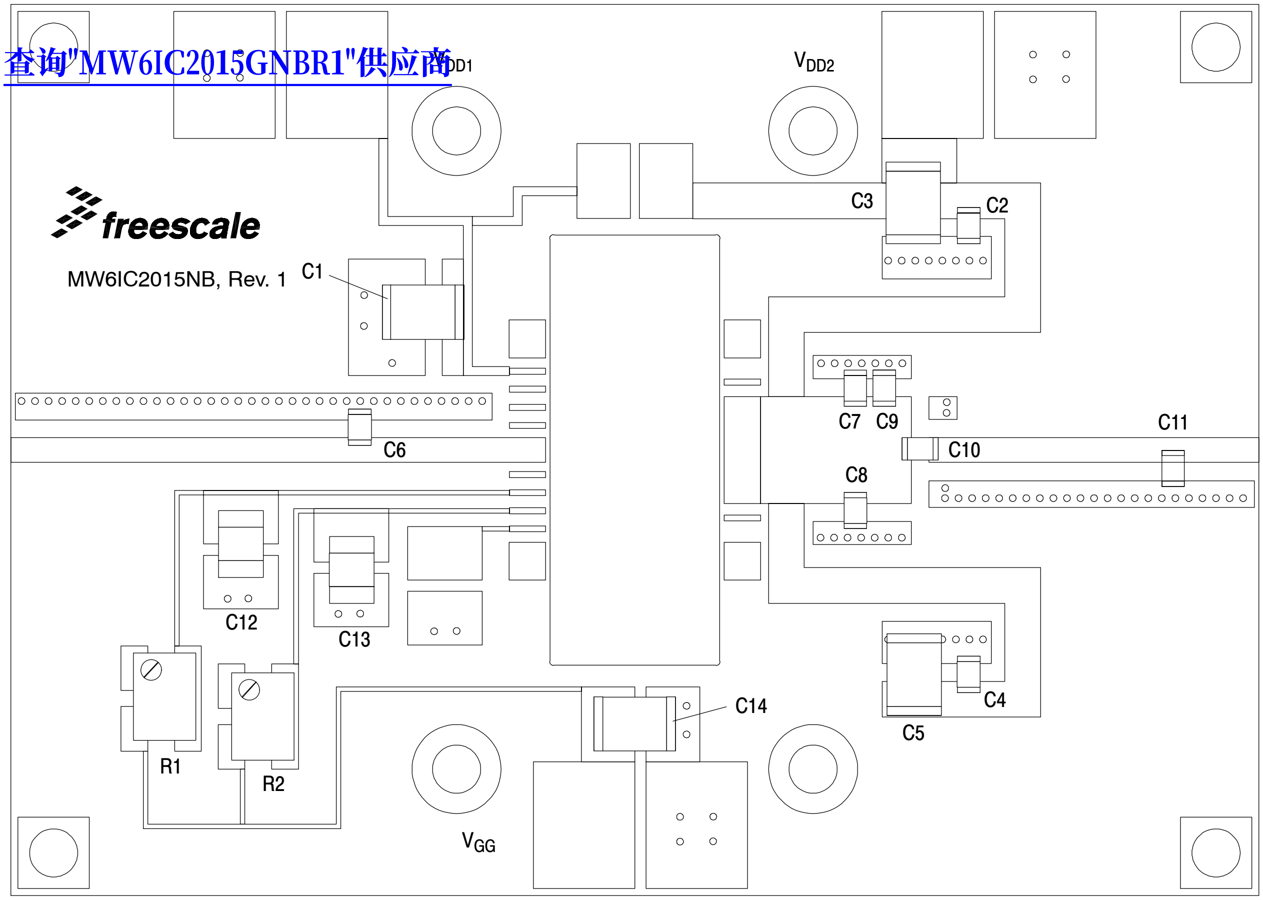


Figure 38. MW6IC2015NBR1(GNBR1) Test Circuit Component Layout — TD-SCDMA

TYPICAL CHARACTERISTICS

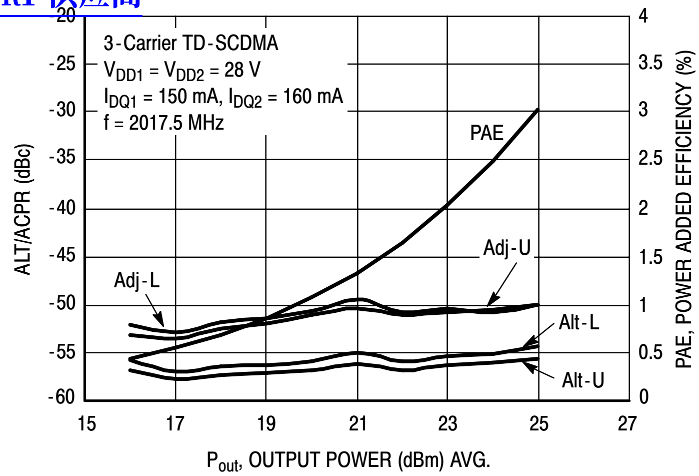


Figure 39. 3-Carrier TD-SCDMA ACPR, ALT and Power Added Efficiency versus Output Power

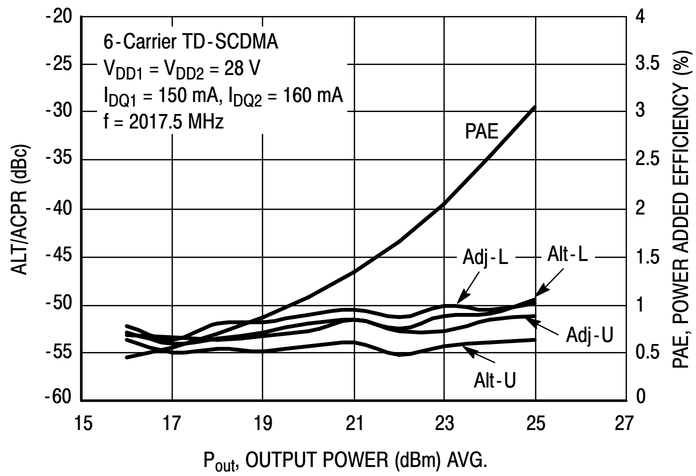


Figure 40. 6-Carrier TD-SCDMA ACPR, ALT and Power Added Efficiency versus Output Power

TD-SCDMA TEST SIGNAL

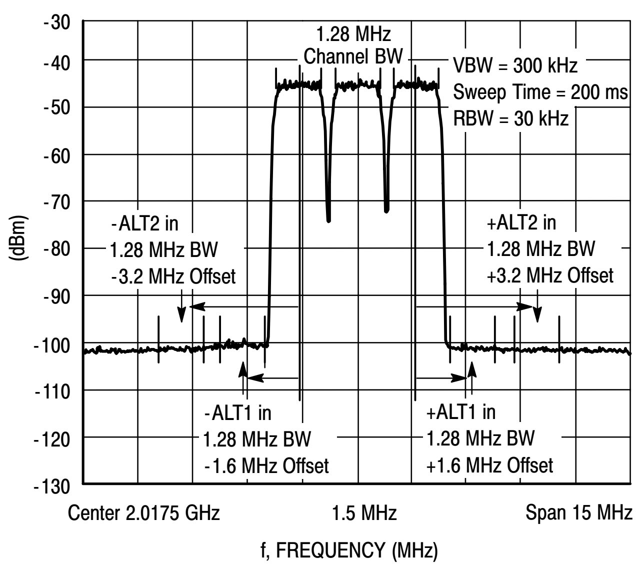


Figure 41. 3-Carrier TD-SCDMA Spectrum

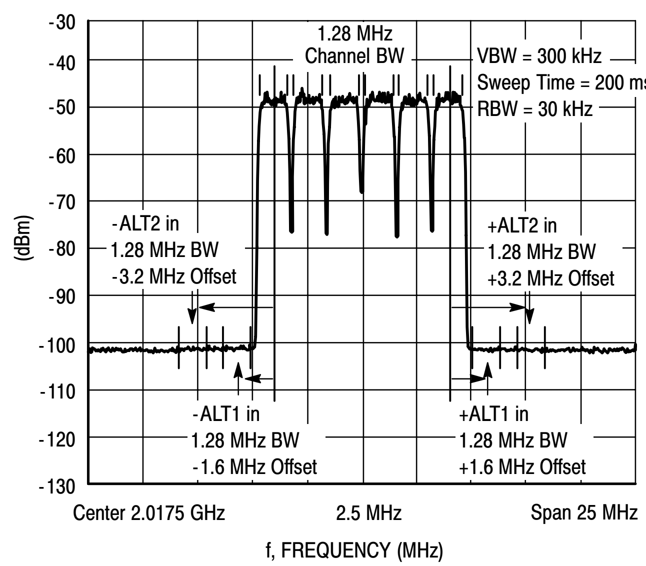
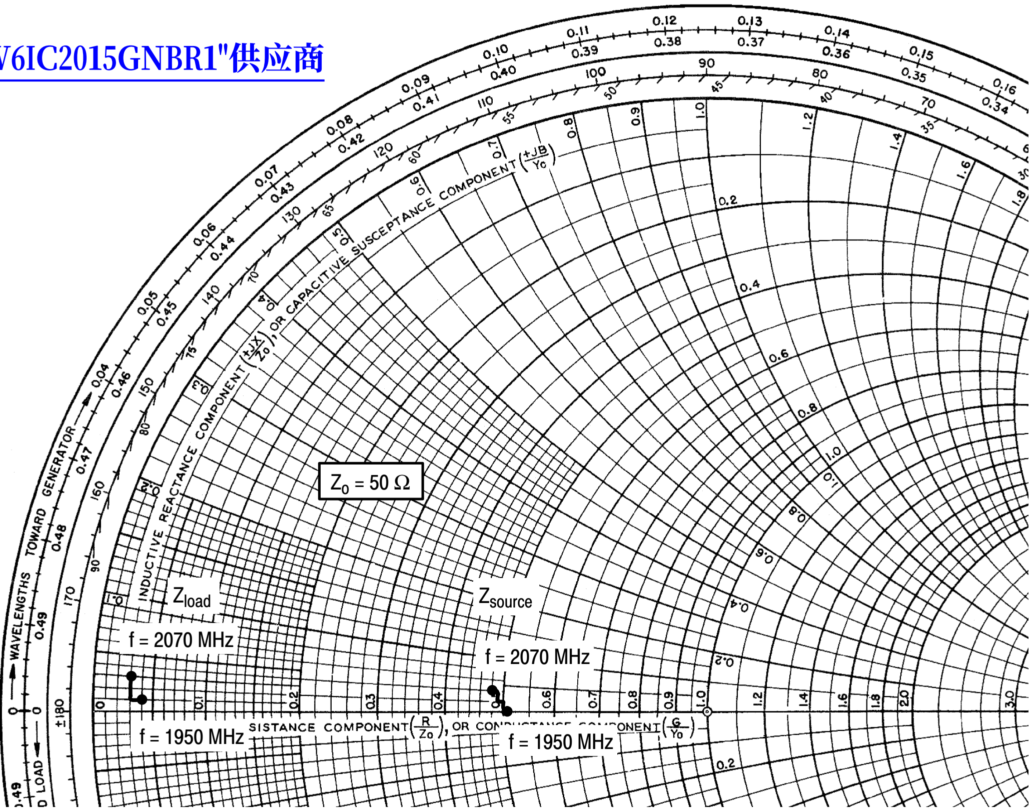


Figure 42. 6-Carrier TD-SCDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ1} = 150 mA, I_{DQ2} = 160 mA

f MHz	Z_{source} Ω	Z_{load} Ω
1950	25.25 + j0.19	1.78 + j0.33
1960	25.16 + j0.34	1.75 + j0.43
1970	25.07 + j0.49	1.72 + j0.54
1980	24.98 + j0.64	1.68 + j0.67
1990	24.89 + j0.79	1.65 + j0.78
2000	24.80 + j0.94	1.63 + j0.89
2010	24.71 + j1.09	1.62 + j1.00
2020	24.63 + j1.25	1.61 + j1.09
2030	24.54 + j1.40	1.58 + j1.19
2040	24.45 + j1.56	1.55 + j1.31
2050	24.37 + j1.71	1.50 + j1.43
2060	24.28 + j1.87	1.48 + j1.62
2070	24.20 + j2.03	1.46 + j1.65

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

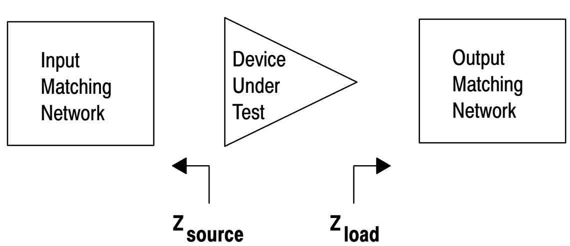
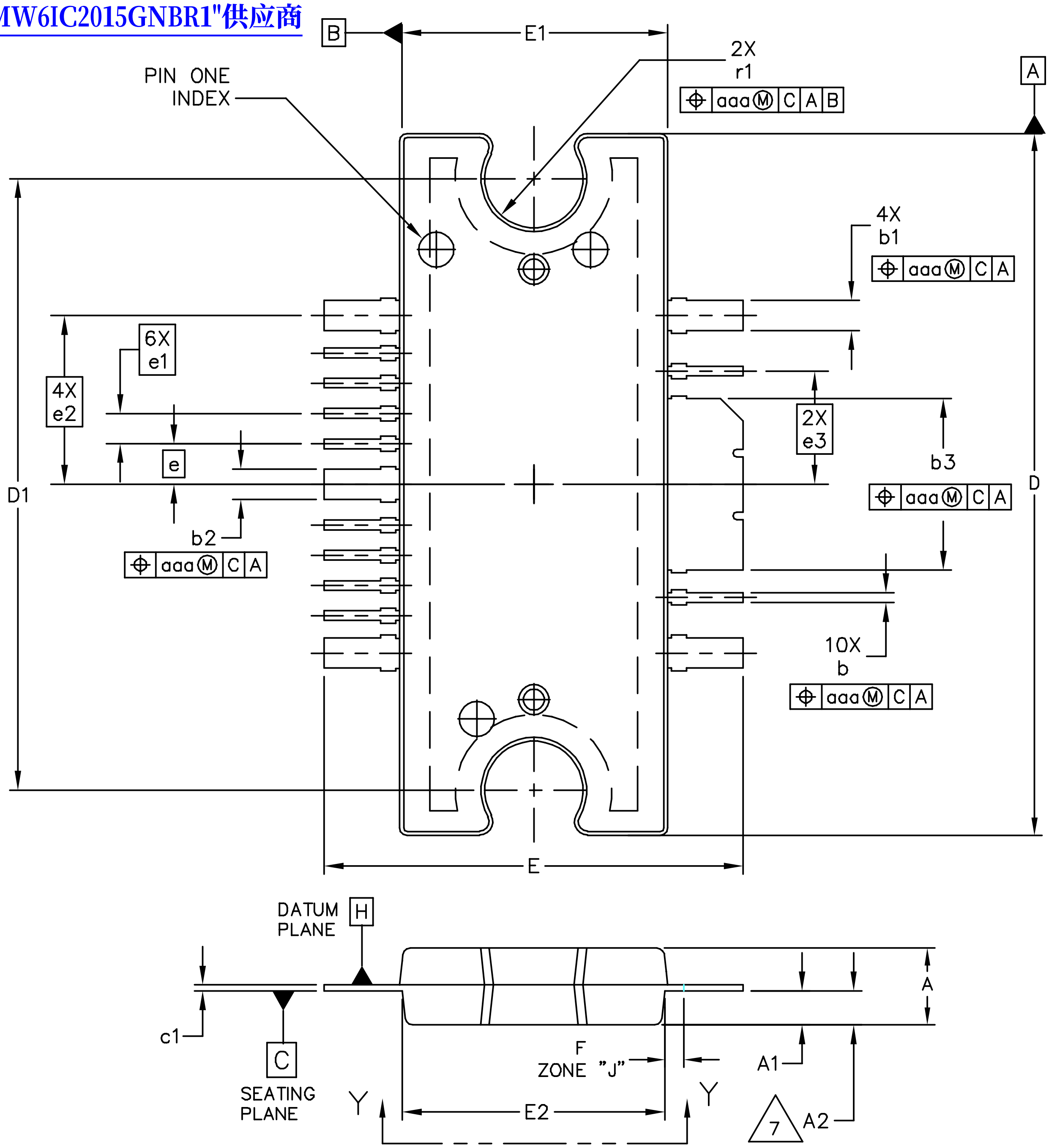


Figure 43. Series Equivalent Input and Load Impedance — TD-SCDMA

PACKAGE DIMENSIONS

查询"MW6IC2015GNBR1"供应商



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	CASE NUMBER: 1329−09	13 MAR 2006
	STANDARD: NON−JEDEC	

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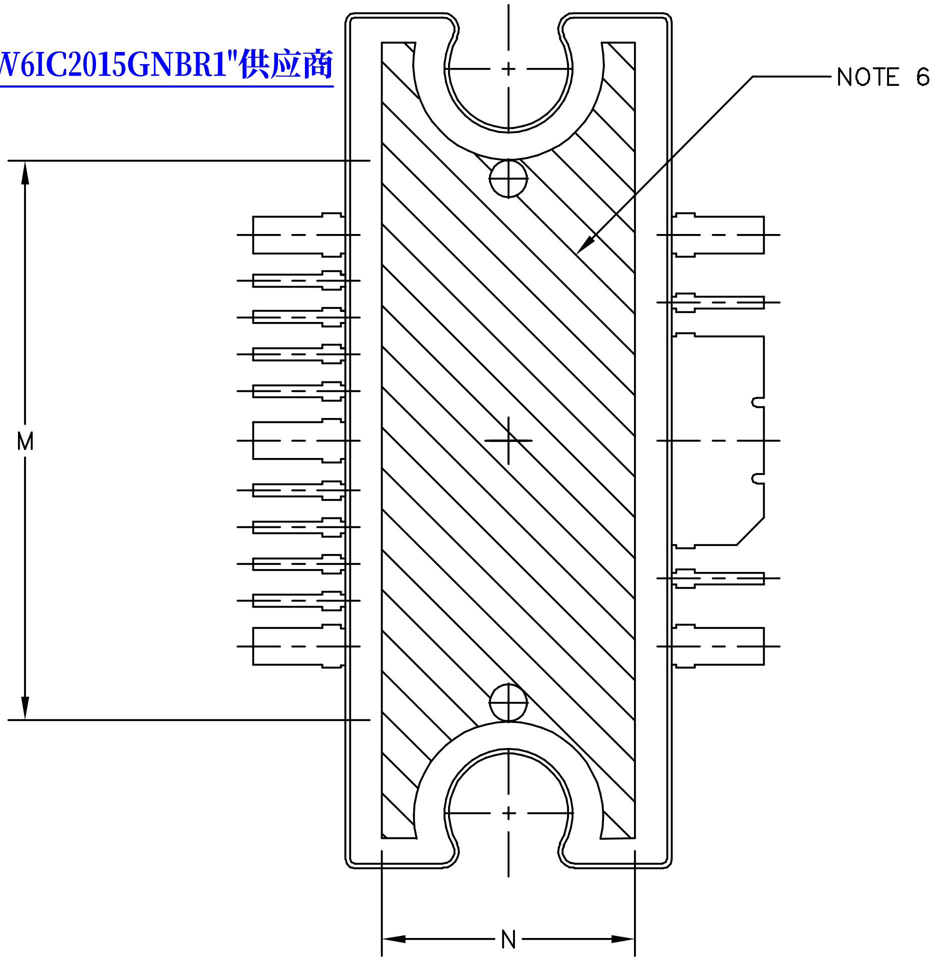

VIEW Y–Y

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	CASE NUMBER: 1329–09	13 MAR 2006
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----					
					aaa	.004		.10	

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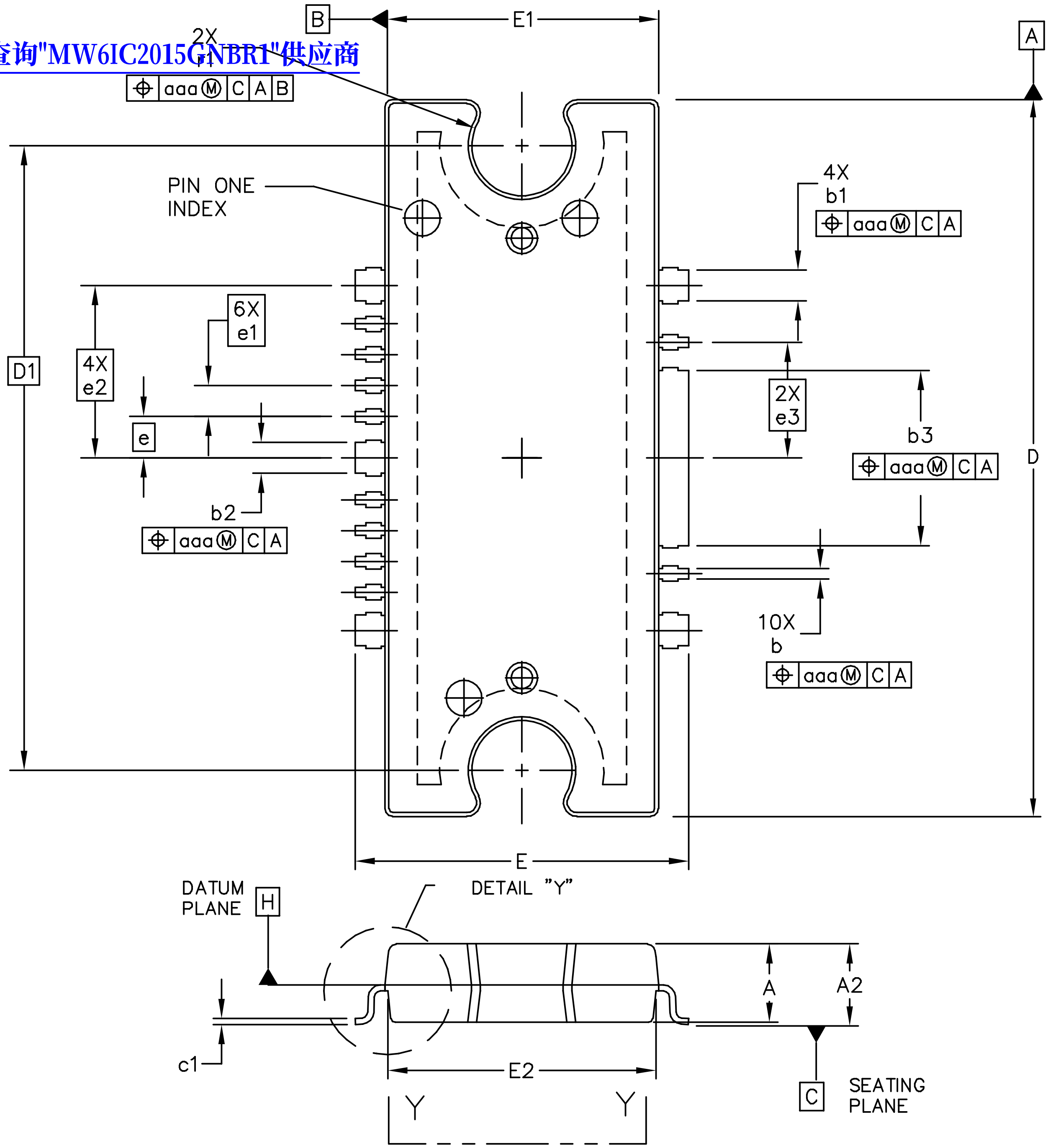
	STANDARD: NON–JEDEC	



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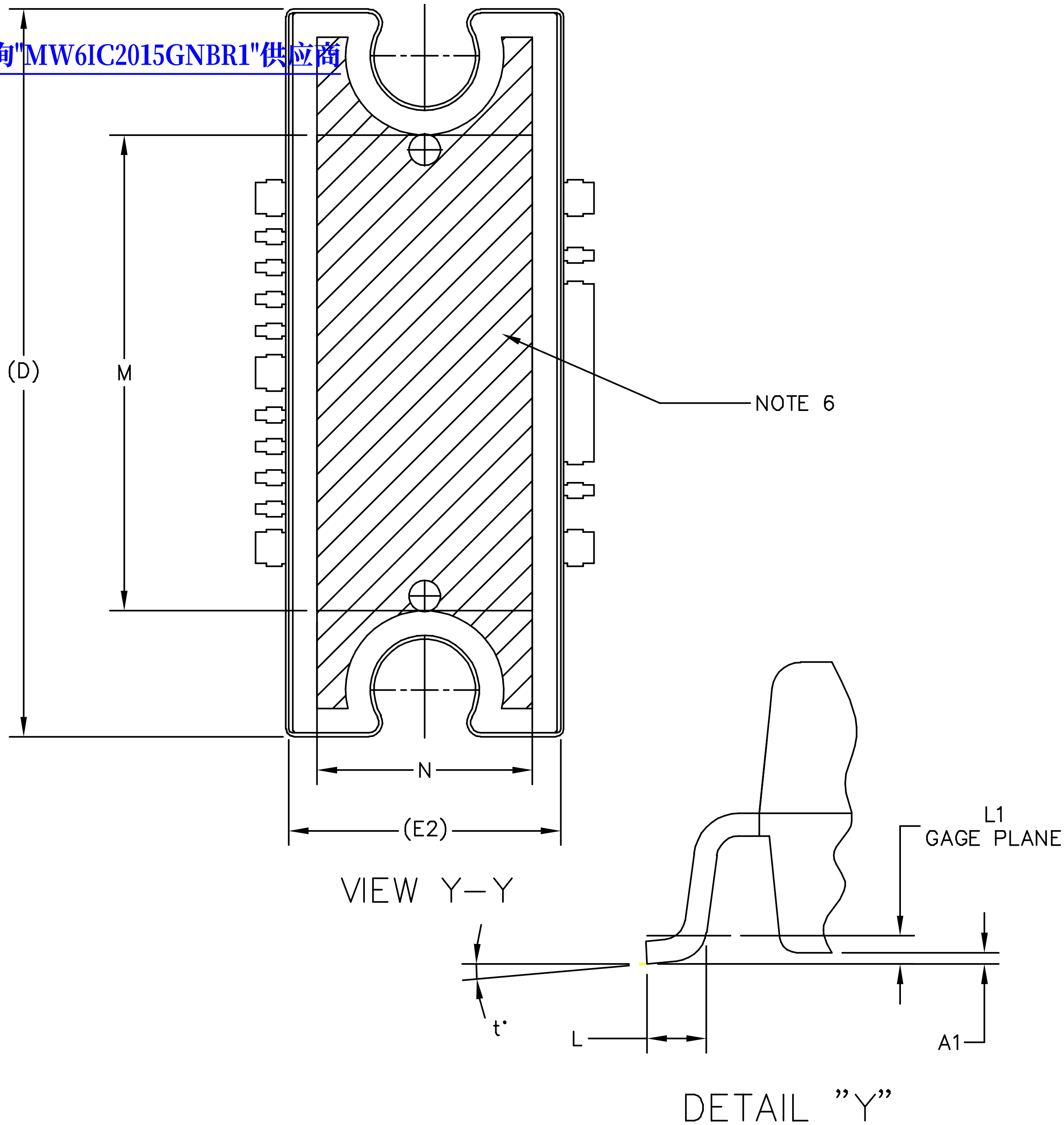
		CASE NUMBER: 1329A–03	3 APR 2006
		STANDARD: NON–JEDEC	



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	CASE NUMBER: 1329A–03	3 APR 2006
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

3. DATUM PLANE —H— IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE —H—.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.001	.004	0.02	0.10	b1	.037	.043	0.94	1.09
A2	.099	.110	2.51	2.79	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
L	.018	.024	4.90	5.06	e3	.150 BSC		3.81 BSC	
L1	.01 BSC		.025 BSC		r1	.063	.068	1.6	1.73
M	.600	----	15.24	----	t	2°	8°	2°	8°
N	.270	----	6.86						
				____	aaa	.004		.10	

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TITLE: TO—272WB, 16 LEAD GULL WING PLASTIC	DOCUMENT NO: 98ASA10532D	REV: E
	CASE NUMBER: 1329A—03	3 APR 2006
	STANDARD: NON—JEDEC	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
2	Feb. 2007	• Added "and TD-SCDMA" to data sheet description paragraph, p. 1. • Updated verbiage on Typical Performances table, p. 2 • Corrected V_{BIAS} and V_{SUPPLY} callouts, Figs. 3 and 21, Test Circuit Schematic, p. 4, 11, Figs. 4 and 22, Test Circuit Component Layout, p. 5, 12 • Updated Part Numbers in Tables 6 and 7, Component Designations and Values, to RoHS compliant part numbers, p. 4, 11 • Adjusted scale for Figs. 7 and 25, Two-Tone Power Gain versus Output Power, Figs. 8 and 26, Intermodulation Distortion Products versus Output Power, Figs. 11 and 29, 2-Carrier W-CDMA ACPR, IM3, Power Gain and Power Added Efficiency versus Output Power, Figs. 12 and 30, Power Gain and Power Added Efficiency versus CW Output Power, Figs. 16 and 34, EVM and Power Added Efficiency versus Output Power, Figs. 17 and 35, Spectral Regrowth at 400 and 600 kHz versus Output Power, to better match the device's capabilities, p. 6-8, 13-15 • Replaced Figure 18, MTTF versus Junction Temperature with updated graph. Removed $Amps^2$ and listed operating characteristics and location of MTTF calculator for device, p. 9 • Corrected Series Impedance data table test conditions, Figs. 20 and 36, p. 10, 16 • Added TD-SCDMA test circuit schematic, component designations and values, component layout, typical characteristic curves, test signal and series impedance, p. 17-20. • Added Product Documentation and Revision History, p. 27

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