



SANYO Semiconductors

DATA SHEET

LA74310LP — Monolithic Linear IC

Audio Interface for DSC + Video Driver

Overview

The LA74310LP is an AV interface IC for digital still cameras (DSCs). It incorporates all the functions necessary for analog audio signal processing for microphone and loudspeaker amplifiers. It also incorporates video output drivers that require no output coupling capacity. The IC is ideal for reducing the number of components and further miniaturization of digital still cameras.

Features

■ AUDIO INTERFACE block

- Three-wire type SERIAL communication • MIC AMP, MIC power supply incorporated (with built-in pull-up resistor)
- ALC
- PB input method: Analog or digital for inputting ($\Delta\Sigma$) signal
- 3rd order LPF (for REC/PB switching control, option of $f_c=4\text{kHz}$ or 11kHz)
- SPEAKER AMP (The BEEP signal can be mixed.), with electronic VOLUME (controlled by Serial communication)
- LINE output (with SERIAL MUTE)
- STANDBY control (current drain $< 10\mu\text{A}$)

■ VIDEO DRIVER block

- Not requires output coupling capacity
- Low voltage drive ($V_{CC}=2.7\text{V}$ to 3.6V)
- V sag does not occur
- 6th order LPF ($f_c=9\text{MHz}$) is built-in.
- $0\mu\text{A}$ current dissipation on standby mode.
- 3 ways amplifier gains (6, 12, 16dB) can be selected. (Pin control (GND/Open/ V_{CC}))
- The video output has the capacity where one load of 75Ω impedance can be driven.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LA74310LP

Specifications"供应商

Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		4.0	V
Allowable power dissipation	Pd max	Ta≤80°C *	550	mW
Operating temperature	Topr		-10 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

* Substrate mounting condition (40mm × 50mm × 0.8mm: glass epoxy) 2S2P (Four layers substrate)

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		3.1	V
	V _{CCA}		3.0	V
	V _{CCSP}		3.3	V
Allowable operating voltage range	V _{CC}		2.7 to 3.6	V
	V _{CCA}		2.7 to 3.6	V
	V _{CCSP}	Take care not to exceed Pd max.	2.7 to 3.6	V

Electrical Characteristics of AUDIO Block at Ta=25°C, V_{CCA}=3.0V, V_{CCSP}=3.3V, f=1kHz, with the VREF capacitance charging circuit in the OFF MODE

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current						
V _{CCA} current dissipation at no signal 1	I _{CCA1}	V _{CCA} =3.0V	7	9.4	11.8	mA
V _{CCA} current dissipation at no signal 2	I _{CCA2}	V _{CCA} =3.0V: REC BLOCK (MIC/ALC/REC AMP) POWER SAVE MODE	5	6.7	8.4	mA
V _{CCA} current dissipation at no signal 3	I _{CCA3}	V _{CCA} =3.0V: LINE AMP POWER SAVE MODE	6.5	8.7	10.9	mA
V _{CCA} standby current dissipation	I _{CCAS}	V _{CCA} =3.0V: during standby control (23PIN=0V application)			1	μA
Current dissipation at no signal 5	I _{CCSP1}	V _{CCSP} =3.3V: SPK POWER ON MODE	1.2	2.5	5	mA
Current dissipation at no signal 6	I _{CCSP2}	V _{CCSP} =3.3V: SPK POWER SAVE MODE		0.05	0.1	mA
V _{CCSP} standby current dissipation	I _{CCSPS}	V _{CCSP} =3.3V: during standby control (23PIN=0V application)		5.5	10	μA
REC output system						
REC reference output LEVEL	VOR	ALC IN, V _{IN} =-49dBV	-16.5	-15.5	-14.5	dBV
REC reference output distortion	HDR	ALC IN, V _{IN} =-49dBV, THD: from 2nd to 5th harmonic		0.05	0.1	%
ALC characteristics 1	ALM1	ALC IN, V _{IN} =-33dBV (standard+16dB)	-11	-8	-5	dBV
ALC distortion 1	ALMD1	ALC IN, V _{IN} =-33dBV (standard+16dB), THD: from 2nd to 5th harmonic		0.15	0.5	%
ALC characteristics 2	ALM2	ALC IN, V _{IN} =-17dBV (standard+32dB)	-11	-8	-5	dBV
ALC distortion 2	ALMD2	ALC IN, V _{IN} =-17dBV (standard+32dB), THD: from 2nd to 5th harmonic		0.2	1	%
ALC IN max input level	VINRMX	ALC IN LEVEL at which REC output THD (from 2nd to 5th harmonic) becomes 3% or less.			-10	dBV
REC output noise voltage	VNOR	ALC IN, no input, JIS-A Filter		-77	-68	dBV
REC output frequency characteristics 1	FEQR1	ALC IN, V _{IN} =-33dBV, comparison of f=4kHz/1kHz	-5	-3.5	-2	dB
REC output frequency characteristics 2	FEQR2	ALC IN, V _{IN} =-33dBV, comparison of f=22kHz/1kHz		-33	-25	dB
REC output frequency characteristics 3	FEQR3	ALC IN, V _{IN} =-33dBV, comparison of f=100kHz/1kHz		-60	-55	dB

Continued on next page.

LA74310LP

Continued from preceding page.

[查询"LA74310LP"供应商](#)

查看 LA-4310LP 供应网

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LINE output system						
LINE reference output LEVEL	VOL	PB IN, $V_{IN}=-15\text{dBV}$	-12	-11	-10	dBV
LINE reference output distortion rate	HDL	PB IN, $V_{IN}=-15\text{dBV}$, THD: from 2nd to 5th harmonic		0.1	0.2	%
LINE reference output noise voltage	VNOL	PB IN, no input, JIS-A Filter		-85	-77	dBV
PB IN max input LEVEL	VINPMX	PB IN LEVEL at which LINE output THD (from 2nd to 5th harmonic) becomes 3% or less.			-5	dBV
LINE output frequency characteristics 1	FEQP1	PB IN, $V_{IN}=-8\text{dBV}$, comparison of $f=4\text{kHz}/1\text{kHz}$	-5	-3.5	-2	dB
LINE output frequency characteristics 2	FEQP2	PB IN, $V_{IN}=-8\text{dBV}$, comparison of $f=22\text{kHz}/1\text{kHz}$		-33	-25	dB
LINE output frequency characteristics 3	FEQP3	PB IN, $V_{IN}=-8\text{dBV}$, comparison of $f=100\text{kHz}/1\text{kHz}$		-65	-60	dB
LINE output level ($\Delta\Sigma$ mode)	VIDVOL	PB IN, PWM signals, digital input MODE (see supplements: p.8 Note26)	-13	-11.5	-10	dBV
SP output system (SP load = as measured at both ends of 8Ω)						
SP reference output LEVEL1 (Vol.MAX)	VOSP1	PB IN, $V_{IN}=-15\text{dBV}$, Vol=MAX (Serial DATA=31)	-5	-2	1	dBV
SP reference output distortion	THDSP	PB IN, $V_{IN}=-15\text{dBV}$, Vol=MAX, THD: from 2nd to 5th harmonic		0.4	1	%
SP reference output LEVEL2 (Vol.TYP)	VOSP2	PB IN, $V_{IN}=-15\text{dBV}$, Vol=TYP (Serial DATA=17)	-19	-13	-7	dBV
SP reference output LEVEL3 (Vol.MIN)	VOSP3	PB IN, $V_{IN}=-15\text{dBV}$, Vol=MIN (Serial DATA=0), JIS-A Filter		-80	-70	dBV
SP reference output noise voltage	VNOSP	PB IN, no input, Vol=MAX, JIS-A Filter		-76	-70	dBV
SP maximum ratings output	VOMSP	PB IN, Vol=MAX, LEVEL at which THD=10%	200	340		mW
MIC output system						
MIC voltage gain	VGMIC	MIC IN, $V_{IN}=-39\text{dBV}$	19	20	21	dB
MIC output distortion	HDMIC	MIC IN, $V_{IN}=-39\text{dBV}$, THD: from 2nd to 5th harmonic		0.02	0.1	%
MIC output noise voltage	VNOMIC	MIC IN, no input, JIS-A Filter		-94	-83	dBV
MIC IN max input level	VINMMX	MIC IN LEVEL at which the MIC output THD (from 2nd to 5th harmonic) becomes 3% or less.			-22	dBV
MIC V_{CC} output voltage	VMIC	At $6.2\text{k}\Omega$ load	1.5	1.7	1.9	V
Control system						
Serial CLOCK frequency	FCLK			1.25	1.5	MHz
Serial input LOW level	SERLO		0		0.7	V
Serial input HIGH level	SERHI		2.3		3.5	V

LA74310LP

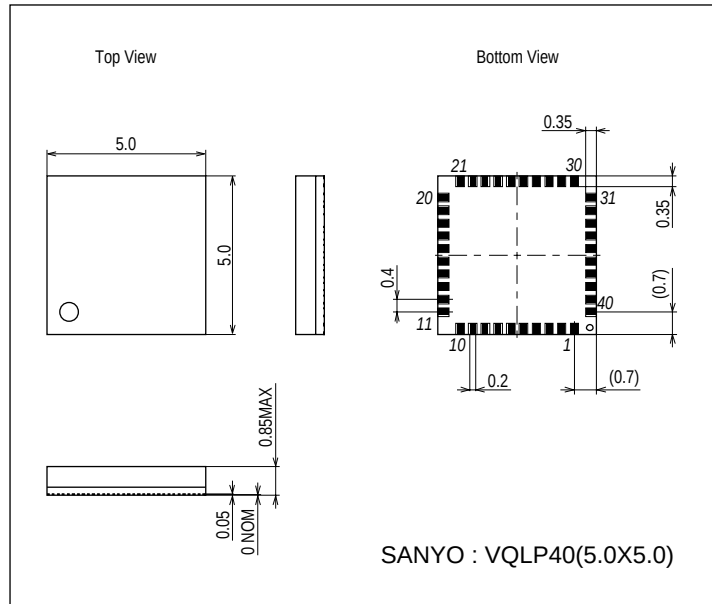
Electrical Characteristics of VIDEO Block at Ta=25°C, V_{CC}=3.1V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current						
V _{CC} current dissipation 1 (V _{IN} =White50%)	I _{CC}	Input=White50%, 34PIN=Low	14	22	30	mA
V _{CC} current dissipation 2 (Non-signal mode)	I _{CC2}	Input=no input, 34PIN=Low	7	11.5	15	mA
V _{CC} current dissipation 3 (Standby mode)	I _{CC-Stby}	34pin=Open (High)		0	5	μA
VIDEO block						
Voltage gain V6	Vg-L	V _{IN} =1Vpp 100% White, 32PIN=Low (GND)	5.7	6.2	6.7	dB
Voltage gain V12	Vg-M	V _{IN} =0.5Vpp 100% White, 32PIN=MID (Open)	11.7	12.2	12.7	dB
Voltage gain V16	Vg-H	V _{IN} =0.317Vpp 100% White, 32PIN=High (V _{CC})	15.7	16.2	16.7	dB
Frequency characteristics	Vf	f=100kHz/5MHz	-1.5	-0.5	+0.5	dB
DG / Differential Gain	Dg	V _{OUT} =2Vpp (Modulated Ramp)	-2.0	0.0	+2.0	%
DP / Differential Phase	Dp	V _{OUT} =2Vpp (Modulated Ramp)	-2.0	0.0	+2.0	Deg
Control pin block						
Standby control pin H voltage (SET=STANDBY MODE)	Vth-Stby-H	Voltage range of the pin 34 to achieve I _{CC} ≤5μA	V _{CC} -0.5		V _{CC}	V
Standby control pin L voltage (SET=ACTIVE MODE)	Vth-Stby-L	Voltage range of the pin 34 to achieve active mode	GND		0.3	V
Gain selection control pin H voltage (SET=16dB)	Vth-G-H	Voltage range of the pin 32 to achieve an amp. gain of 16dB	V _{CC} -0.3		V _{CC}	V
Gain selection control pin M voltage (SET=12dB)	Vth-G-M	Voltage range of the pin 32 to achieve an amp. gain of 12dB	1.0	1.2 (Open)	1.4	V
Gain selection control pin L voltage (SET=6dB)	Vth-G-L	Voltage range of the pin 32 to achieve an amp. gain of 6dB	GND		0.3	V

Package Dimensions

unit : mm (typ)

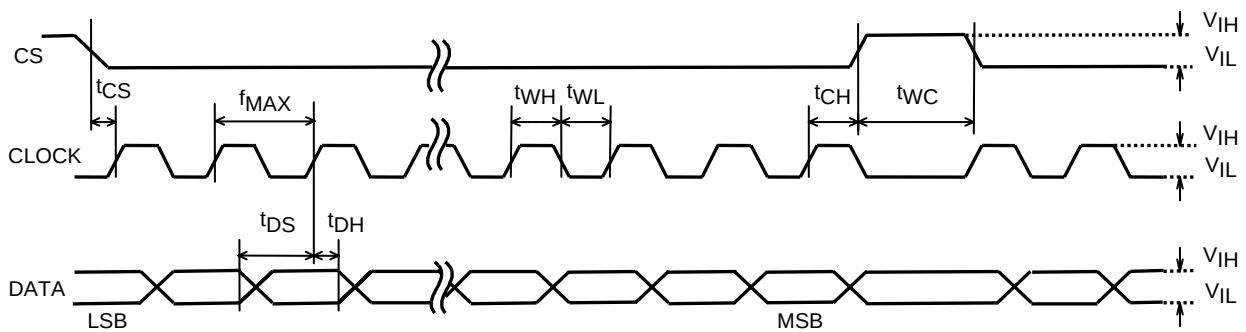
3302A



Description of the Content of Serial Communication

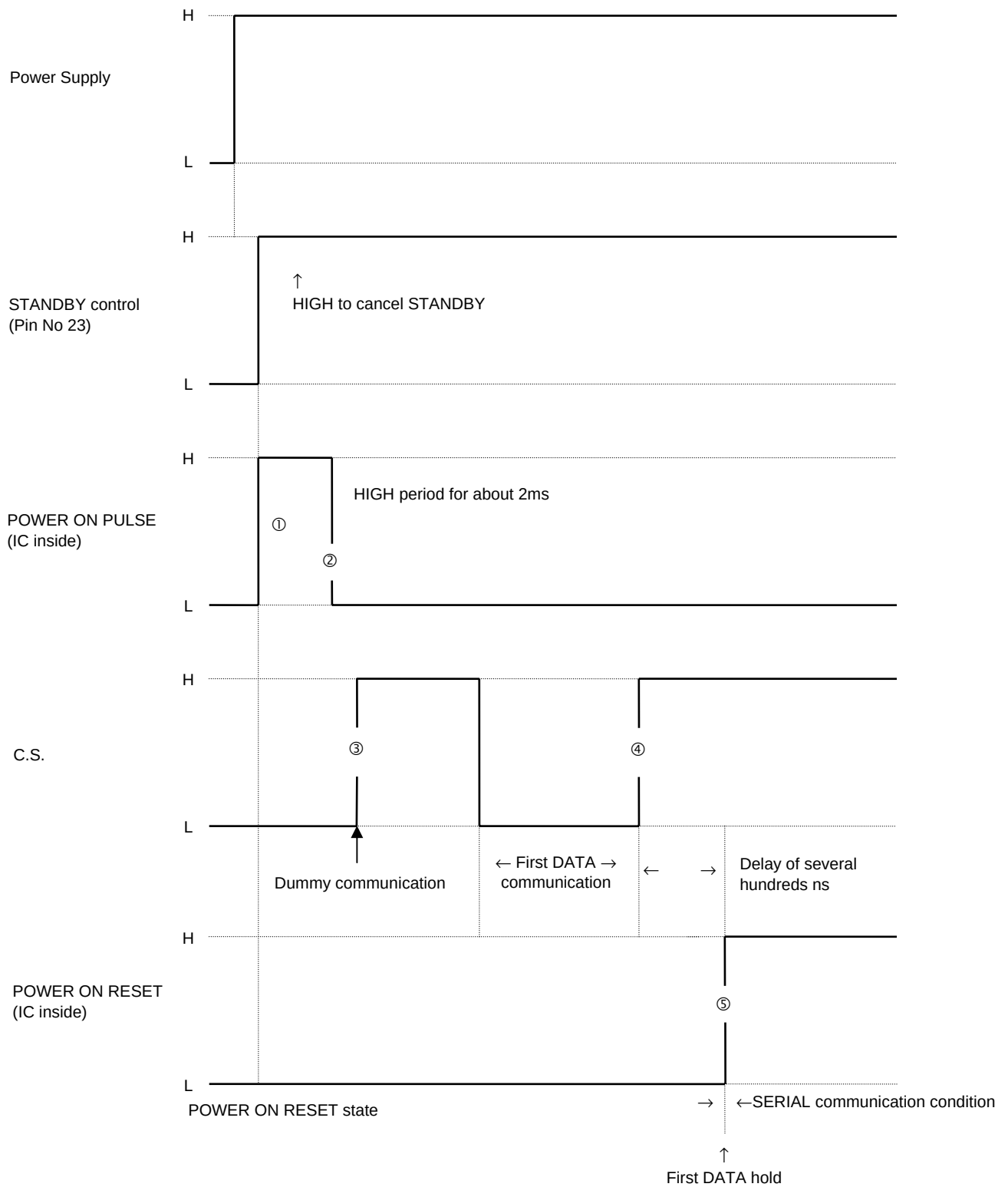
DATA No.	Parameter	Default
0	DUMMY	0
1	LPF Cut-off frequency SW	0:11kHz, 1:4kHz
2	VREF capacitor charging circuit control SW	0:ON, 1:OFF
3	MIC AMP POWER SW	0:ON, 1:OFF
4	ALC AMP POWER SW	0:ON, 1:OFF
5	LPF1 MODE SW	0:PB MODE1, 1:REC MODE
6	LPF1/LPF2 selection SW	0:LPF1, 1:LPF2
7	REC BLOCK POWER SW	0:ON, 1:OFF
8	LINE OUT POWER SW	0:ON, 1:OFF
9	LINE MUTE SW	0:ON, 1:OFF
10	SPK POWER SW	0:ON, 1:OFF
11	DATA=1	1 1 1 1 1: VOL MAX
12	DATA=2	to
13	DATA=4	0 0 0 0 0: VOL MIN (MUTE)
14	DATA=8	* EVR setting (the numeral shown in the left is decimal.
15	DATA=16	For characteristics, see P12.)

Serial Transmission Timing



- | | | |
|-------------|----------------------------|---------------|
| • f_{MAX} | (Max clock frequency) | 1.5MHz |
| • t_{WL} | (Clock pulse width: Low) | 333ns or more |
| • t_{WH} | (Clock pulse width: High) | 333ns or more |
| • t_{CS} | (Chip enable setup time) | 333ns or more |
| • t_{CH} | (Chip enable hold time) | 333ns or more |
| • t_{DS} | (Data setup time) | 333ns or more |
| • t_{DH} | (Data hold time) | 333ns or more |
| • t_{WC} | (Chip enable pulse width) | 333ns or more |
| • V_{IH} | (High voltage lower limit) | 2.3V to 3.5V |
| • V_{IL} | (Low voltage upper limit) | 0V to 0.7V |

POWER ON Condition (SERIAL communication)



The POWER ON RESET state covers a period up to the rise ④ of the second C.S. input after fall ② of POWER ON PULSE ① generated inside IC when the power is applied and the STANDBY control is canceled. ③ is the dummy communication.

Actually, because of delay of several hundreds ns in the IC, the first DATA condition begins in ⑤ and the normal SERIAL communication condition begins after ⑤.

LA74310LP

Method of Measuring Electric Characteristics of AUDIO Block at Ta=25°C, V_{CC}L=3.0V, V_{CC}SP=3.3V, f=1kHz VREF capacitor charging circuit OFF MODE

No.	Symbol	Input		Output	STANDBY pin	Serial control setting																		
		Pin	Conditions	Pin		Major conditions (for the serial control setting, see the table in the right)																		
						0	1	2	3	4	5	6		7	8	9	10	11	12	13	14	15		
					Voltage applied to pin 23	DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW (1.~)REC	(0.0);PB Analog	(0.1);PB Digital	REC P SW	LINE P SW	LINE Mute	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA		
						*	0:1kHz 1:4kHz	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF			0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON
						*																		
Circuit current																								
1	ICCA1	29	VCCA=3.0V No input	29	VREF capacitance charging circuit in the OFF MODE	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0		
2	ICCA2	29	VCCA=3.0V No input	29	VREF capacitance charging circuit in the OFF MODE MICALC REC AMP POWER SAVE MODE	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0		
3	ICCA3	29	VCCA=3.0V No input	29	VREF capacitance charging circuit in the OFF MODE LINE AMP POWER SAVE MODE	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
4	ICCA5	29	VCCA=3.0V No input	29	With the STANDBY pin (23PIN)=0V	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
5	ICCS1	16	VCCSP=3.3V No input	16	VREF capacitance charging circuit in the OFF MODE SPK AMP ON MODE	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
6	ICCS2	16	VCCSP=3.3V No input	16	VREF capacitance charging circuit in the OFF MODE SPK AMP POWER SAVE MODE	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0		
7	ICCSPS	16	VCCSP=3.3V No input	16	With the STANDBY pin (23PIN)=0V	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
REC output system																								
8	VOR	7	VIN=-49dBV f=1kHz	5	400 to 20kHz LPF used	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
9	HDR1	7	VIN=-49dBV f=1kHz	5	400 to 20kHz LPF used THD: from 2nd to 5th harmonic	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
10	ALM1	7	VIN=-33dBV f=1kHz	5	400 to 20kHz LPF used	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
11	ALMD1	7	VIN=-33dBV f=1kHz	5	400 to 20kHz LPF used THD: from 2nd to 5th harmonic	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
12	ALM2	7	VIN=-17dBV f=1kHz	5	400 to 20kHz LPF used	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
13	ALMD2	7	VIN=-17dBV f=1kHz	5	400 to 20kHz LPF used THD: from 2nd to 5th harmonic	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
14	VINRMX	7	f=1kHz	5 & 7	400 to 20kHz LPF used Pin 7 level at which pin 5 becomes THD = 3% (from 2nd to 5th harmonic)	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
15	VNOR	7	No input	5	JIS-A FILTER used	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
16	FEQR1	7	VIN=-33dBV f=4kHz	5	f=4kHz/1kHz level ratio	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
17	FEQR2	7	VIN=-33dBV f=22kHz	5	f=22kHz/1kHz level ratio	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		
18	FEQR3	7	VIN=-33dBV f=100kHz	5	f=100kHz/1kHz level ratio	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0		

查询"LA74310LP"供应商

No.	Symbol	Input		Output	STANDBY pin	Serial control setting																																																																																																																																																																																																																																																																																																																																																																																			
		Pin	Conditions	Pin		Major conditions (for the serial control setting, see the table in the right)	Voltage applied to pin 23	0	1	2	3	4	5		6	7	8	LINE P SW	Mute	SPK P SW	EVR1 DATA	12	13	14	15																																																																																																																																																																																																																																																																																																																																																																
													LPF C SW	CHRG P SW												MIC P SW	ALC P SW	LPF MODESW (1.):REC	REC P SW	LINE P SW	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON																																																																																																																																																																																																																																																																																																																																																				
																																						* 0:11kHz 1:4kHz	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF	* 0:ON 1:OFF

Supplements: (Note 26) The line out signal level shall be VIDVOL when inputting the PWM waveform in Figure 26 into the pin 2.

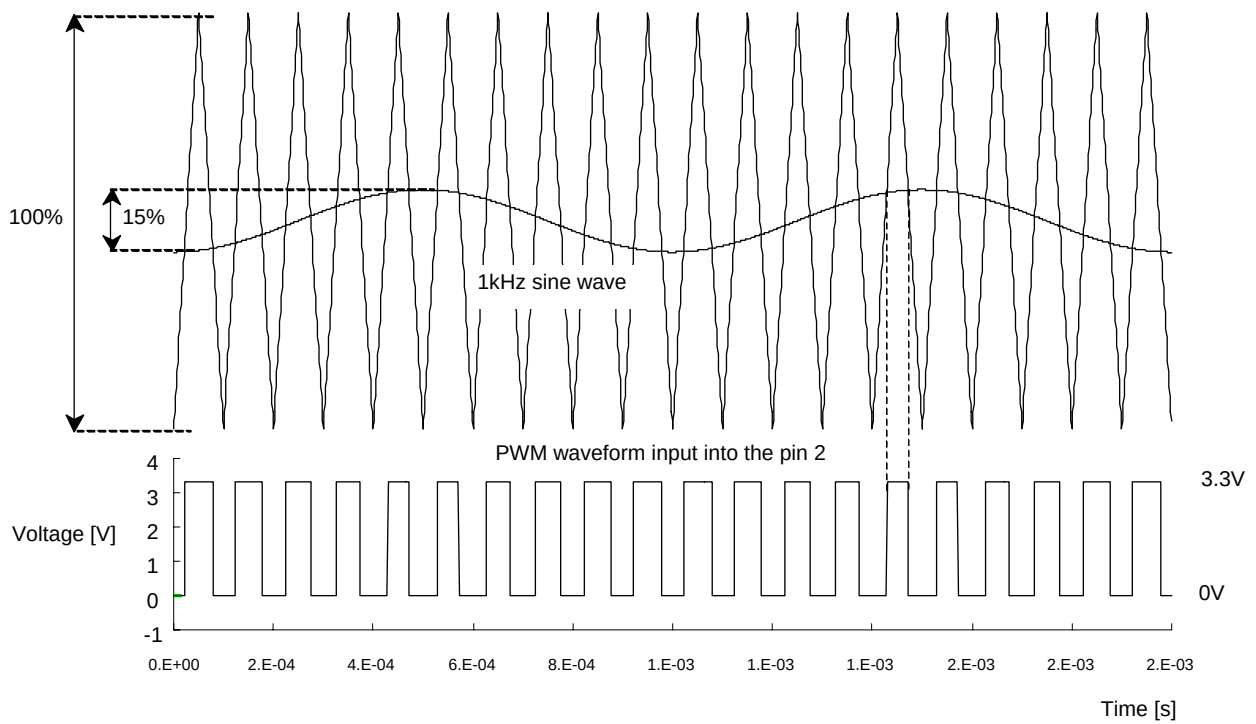
[查询"LA74310LP"供应商](#)

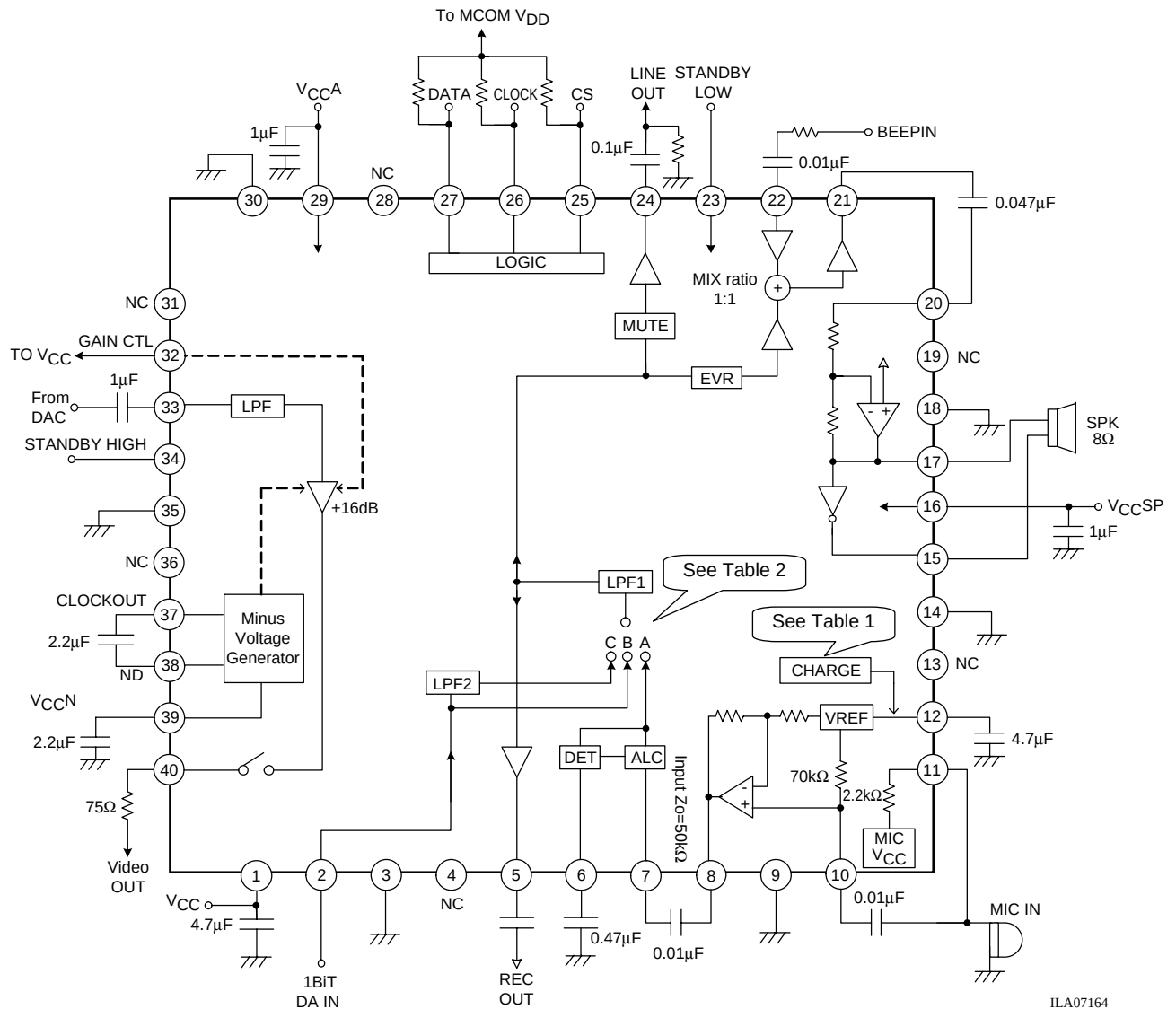
Figure 26. PWM waveform input into the pin 2 when measuring VIDVOL

LA74310LP

Description of Pin Functions

Pin No.	Pin Description	Pin purpose
1	V _{CC} (Power source for VIDEO)	For VIDEO
2	PB input	For AUDIO
3	A GND	For AUDIO
4	NC	
5	REC output	For AUDIO
6	ALC detection	For AUDIO
7	ALC input	For AUDIO
8	MIC output	For AUDIO
9	MIC GND	For AUDIO
10	MIC input	For AUDIO
11	INT power supply for MIC	For AUDIO
12	Ripple rejection for VREFL	For AUDIO
13	NC	
14	SPK GND	For AUDIO
15	Speaker positive-phase output	For AUDIO
16	V _{CC} SP	For AUDIO
17	Speaker negative-phase output	For AUDIO
18	SPK GND	For AUDIO
19	NC	
20	Speaker input	For AUDIO
21	MIX output	For AUDIO
22	BEEP input	For AUDIO
23	STANDBY control	For AUDIO
24	LINE output	For AUDIO
25	C.S. input	For AUDIO
26	CLOCK input	For AUDIO
27	DATA input	For AUDIO
28	NC	
29	V _{CCA}	For AUDIO
30	Analog GND	For VIDEO
31	NC	
32	Gain select pin	For VIDEO
33	Video input	For VIDEO
34	Power save mode select pin	For VIDEO
35	GND	For VIDEO
36	NC	
37	CLOCK output	For VIDEO
38	Charge transfer	For VIDEO
39	Negative V _{CC}	For VIDEO
40	Video output	For VIDEO

LA74310LP Pin Configuration, Equivalent Diagram and Recommended Circuit Diagram



ILA07164

NC PIN handling

This pin is electrically open and can be connected to GND with no problem.

However, we recommend you to make a foot pattern of a form similar to other pins to assure good balance after mounting.

Table 1: Logic of external capacitor charging circuit

SERIAL	No.2
ON	0
OFF	1

Initially "ON"

Table 2: LPF SW control logic

SERIAL	No.5	No.6
A	1	*
B	0	0
C	0	1

*) Don't care.

LA74310LP EVR characteristics

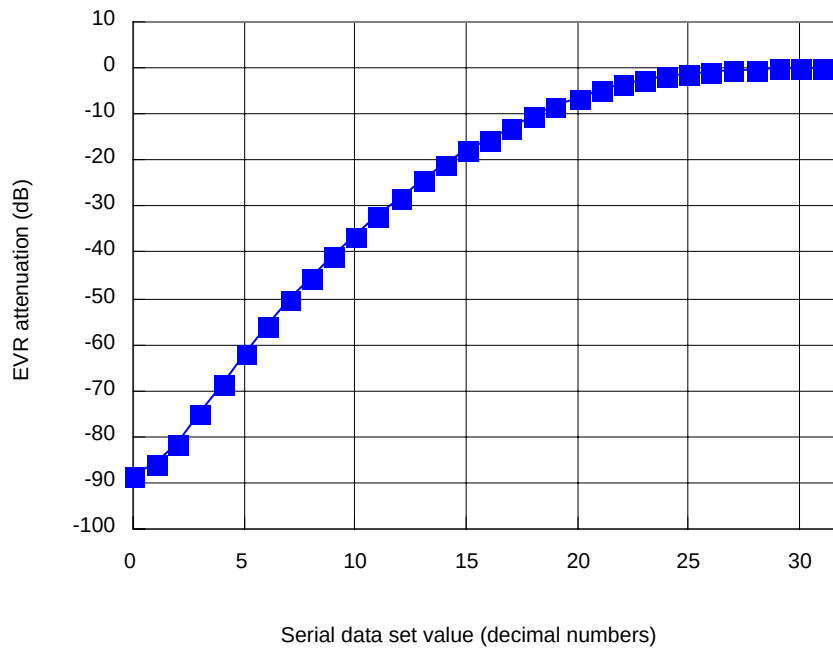


Table of Input/Output Forms of LA74310LP (Audio Block)

Pin No.	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
2	PB IN	1.64V	Reference input level =-15dBV Maximum input level = -5dBV In analog input mode = 3.465Vpp In $\Delta\Sigma$ input mode	PB input pin	
3	A GND	0V		GND pin for analog signal part	
4	NC			NC pin	
5	REC OUT	1.50V	At PB reference input Output level = -15dBV	REC output pin	

Continued on next page.

LA74310LP

Consulted from preceding page.
LA74310LP 供应商

Pin No.	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
6	ALC DET			ALC detection pin	
7	ALC IN	1.64V	At MIC reference input Output level = -49dBV Max input level =-10dBV	ALC input pin	
8	MIC OUT	1.6V	At MIC reference input Output level = -49dBV	MIC output pin	
9	MIC GND	0V		For MIC Amp blocking GND pin	
10	MIC IN	1.64V	Reference input level =-69dBV Maximum input level =-30dBV	MIC input pin	
11	MIC VCC	2.30V		MIC power pin	

Continued on next page.

LA74310LP

Consulted from preceding page.
LA74310LP 供应商

Pin No.	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
12	VREFL	2.30V		MIC V_{CC} and VREFL ripple rejection pin	
13	NC			NC pin	
14	SP GND	0V		Speaker GND pin	
15	SPK OUT+	1.27V	At PB reference input Output level = -8dBV (EVR MAX)	Speaker positive-phase output pin	
16	V_{CCSP}	3.3V		Speaker power pin	
17	SP OUT-	1.27V	At PB reference input Output level = -8dBV (EVR MAX)	Pin for output of speaker reversed phase	
20	SPK IN	1.27V	At PB reference input Output level = -8dBV (EVR MAX)	Speaker input pin	
18	SP GND	0V		Speaker GND pin	
19	NC			NC pin	
21	MIX OUT	1.58V	At PB reference input Output level = -8dBV	EVR output pin	
22	BEEP IN	1.64V	Maximum input level = -8dBV		

Continued on next page.

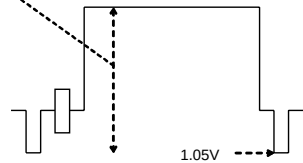
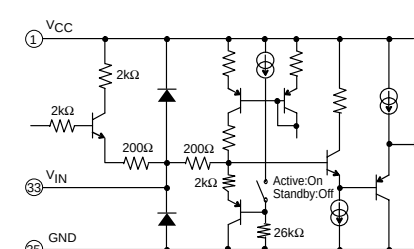
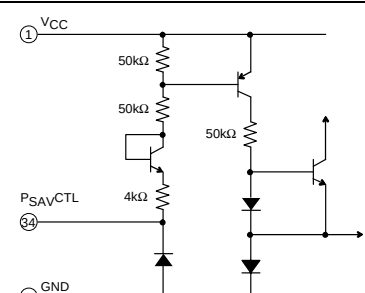
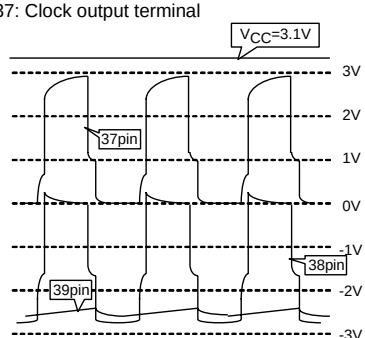
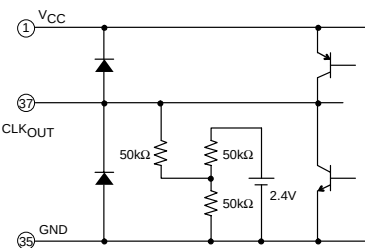
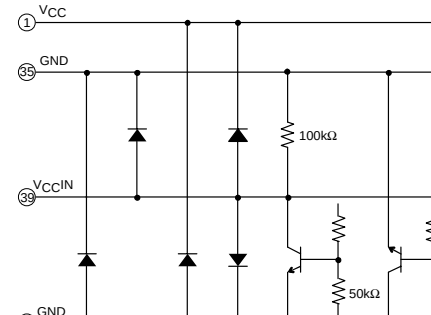
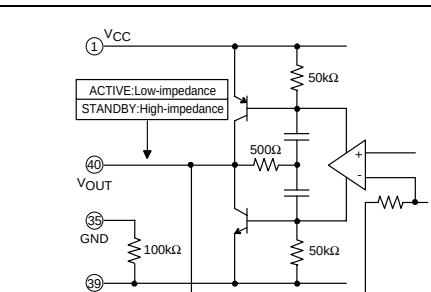
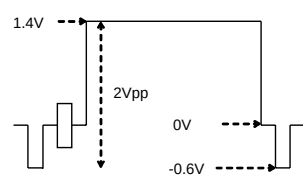
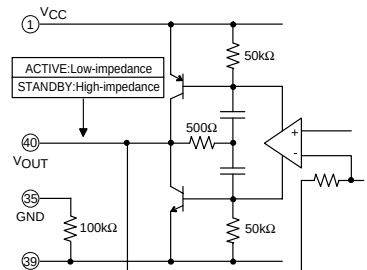
Constructed from preceding page:

Table of Input/Output Forms of LA74310LP (Video Block)

Continued on next page.

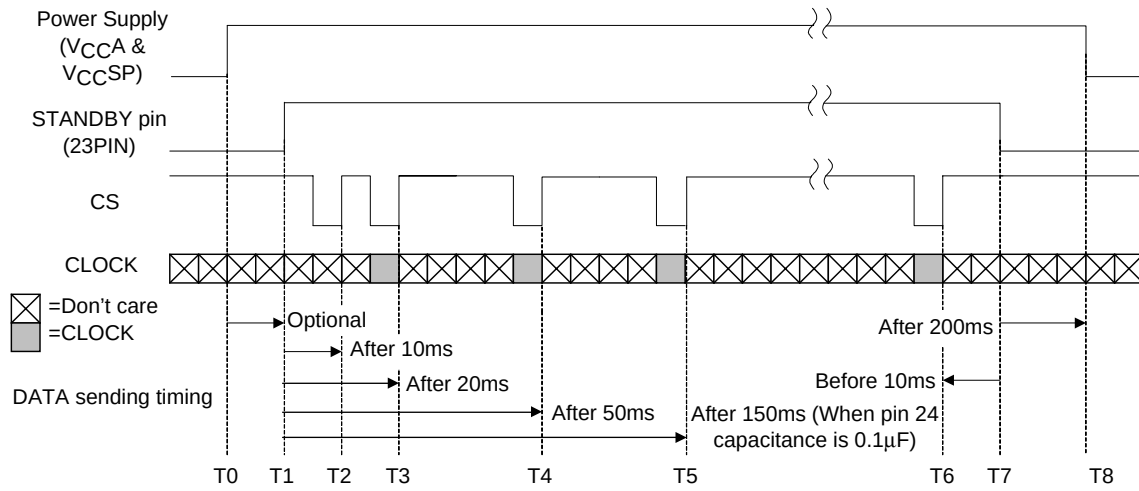
LA74310LP

Consult with your nearest LA74310LP supplier

Pin No.	Pin Name	DC voltage	Description of functions	Equivalent circuit diagram in pin												
33	V _{IN}	1.1V	Video input terminal (Sync-tip clamp (input High-impedance)) GAIN SET: 6dB⇒1.0Vpp GAIN SET: 12dB⇒500mVpp GAIN SET: 16dB⇒317mVpp 													
34	P _{SAV} CTL	V _{CC} or 0V	Power save mode select pin <table><tr><th colspan="3">Control of Pin4</th><th>MODE</th></tr><tr><td>H (V_{CC})</td><td>OPEN or V_{CC}±0.5V</td><td>⇒</td><td>STANDBY</td></tr><tr><td>L (GND)</td><td>0V to 0.3V</td><td>⇒</td><td>ACTIVE</td></tr></table>	Control of Pin4			MODE	H (V _{CC})	OPEN or V _{CC} ±0.5V	⇒	STANDBY	L (GND)	0V to 0.3V	⇒	ACTIVE	
Control of Pin4			MODE													
H (V _{CC})	OPEN or V _{CC} ±0.5V	⇒	STANDBY													
L (GND)	0V to 0.3V	⇒	ACTIVE													
35	GND	0V														
36	NC		NC pin													
37	CLK _{OUT}	+3.0V ↑↓ 0V	Pin37: Clock output terminal 													
38	ND	+0.5V ↑↓ -2.6V (-V _{CC})	Pin38: The terminal which transmits an electric charge 													
39	V _{CC} N	0V ↑↓ -2.5V (-V _{CC})	Pin39: Negative V _{CC}													
40	V _{OUT}	0V	Video output terminal (Push-pull output Low-impedance) 													

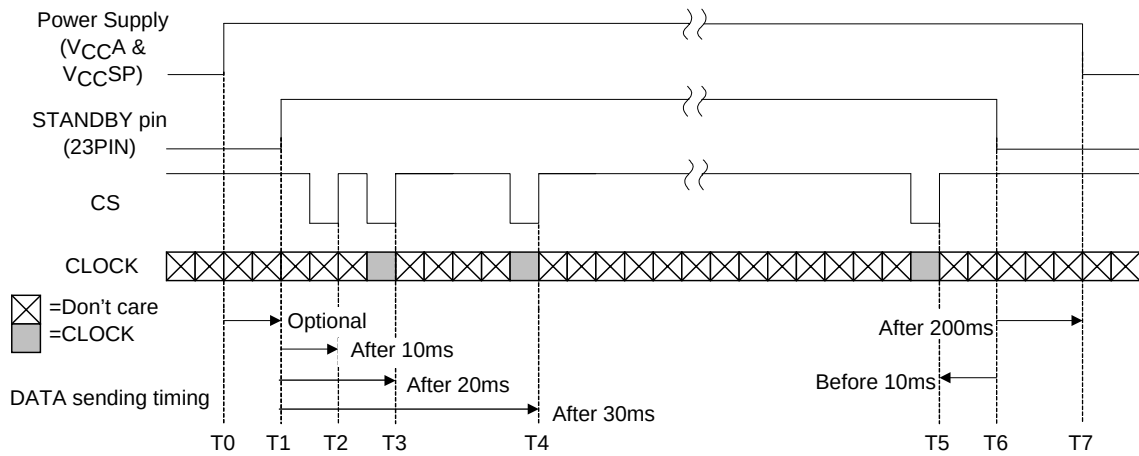
POP Sound Avoiding Sequence

① Upon STANDBY cancellation & control (PBMODE)



Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW		REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA
		*	0:11kHz	0:ON	0:ON	0:ON	(1, *): REC (0, 0): PB Analog		0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital		1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON
T1	Standby cancellation	DATA unnecessary															
T2	Dummy communication (only CS)																
T3	VREF charging circuit: OFF	0	0/1	1	1	1	0	0/1	1	1	0	1	0	0	0	0	0
T4	Speaker AMP: ON	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	0
T5	Line AMP: ON	0	0/1	1	1	1	0	0/1	1	0	1	0	0	0	0	0	0
T6	Return to the initial state	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
T7	Standby control	DATA unnecessary															

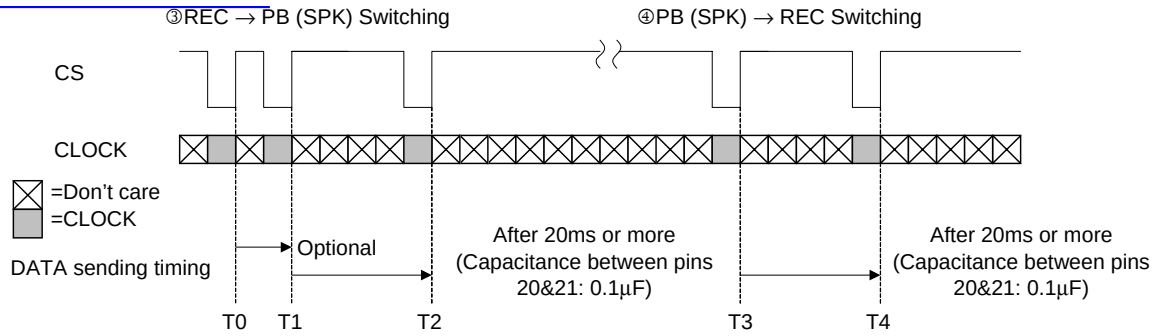
②Upon STANDBY cancellation & control (RECMODE)



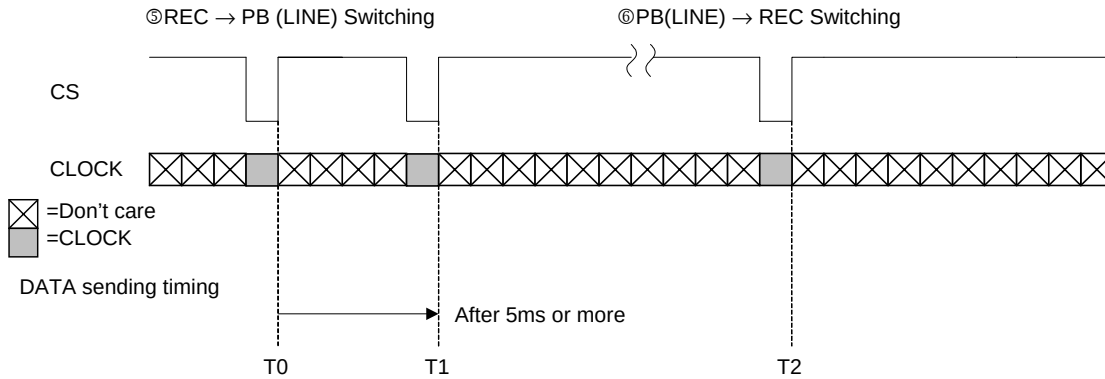
Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			LPF	CHRG	MIC	ALC	LPF MODESW	REC	LINE	LINE	SPK	EVR1	EVR2	EVR4	EVR8	EVR16	
		DMY	C SW	P SW	P SW	P SW		P SW	P SW	MUTE	P SW	DATA	DATA	DATA	DATA	DATA	
		*	0:11kHz	0:ON	0:ON	0:ON	(1, *): REC (0, 0): PB Analog	0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF	
	*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital	1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON		
T1	Standby cancellation	DATA unnecessary															
T2	Dummy communication (only CS)																
T3	Charging circuit & ALC: OFF, LPF: REC	0	0/1	1	0	1	1	0	0	1	0	1	0	0	0	0	0
T4	ALC: ON	0	0/1	1	0	0	1	0	0	1	0	1	0	0	0	0	0
T5	Return to the initial state	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
T6	Standby control	DATA unnecessary															

LA74310LP

查询"LA74310LP"供应商



Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW		REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA
		*	0:11kHz	0:ON	0:ON	0:ON	(1, *): REC (0, 0): PB Analog		0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital		1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON
T0	Speaker AMP: ON	0	0/1	1	0	0	1	0/1	0	1	0	1	0	0	0	0	0
T1	PBMODE: switching EVR: setting	0	0/1	1	1	1	0	0/1	1	1	0	1	a	a	a	a	a
T2	Speaker AMP: ON	0	0/1	1	1	1	0	0/1	1	1	0	0	a	a	a	a	a
T3	RECMODE: switching EVR: MUTE Speaker AMP: OFF	0	0/1	1	0	0	1	0/1	0	1	0	1	0	0	0	0	0
T4	Speaker AMP: ON	0	0/1	1	0	0	1	0/1	0	1	0	0	0	0	0	0	0

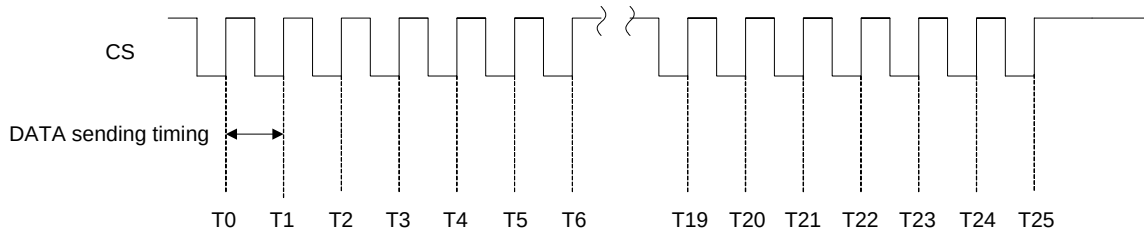


Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW		REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA
		*	0:11kHz	0:ON	0:ON	0:ON	(1, *): REC (0, 0): PB Analog		0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital		1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON
T0	PBMODE: switching	0	0/1	1	1	1	0	0/1	1	1	0	1	0	0	0	0	0
T1	Line AMP: ON Line MUTE: OFF	0	0/1	1	1	1	0	0/1	1	0	1	1	0	0	0	0	0
T2	RECMODE: switching	0	0/1	1	0	0	1	0/1	0	1	0	1	0	0	0	0	0
	Line AMP: ON Line MUTE: OFF	0	0/1	1	0	0	1	0/1	0	1	0	1	0	0	0	0	0

LA74310LP

查询"LA74310LP"供应商

⑦EVR Switching (min → max) 0.25ms/CS



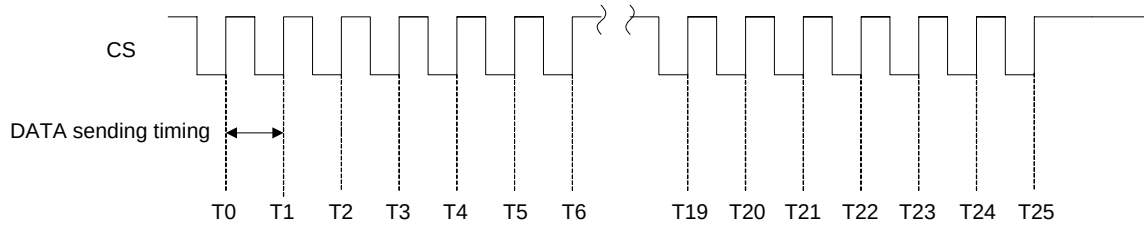
Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW		REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA
		*	0:11kHz	0:ON	0:ON	0:ON	(1, *): REC (0, 0): PB Analog		0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital		1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON
T0	EVRDATA=0	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	0
T1	EVRDATA=7	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	0
T2	EVRDATA=8	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	0
T3	EVRDATA=9	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	0
T4	EVRDATA=10	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	0
T5	EVRDATA=11	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	0
T6	EVRDATA=12	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	0
T7	EVRDATA=13	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	0
T8	EVRDATA=14	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	0
T9	EVRDATA=15	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	0
T10	EVRDATA=16	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	1
T11	EVRDATA=17	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	0	1
T12	EVRDATA=18	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	0	1
T13	EVRDATA=19	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	0	1
T14	EVRDATA=20	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	0	1
T15	EVRDATA=21	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	0	1
T16	EVRDATA=22	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	0	1
T17	EVRDATA=23	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	1
T18	EVRDATA=24	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	1
T19	EVRDATA=25	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	1
T20	EVRDATA=26	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	1
T21	EVRDATA=27	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	1
T22	EVRDATA=28	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	1
T23	EVRDATA=29	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	1
T24	EVRDATA=30	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	1
T25	EVRDATA=31	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	1

Note) DATA1 to 6 are the mute area of EVR characteristics and jumped due to no generation of POP noise.

LA74310LP

[查询"LA74310LP"供应商](#)

⑧EVR Switching (max → min) 0.25ms/CS



Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW		REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA
		*	0:11kHz	0:ON	0:ON	0:ON	(1, *): REC (0, 0): PB Analog		0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital		1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON
T0	EVRDATA=31	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	1
T1	EVRDATA=30	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	1
T2	EVRDATA=29	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	1
T3	EVRDATA=28	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	1
T4	EVRDATA=27	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	1
T5	EVRDATA=26	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	1
T6	EVRDATA=25	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	1
T7	EVRDATA=24	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	1
T8	EVRDATA=23	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	1
T9	EVRDATA=22	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	0	1
T10	EVRDATA=21	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	0	1
T11	EVRDATA=20	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	0	1
T12	EVRDATA=19	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	0	1
T13	EVRDATA=18	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	0	1
T14	EVRDATA=17	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	0	1
T15	EVRDATA=16	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	1
T16	EVRDATA=15	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	0
T17	EVRDATA=14	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	0
T18	EVRDATA=13	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	0
T19	EVRDATA=12	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	0
T20	EVRDATA=11	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	0
T21	EVRDATA=10	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	0
T22	EVRDATA=9	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	0
T23	EVRDATA=8	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	0
T24	EVRDATA=7	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	0
T25	EVRDATA=0	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	0

Note) DATA1 to 6 are the mute area of EVR characteristics and jumped due to no generation of POP noise.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of September, 2007. Specifications and information herein are subject to change without notice.